pcim
ASIA

Accurate Characterization of the Gate Charge for SiC MOSFETs based on Double Pulse Test Scheme

Chenghui Qian, UniSiC Technology (Shanghai) Co., Ltd.

UniSiC Products Introduction

Wafer Level Dynamic, Static, UIS Test

Wafer Level Dynamic Burn-in Test

Dynamic,Static Test → **Gate Charge Test**

UIS, Rg/Cg, DVDS, ISO Test

Dynamic Burn-in Test

Surge Current Test

Power Cycling Test

Chip Probing Test → **Known Good Die Test** → **Final Test** → **System Level Test**

Chip Level Dynamic, Static Test

DHTOL On-board Aging Test

Continuous Power Test

Qg Test Background

Purpose:

Gate driving loss calculation

High frequency switching performance evaluation

...

Qg Test for SiC MOSFETs

Challenge:

Qgs & Qgd extraction

Vgsth hysteresis

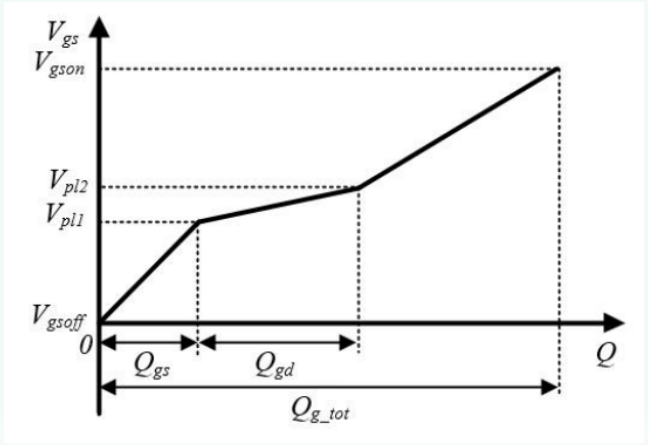
No uniform test method

Accuracy & Repeatability

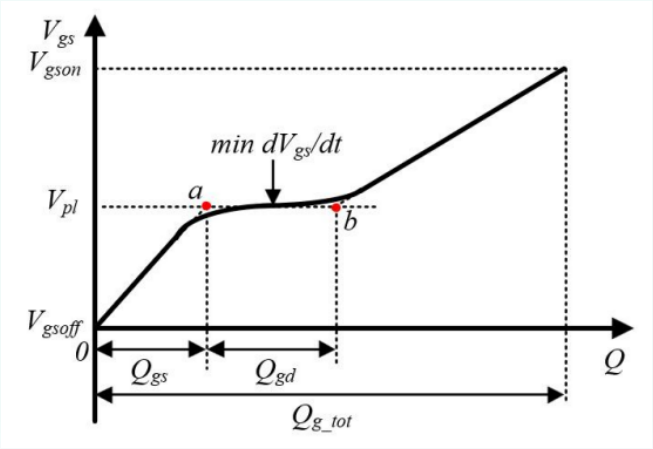
Test cost

...

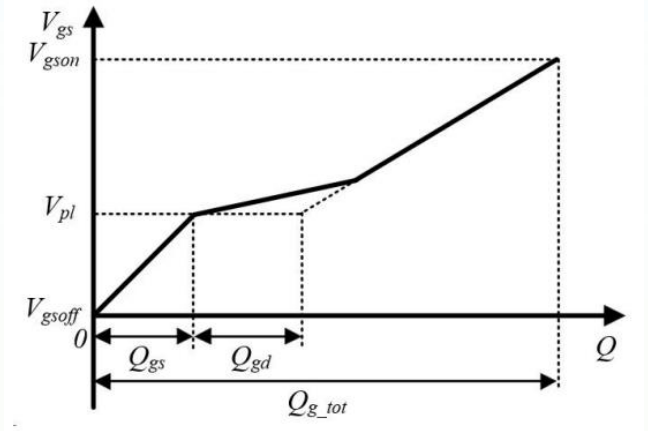
Qg Test Background



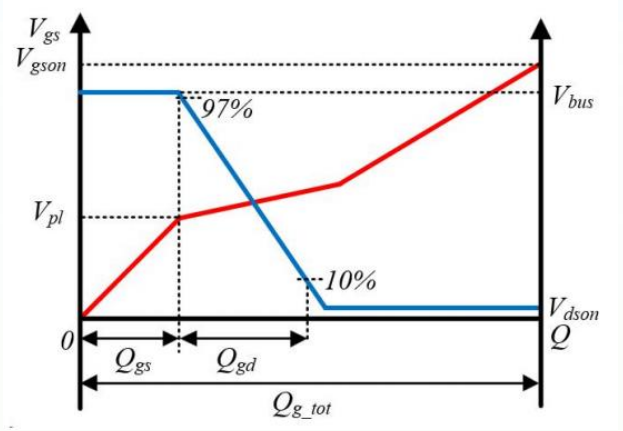
(a)



(b)



(c)

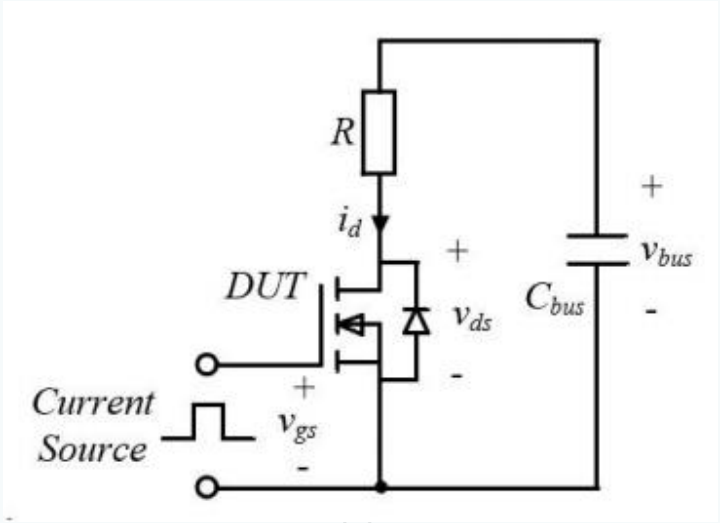


(d)

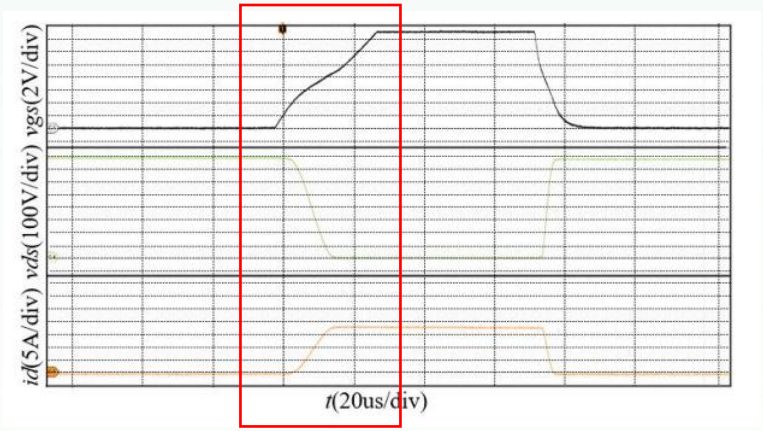
- Vgs-Qg curve and four Qg_tot, Qgs,Qgd extraction method
- **The key is to get the accurate Vgs-Qg curve.**

[1] JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, Gate Charge Test Method, JESD24-2, 2002
[2] JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, Guidelines for Gate Charge (QG) Test Method for SiC MOSFET, JEP192, 2022
[3] T. Basler, D. Heer, D. Peters, T. Aichinger and R. Schoerner, "Practical Aspects and Body Diode Robustness of a 1200 V SiC Trench MOSFET," PCIM Europe; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2018, pp. 1- 7

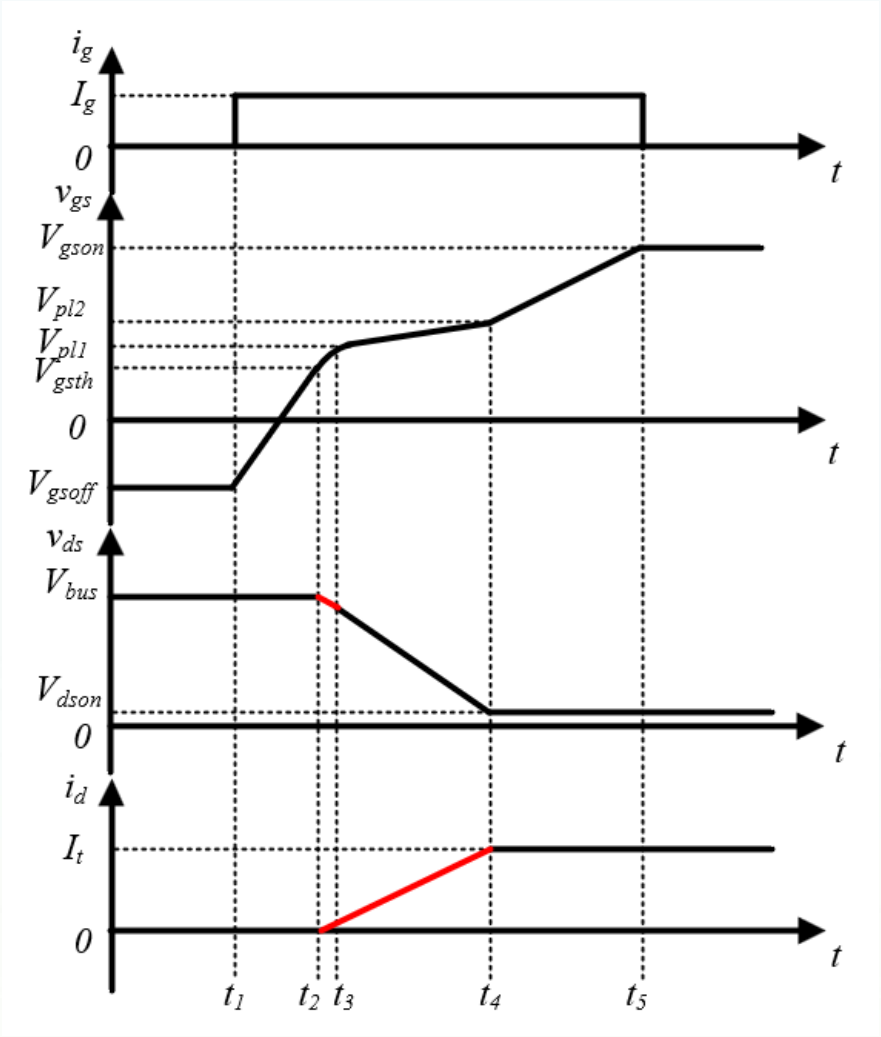
Qg Test Method - Single pulse test with resistive load



(a)



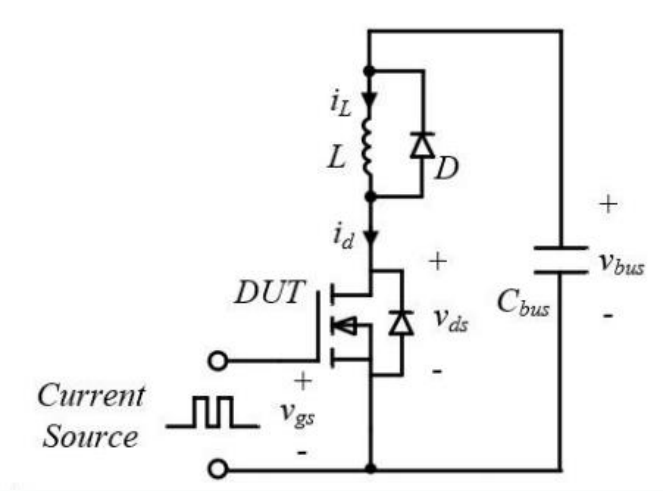
(b)



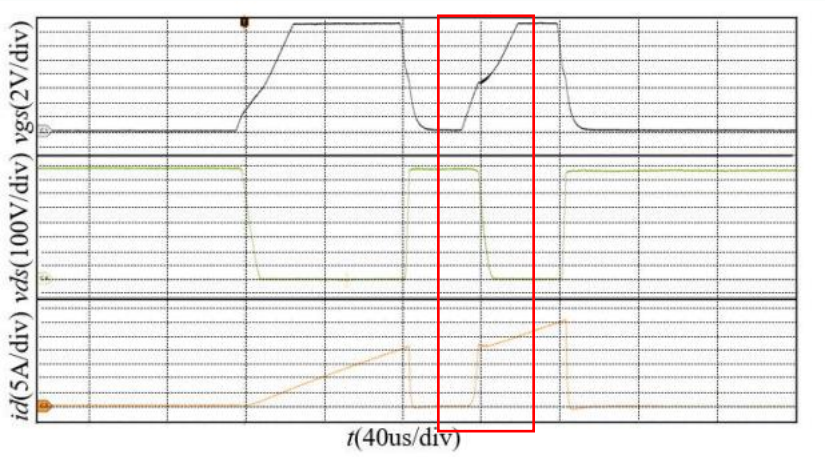
(c)

- R = Vbus/It
- **vds and id variation** of DUT due to the voltage drop at resistor at "Miller Ramp"
- **Stepwise regulation** of the target Id

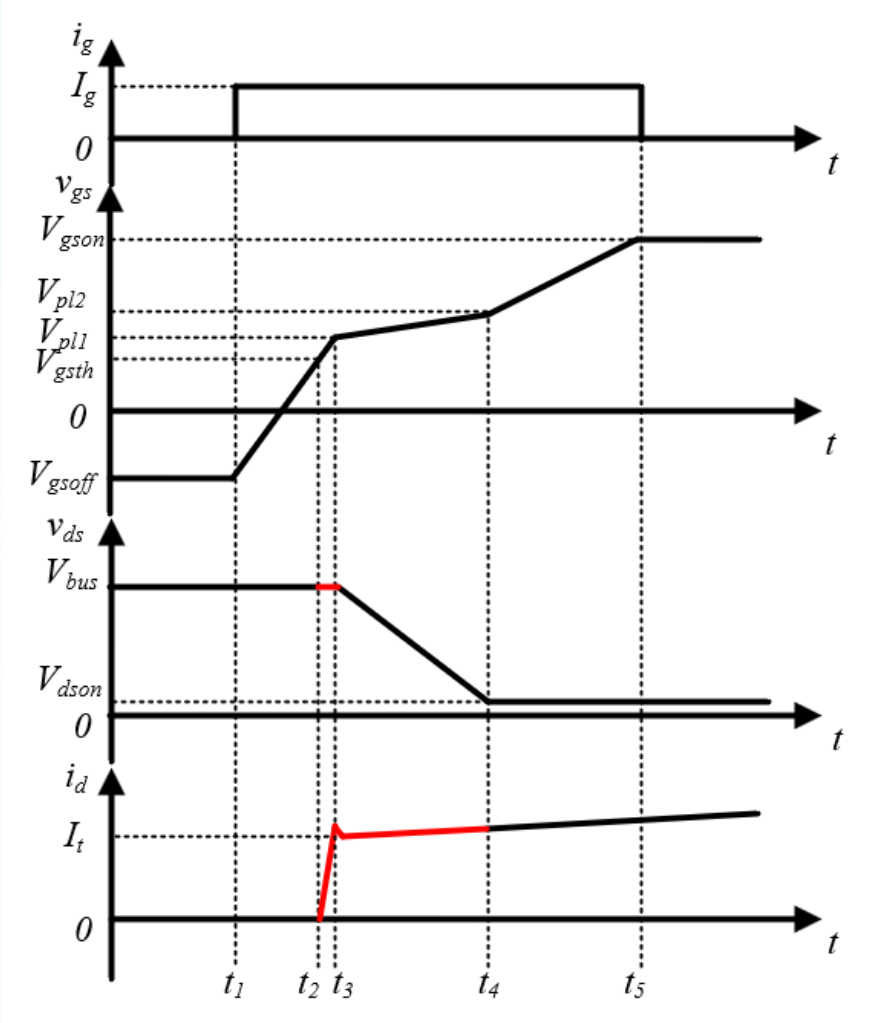
Qg Test Method - Double pulse test



(a)



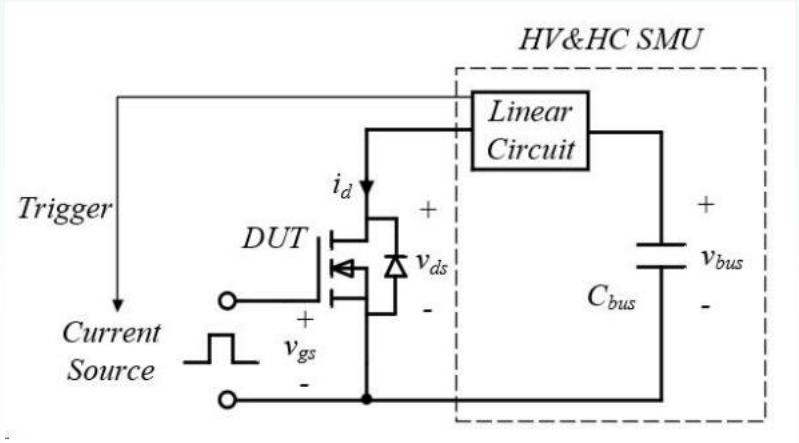
(b)



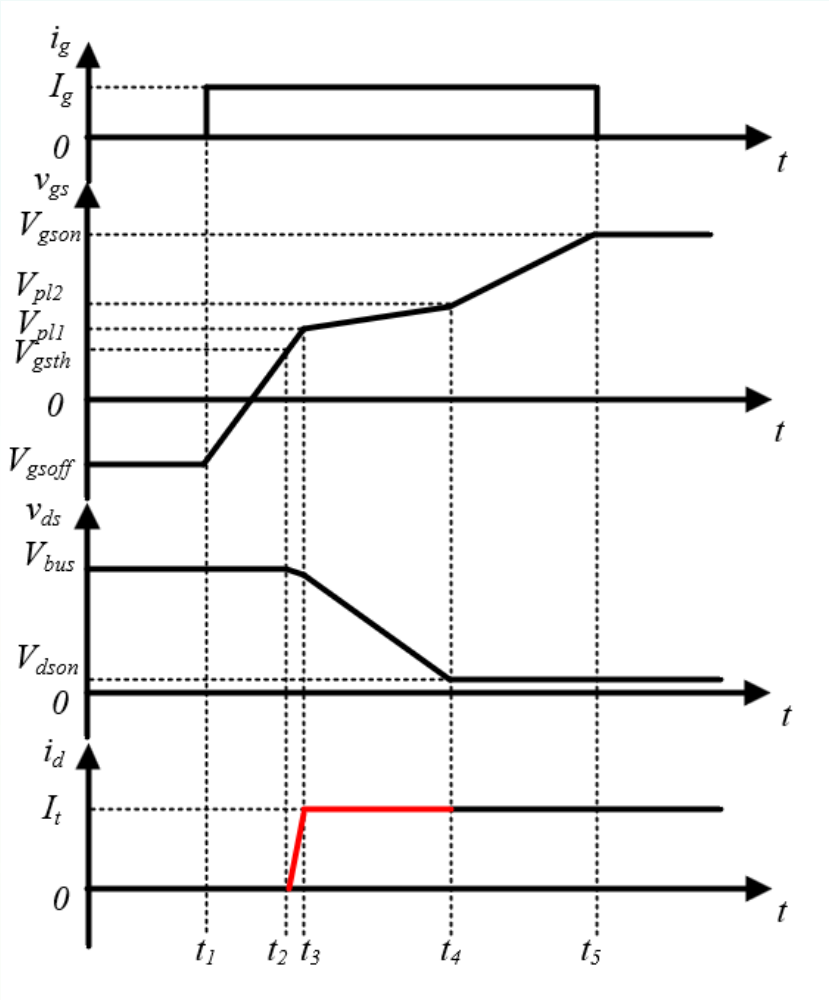
(c)

- Extracting the turning-on process of the second pulse
- **The increment of id depends on the value of L and ig.**
- The target Id is adjusted by the width of the first pulse.

Qg Test Method - Single pulse test with high voltage and high current SMU



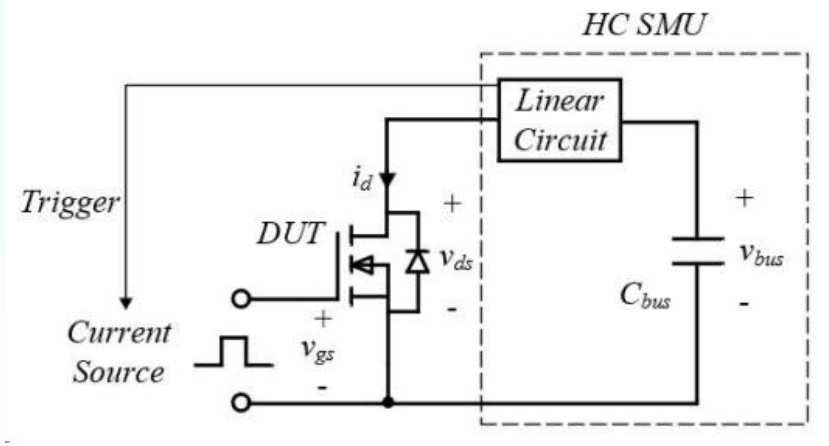
(a)



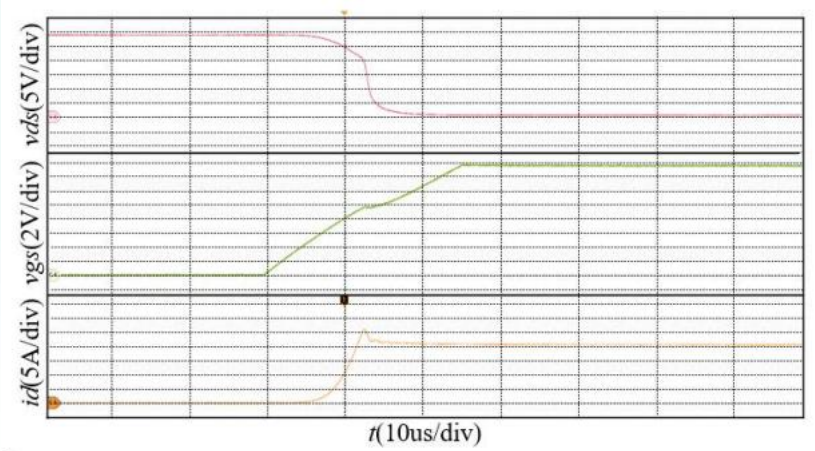
(b)

- Constant and adjustable id is implemented by SMU at CC mode.
- **It is difficult to develop such a high voltage and high current SMU.**

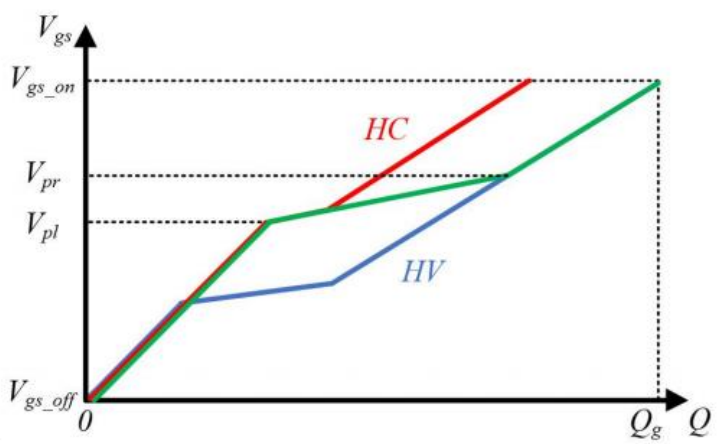
Qg Test Method – Single pulse test by combining HC & HV curves



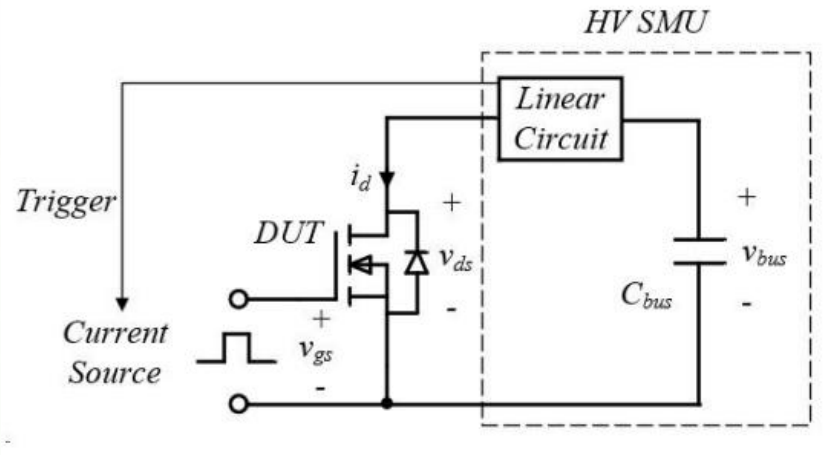
(a)



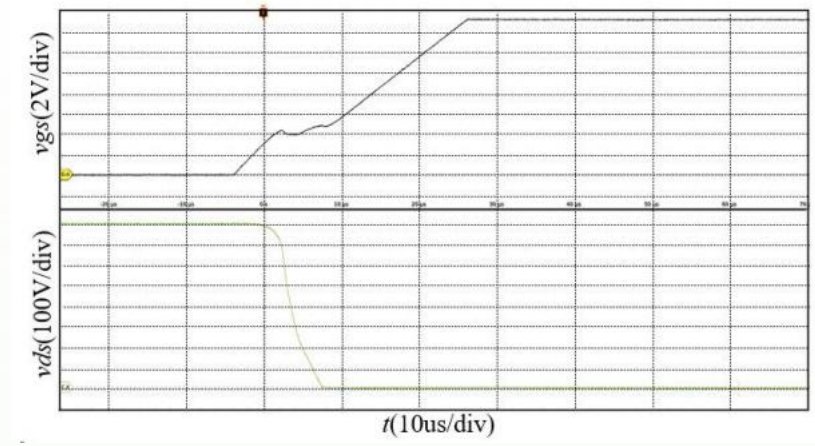
(b)



(c)



(d)

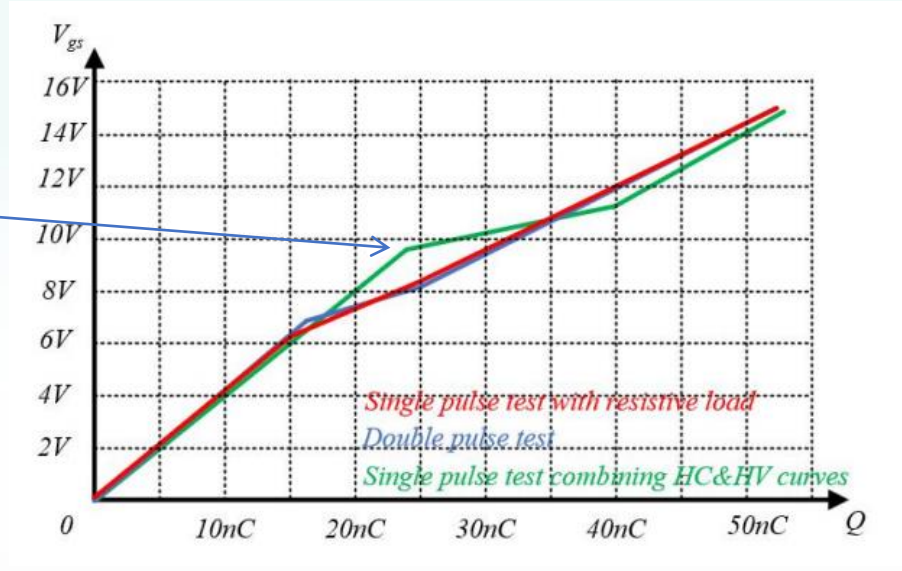


(e)

- Single pulse test with high current and low voltage SMU.
- Single pulse test with low current and high voltage SMU.
- **Combining the two Vgs-Qg curves.**
- Safe due to lower power needed.

Qg Test Method Comparison

	Single pulse test with resistive load	Double pulse test	Single pulse test with high voltage and high current SMU	Single pulse test by combining HC & HV curves
Accurate?	YES	YES	YES	**NO**
Easy to implement?	YES	YES	NO	YES
Stepless current regulation?	NO	YES	YES	YES
For Test equipment	/	Dynamic	Static	Static
Cost	Medium	Low	High	Low

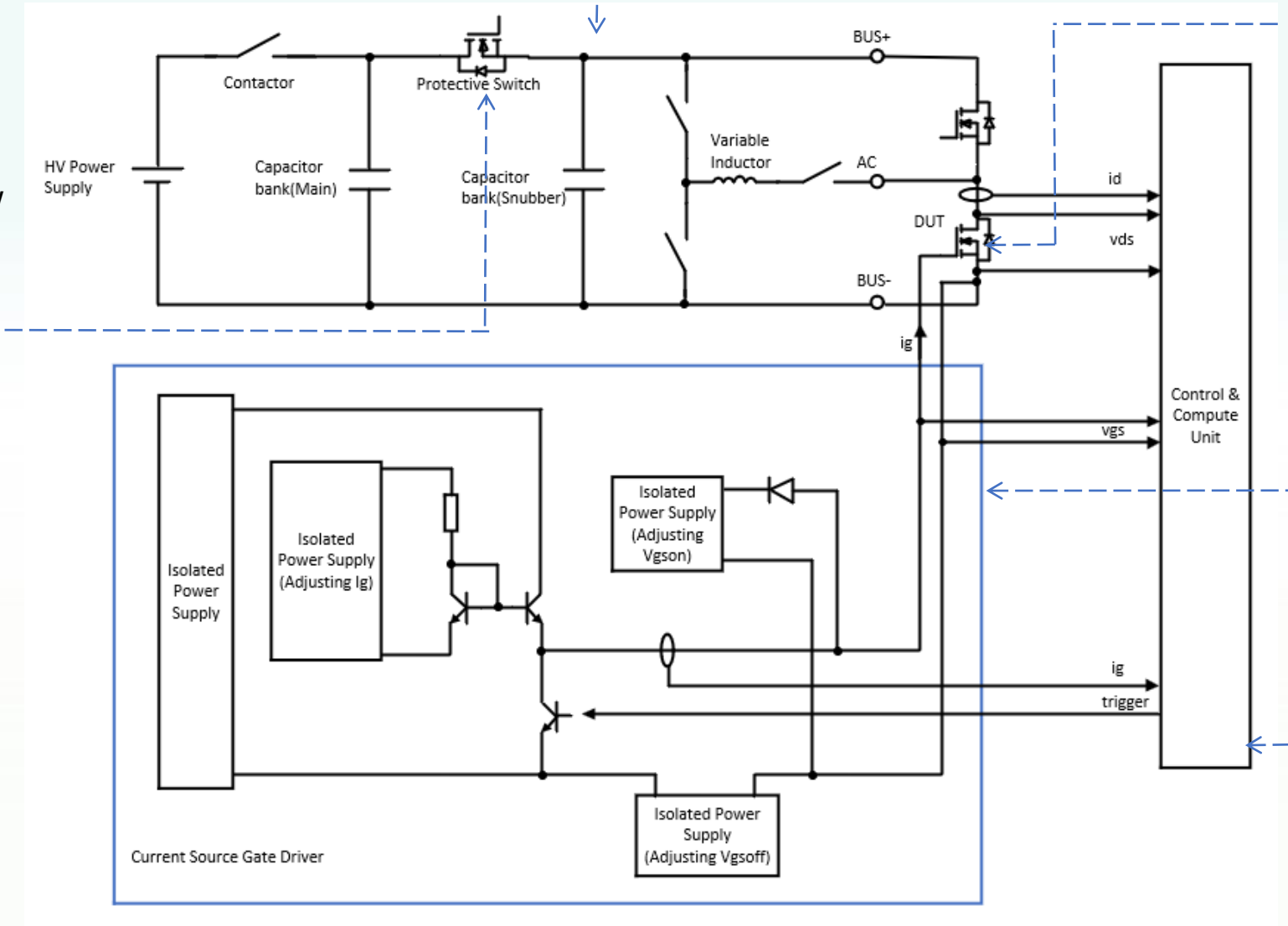


- DUT: Infineon SiC MOSFET IMZ120R045M1
- Ig: 1.8mA

- **DIBL of SiC MOSFETs causes the incorrect Vpl for the low voltage and high current test.**

UniSiC Solution

- Innovative laminated busbar and capacitor bank design. Ultra-low stray inductance(**6nH**)
- Solid-state protective switch with a protection response time **< 500ns**



- Fully covering the test of power modules and discrete devices.
- Multi-range current source gate driver with **adjustable Vgsoff,Vgson and Ig**.
- Parasitic capacitor compensation. Qg accuracy at **0.1nC**

Conclusion

- Considering accuracy,realizability and other factors, **double pulse test scheme of Qg test** is the most suitable for SiC MOSFETs.
- Single pulse test with high voltage and high current SMU is a potential way for Qg test.
- **Adjustable Vgsoff,Vgson and Ig** is important for the assessment of Qg.

THANKS!