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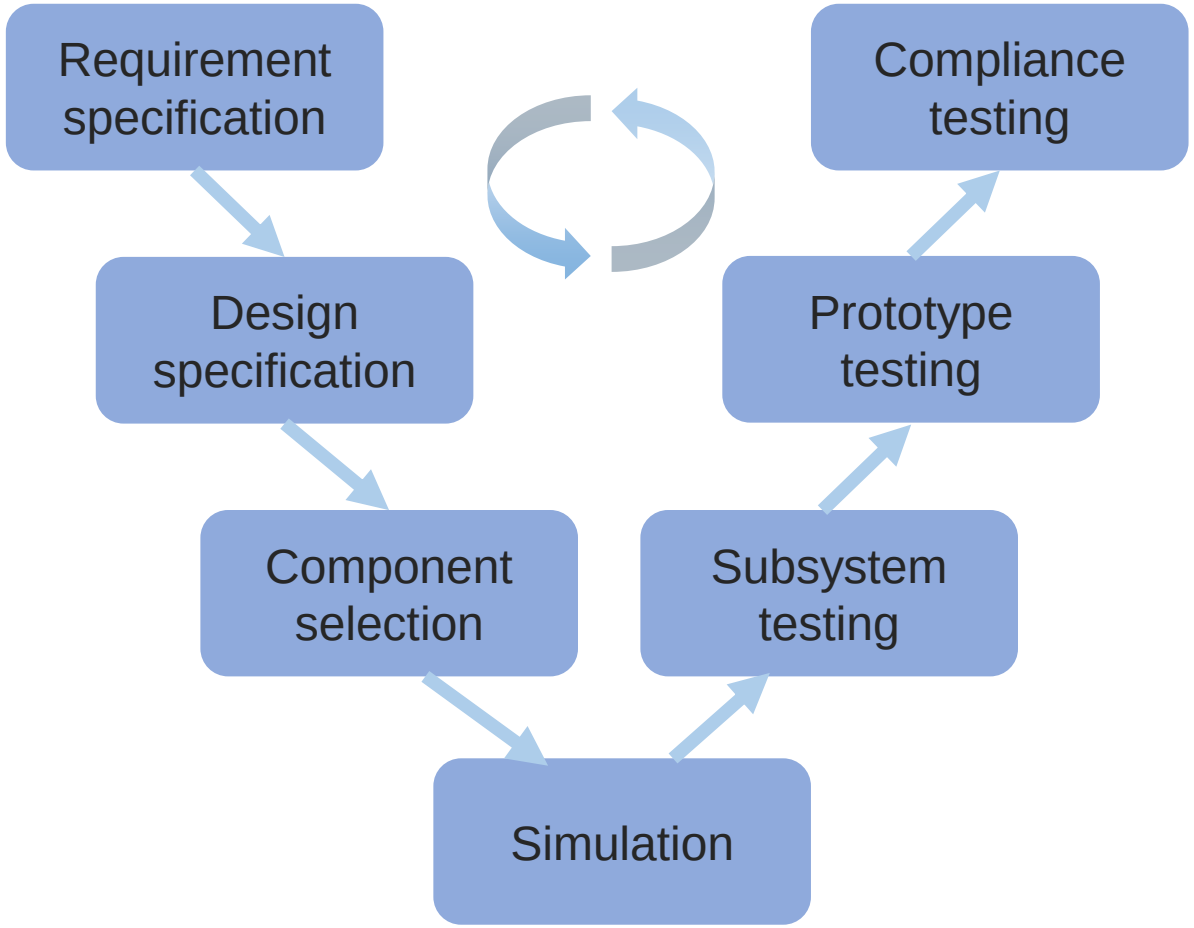
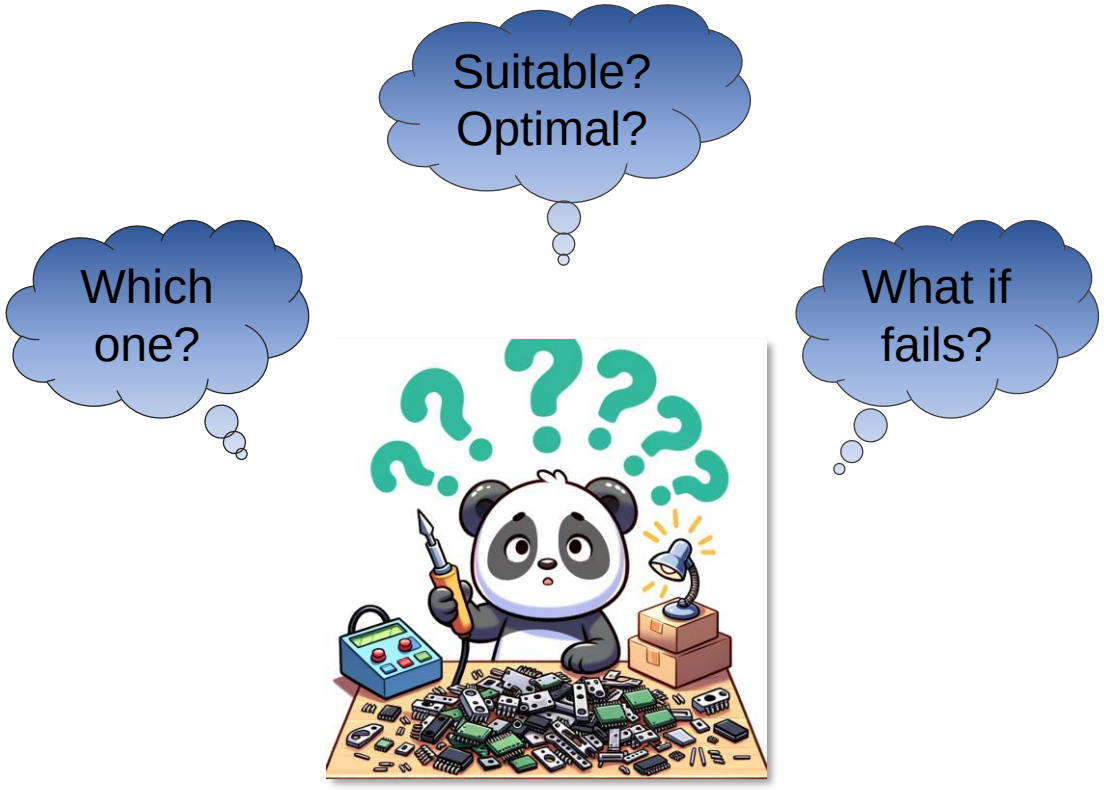
# PowerBrain: An automatic data extraction tool for semiconductor datasheets

Fanghao Tian, KU Leuven - EnergyVille

# Choosing a component is complex

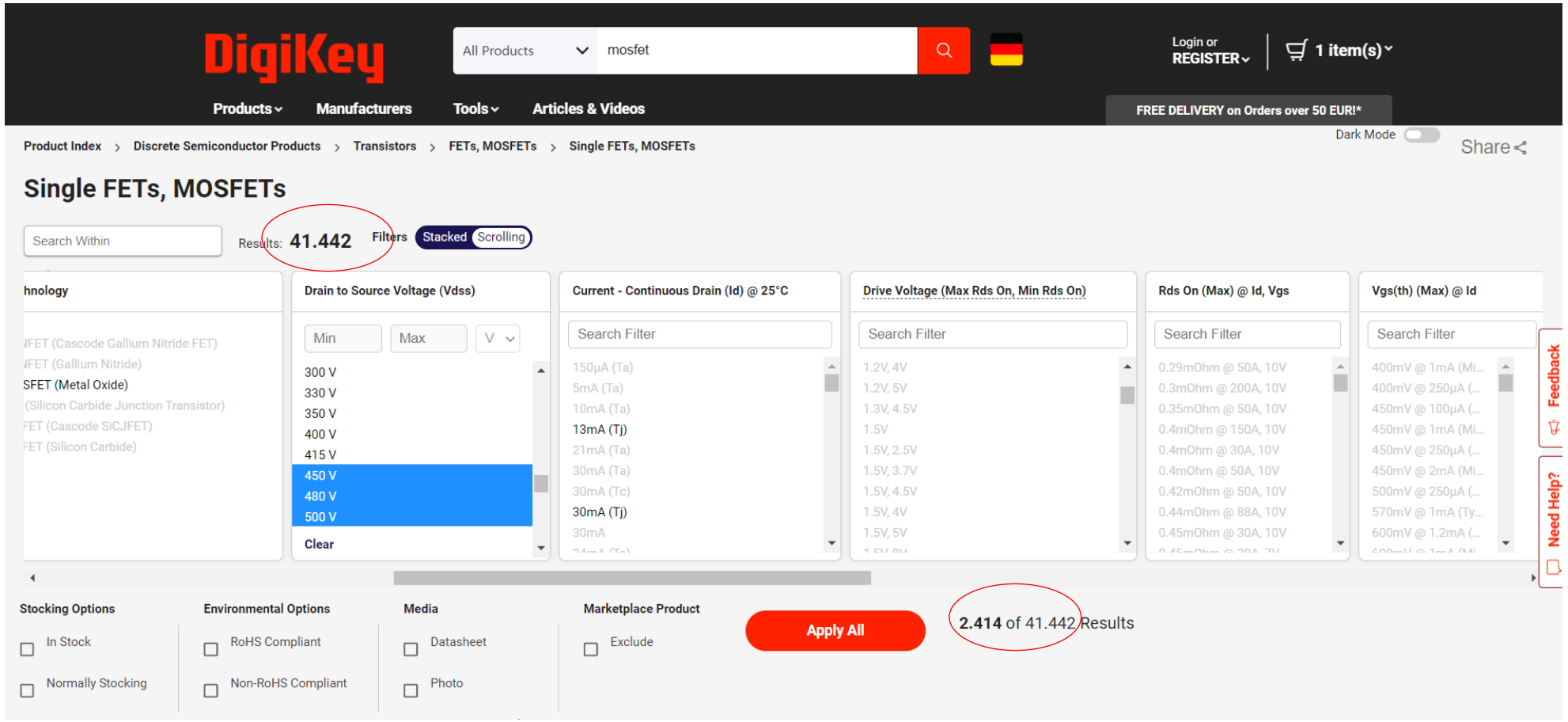
A general design flow of power electronics




 https://attend.ieee.org/dmc-2022/machine-readable-data-sheet-for-power-semiconductors-and-how-it-helps-to-pave-the-way-for-design-automation/

# Our Market is flooded with Available Choices




 https://www.digikey.de/en/products/filter/single-fets-mosfets/278?s=N4IgTCBcDaILYHsDOAzApgFxAXQL5A

# PowerBrain can collect data in mins

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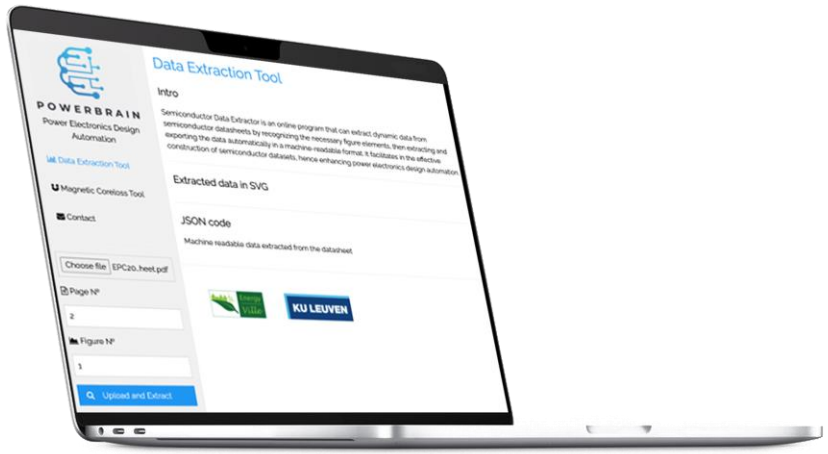
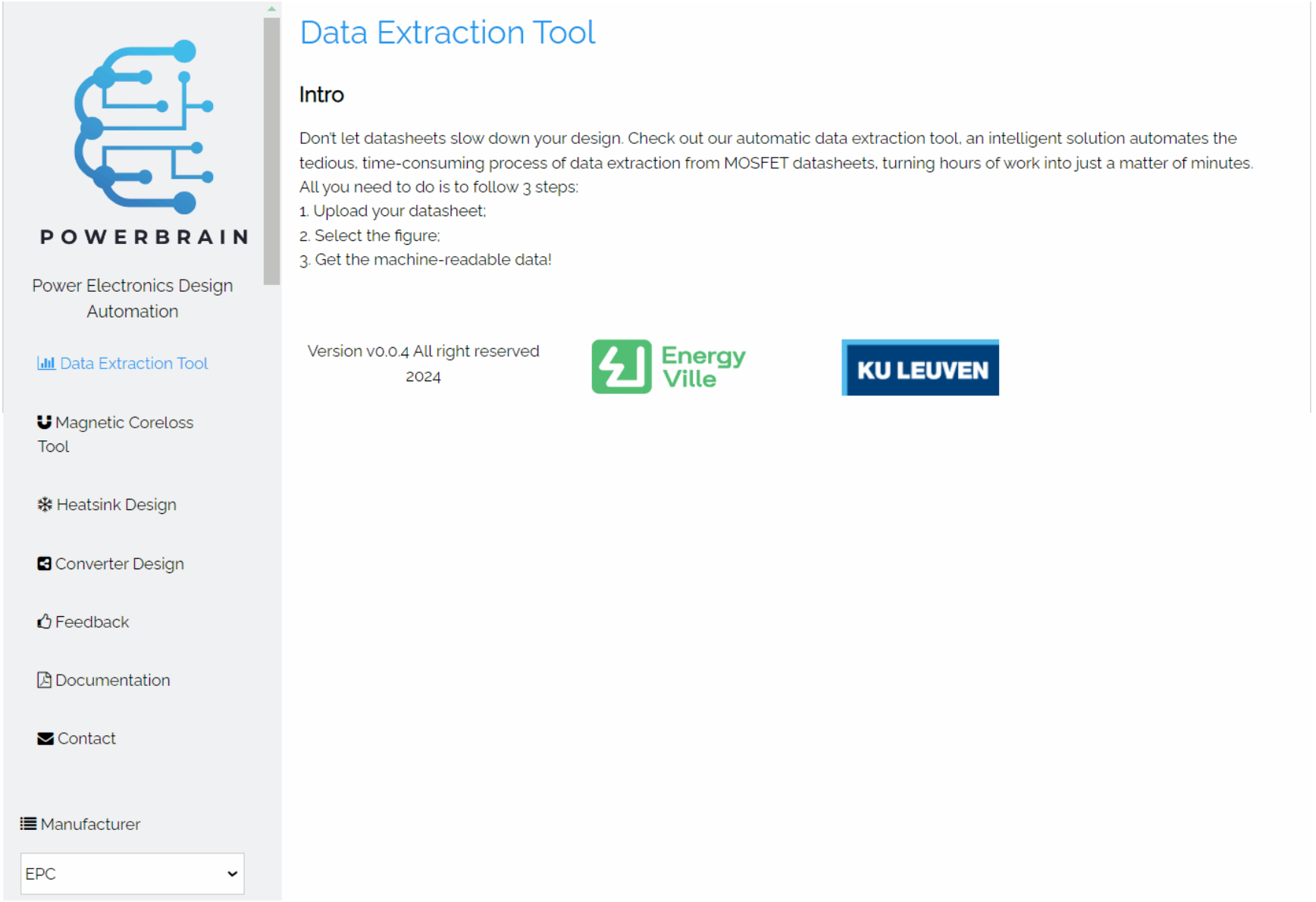
POWERBRAIN

**DON'T LET DATASHEETS SLOW YOU DOWN!**

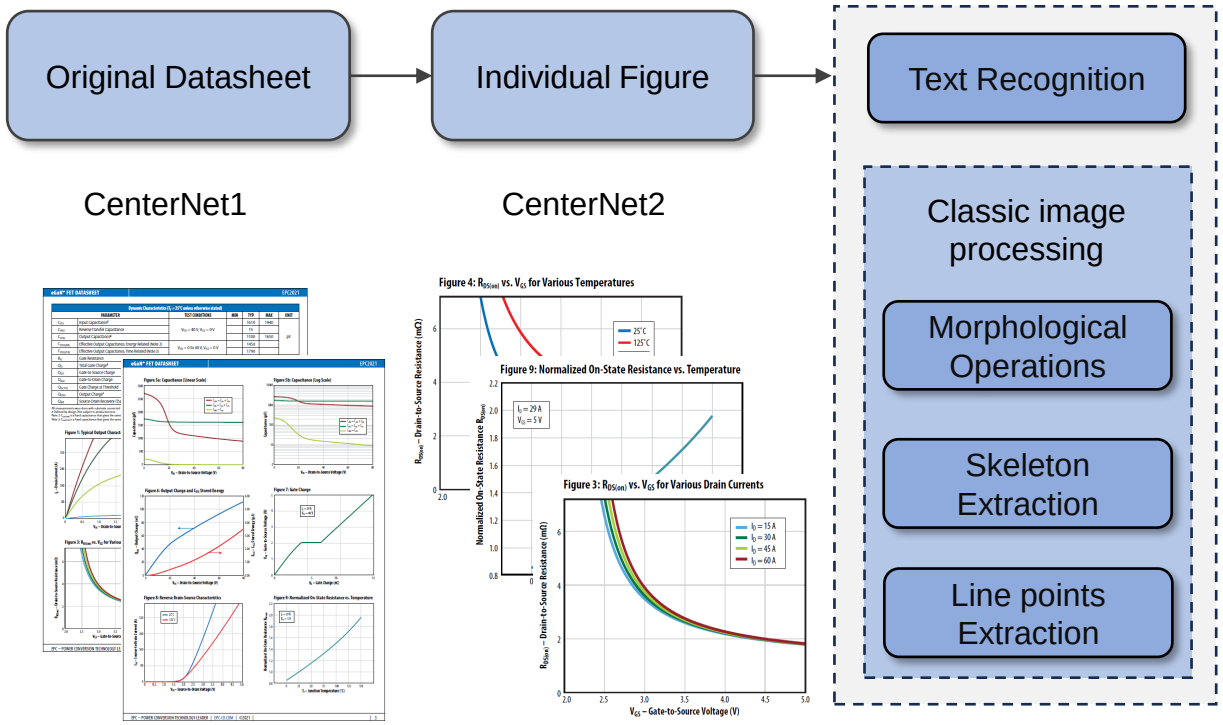
1. Upload Your Datasheet
2. Select the Figure
3. Get Machine Readable Data



# Demonstration of a case



# The overview of PowerBrain

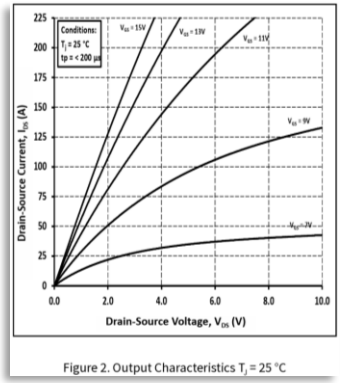



**Task1**: Detect figures from original datasheet page

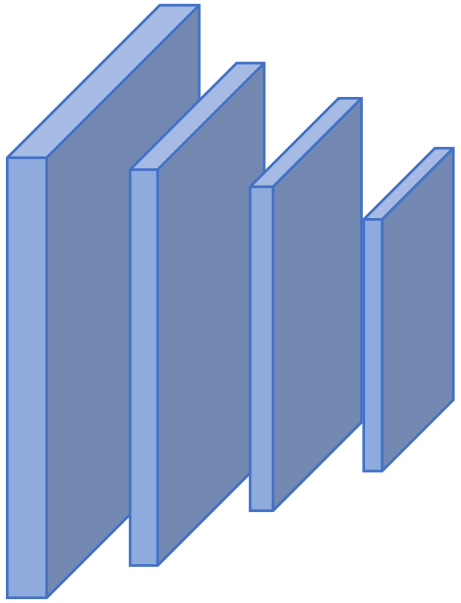
Task2: Extract data from individual Line Chart

- Object detection: detect key elements: title, legend, label, value, corner, and others
- Text recognition: Recognize texts & numbers
- Data extraction: Extract line pixels and align it with coordination

# Structure of CenterNet - Object Detection




(512,512,3)



(16,16,2048)

Backbone-(ResNet50)

Transposed Convolution

High-resolution feature maps

(128,128,64)

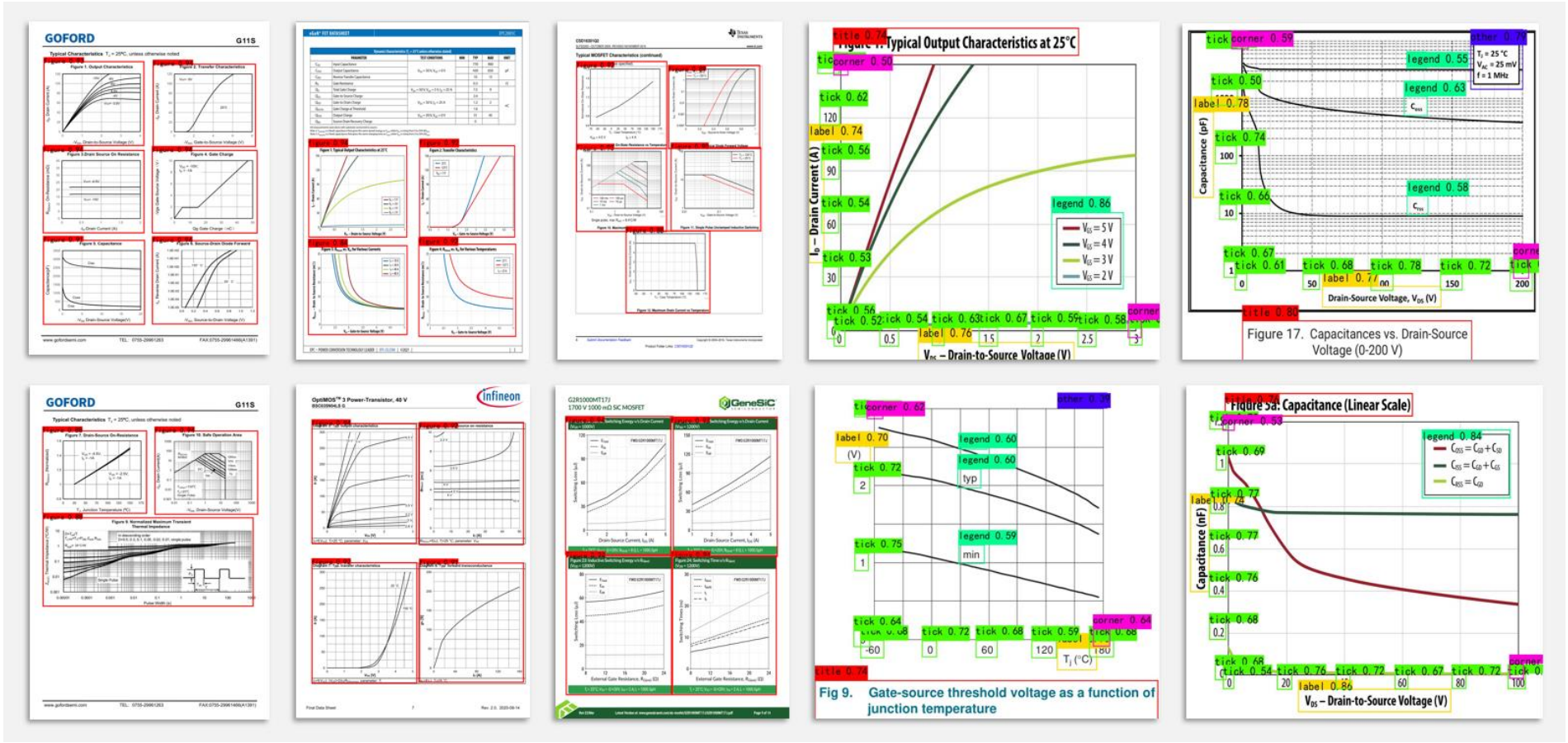
Category

Center Position

Width & Length

# Results of CenterNet

CenterNet based object detection algorithm applied to detect the key elements from the datasheet






F. Tian, et al, "Automatic Data Extraction Based on Semiconductor Datasheet for Design Automation of Power Converters," IPEC, 2022.

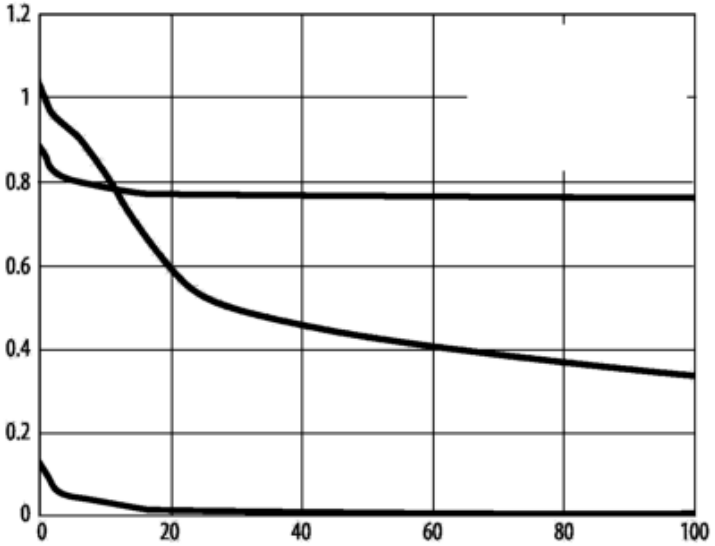
# Automatic Data Extraction – Line Data Extraction

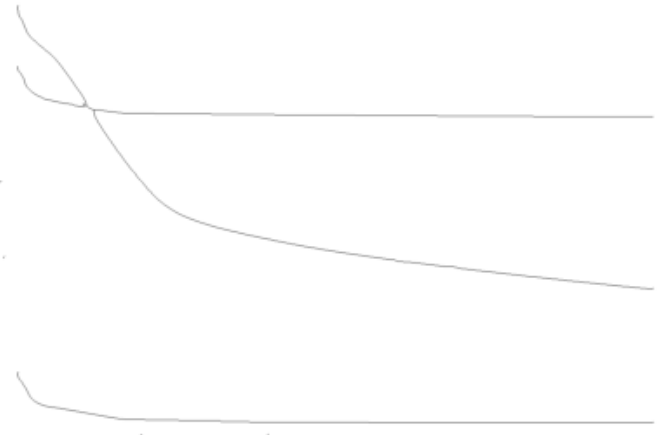
Binarized image

Align mark values and grids to determine coordination

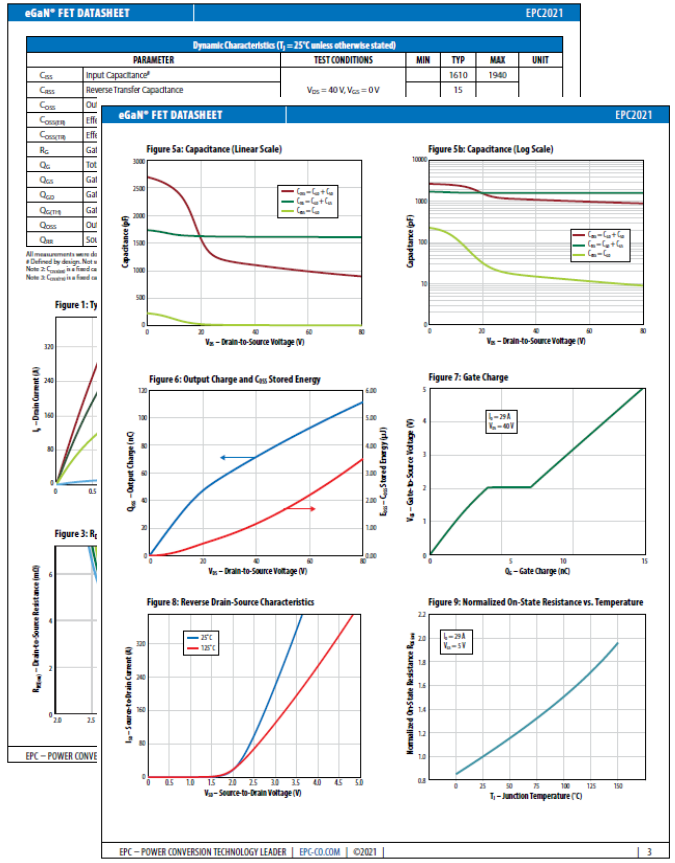
Morphological image processing techniques

Skeleton



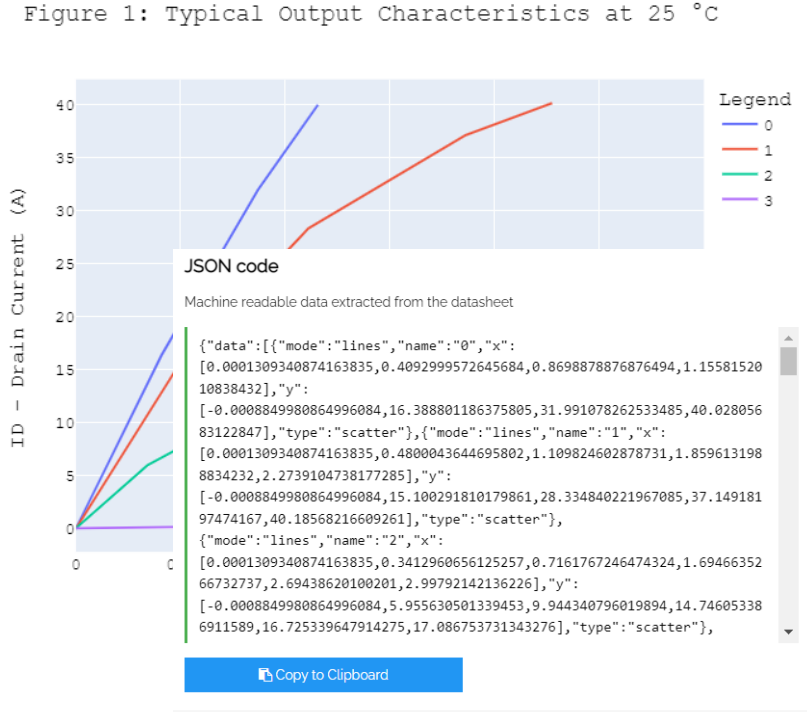



# PowerBrain Interpret the Datasheet to Machine-Readable




Original Datasheet

POWERBRAIN




Machine Readable Data

# Data needed for Power Loss Model

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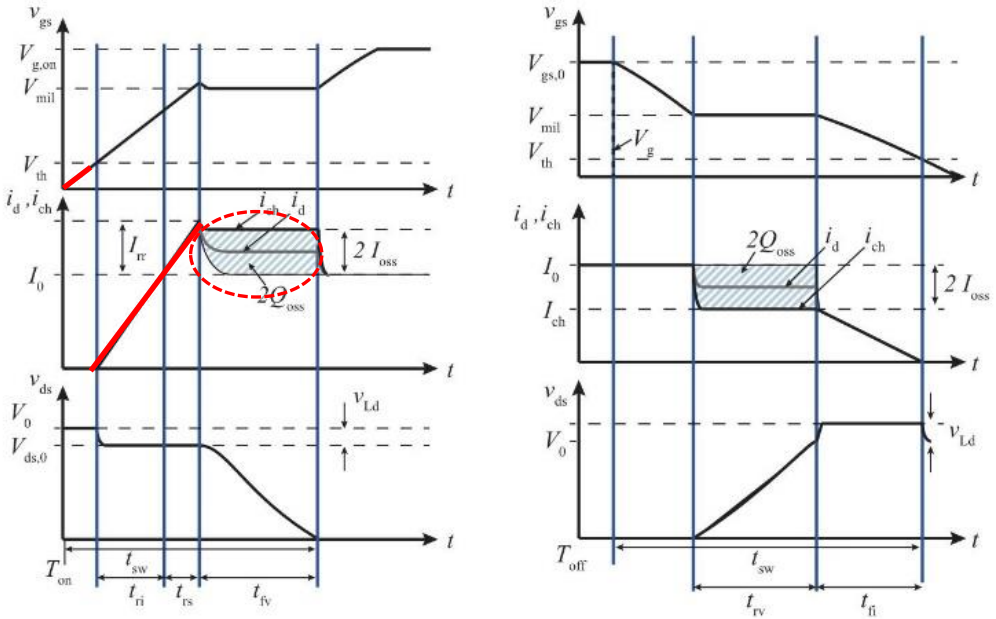
Switching Process of SiC MOSFET




(a) Turn-on process (b) Turn-off process

$$E_{Ton} = \frac{1}{2} t_{ri} V_{ds} I_o + \frac{1}{2} t_{fv} V_{ds} (I_o - 2I_{oss}) + t_{rs} V_{ds} I_o + E_{rr}$$

$$t_{fi} = -ln(\frac{V_{th} + V_g}{V_{mil} + V_g})(C_{gs} Rg + L_s g_m)$$

$$t_{ri} = -ln(1 - \frac{I_o}{g_m (V_g - V_{th})})(C_{gs} Rg + L_s g_m)$$

$$E_{Toff} = \frac{1}{2} t_{rv} V_o (I_o - 2I_{oss}) + \frac{1}{2} t_{fi} (V_o + V_{Ld})(I_o - 2I_{oss})$$

$$t_{rv} = \frac{Q_{coss,discharge}}{I_{coss,discharge}}$$

$$t_{fv} = -\frac{Q_{coss,charge}}{I_{coss,charge}}$$

$$E_{cond} = I^2_{ds(rms)} R_{ds(on)} T$$



D. Christen and J. Biela, ”Analytical Switching Loss Modeling Based on Datasheet Parameters for mosfets in a Half-Bridge,” in IEEE Transactions on Power Electronics.

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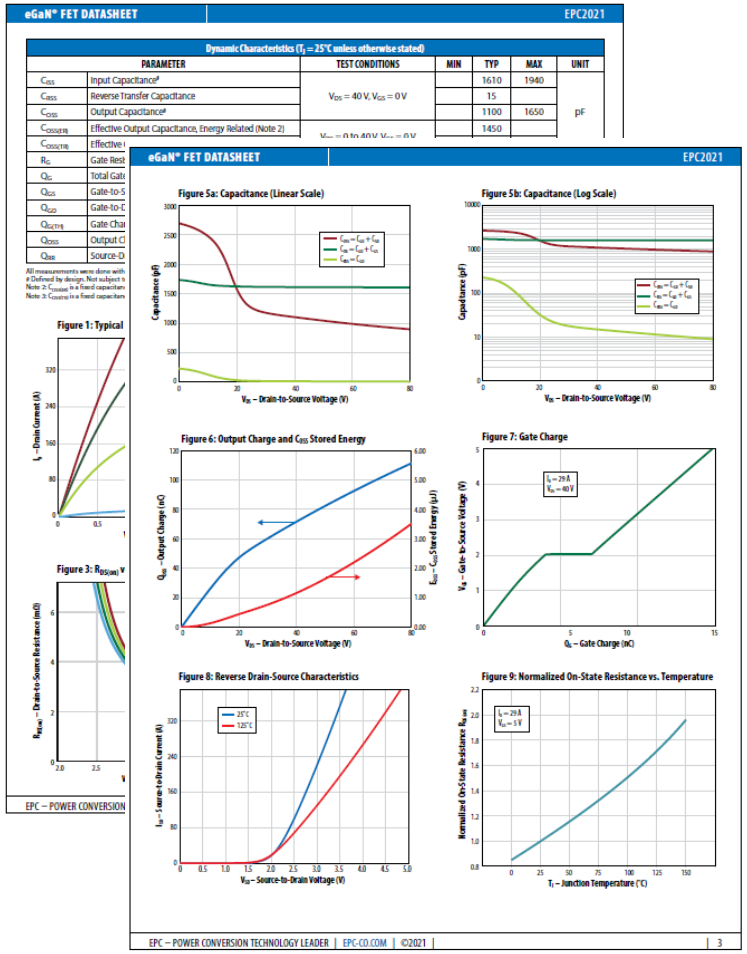
# Conduction Loss



eGaN® FET DATASHEET EPC2021

Dynamic Characteristics ($T_J$ = 25°C unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_{ISS}$ | Input Capacitance* | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V | | 1610 | 1940 | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | 15 | | |
| $C_{OSS}$ | Output Capacitance* | | | 1100 | 1650 | |
| $C_{OSS(ER)}$ | Effective Output Capacitance, Energy Related (Note 2) | | | 1450 | | |

Figure 1: Typical

Figure 3: $R_{DS(on)}$

Figure 5a: Capacitance (Linear Scale)

Figure 5b: Capacitance (Log Scale)

Figure 6: Output Charge and $C_{OSS}$ Stored Energy

Figure 7: Gate Charge

Figure 8: Reverse Drain-Source Characteristics

Figure 9: Normalized On-State Resistance vs. Temperature

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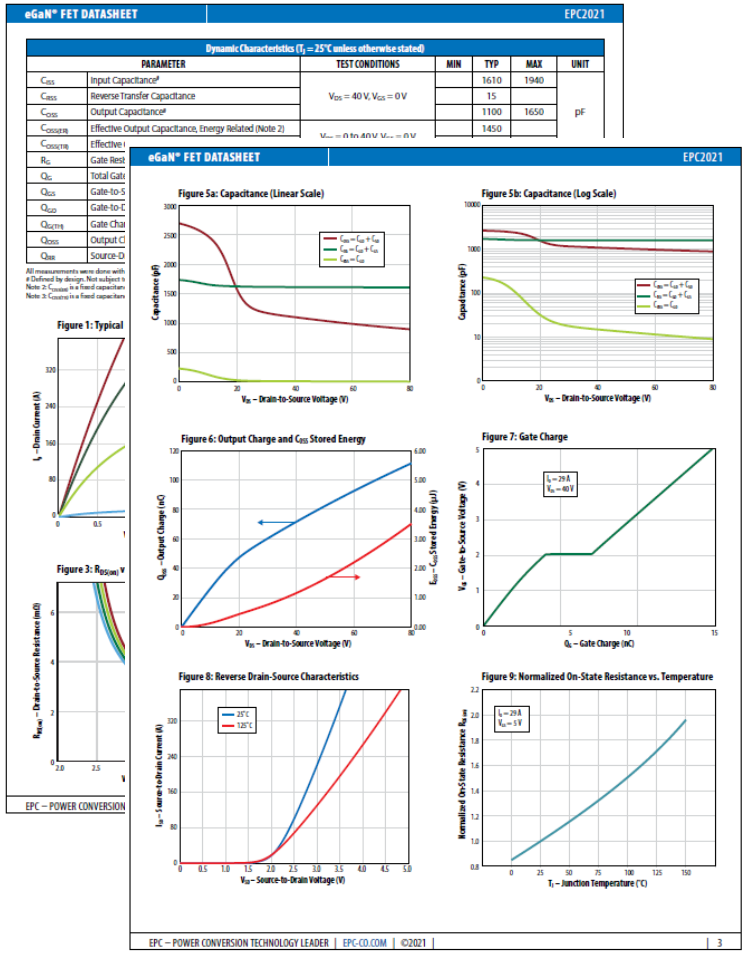
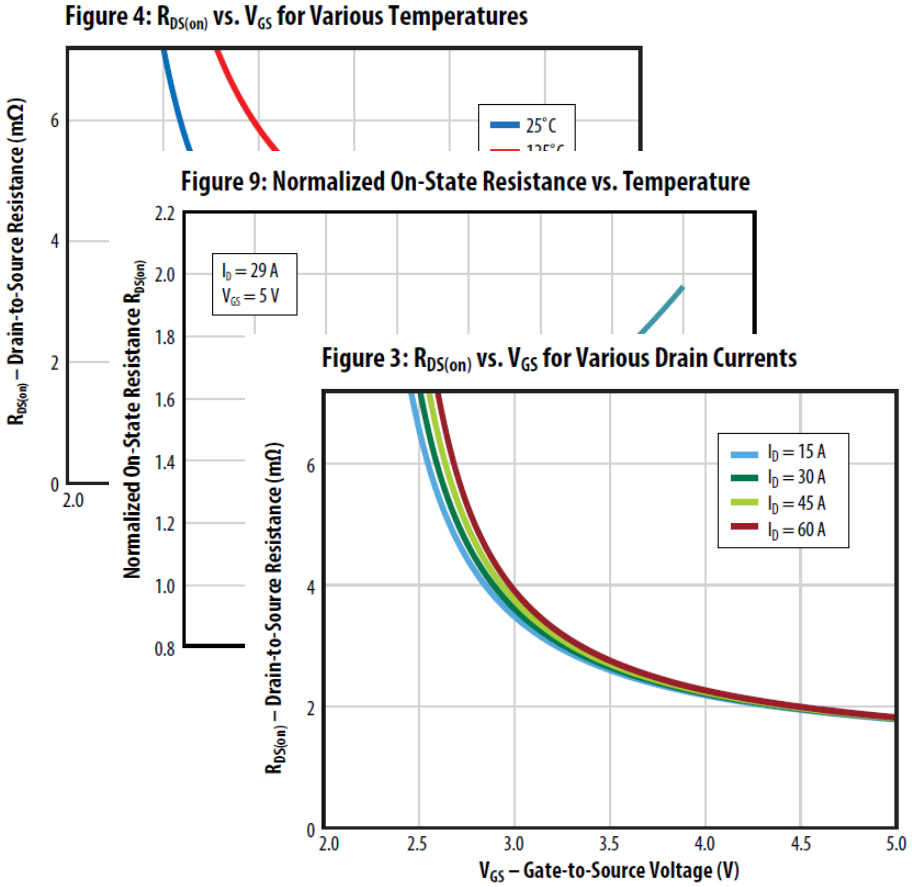
8/13/2024 https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2021_datasheet.pdf

# Conduction Loss

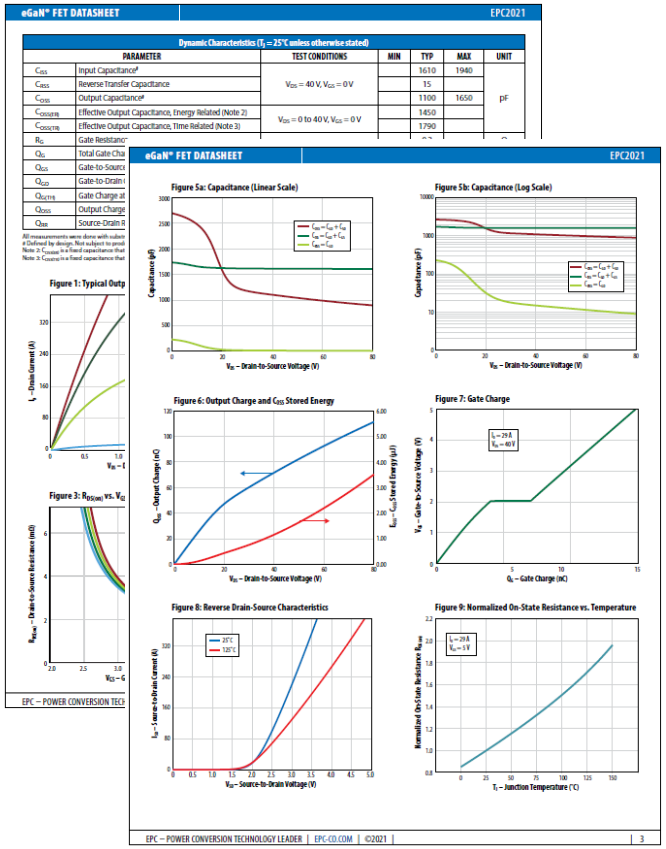


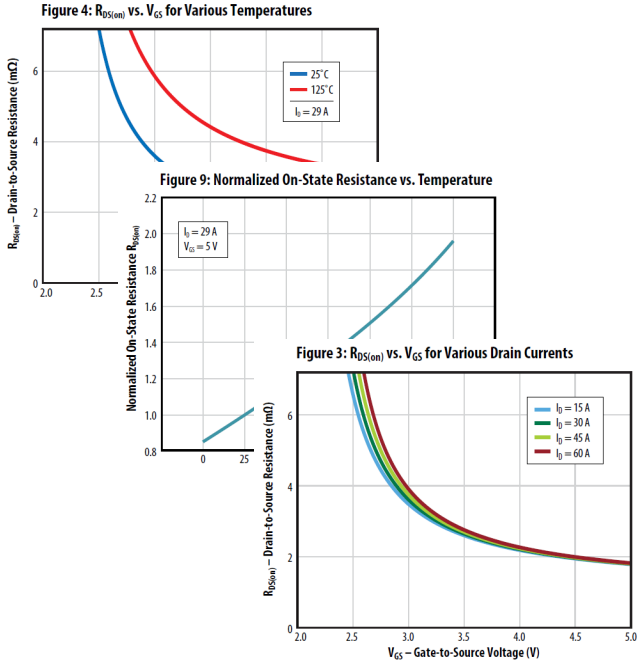



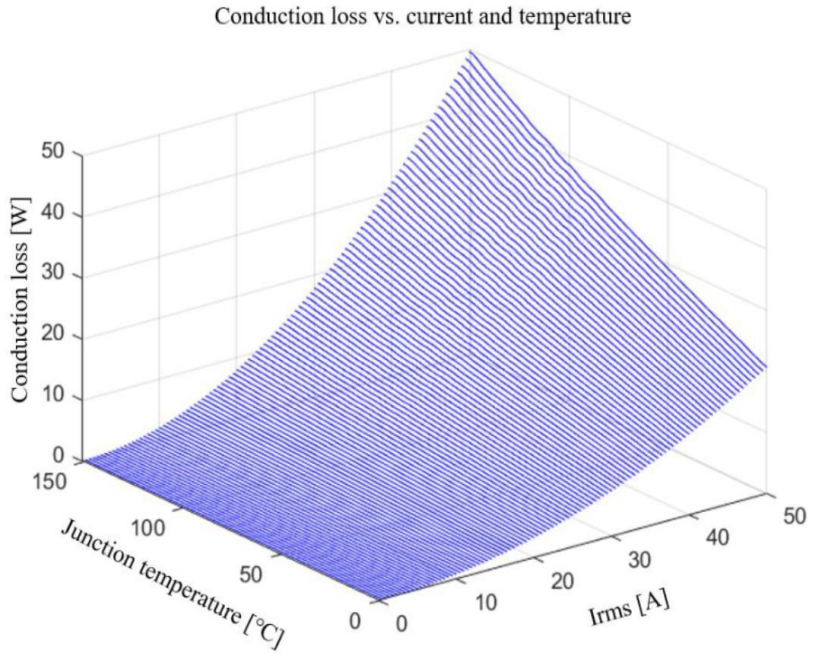



https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2021_datasheet.pdf

# Conduction Loss



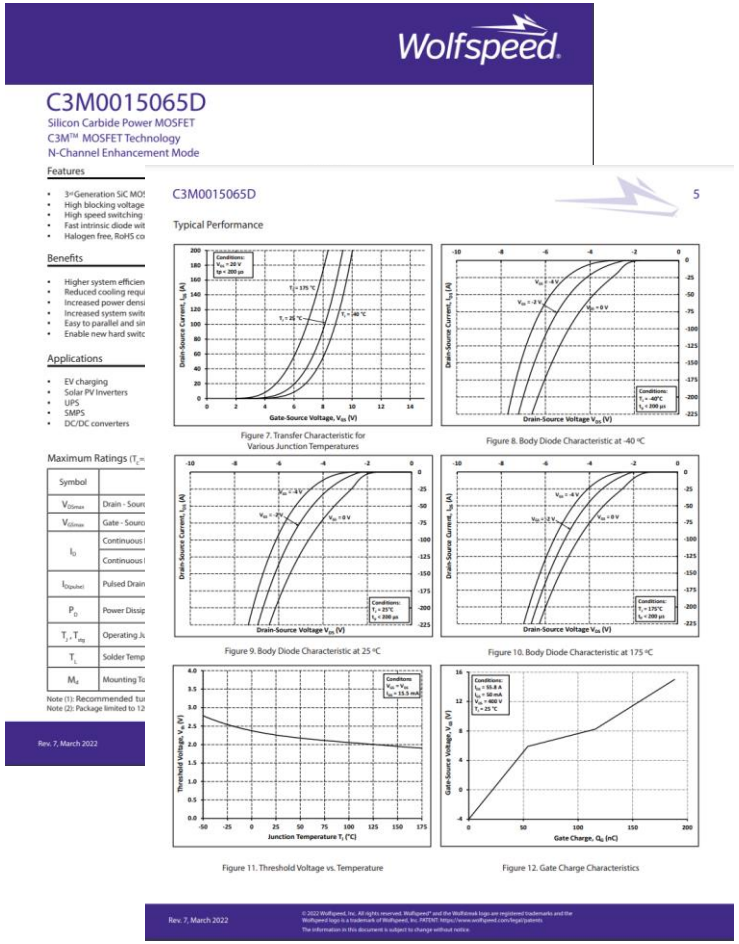



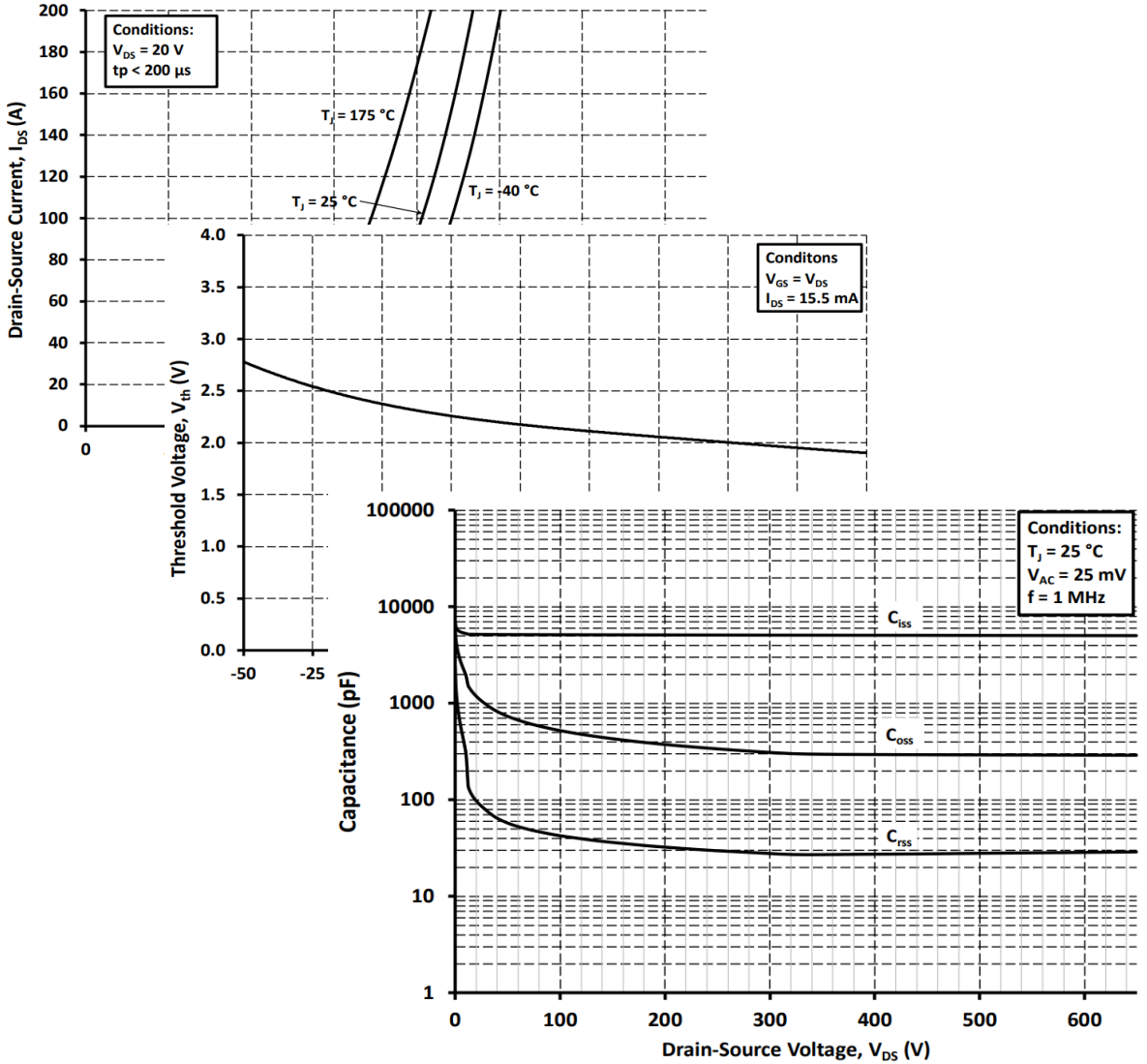

Conduction loss vs. RMS current and junction temperature.



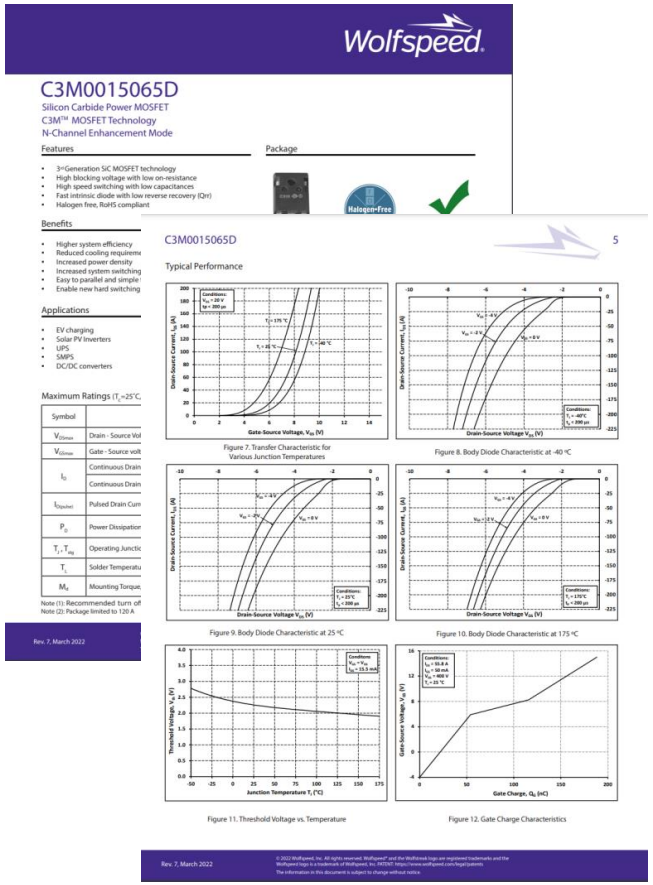
https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2021_datasheet.pdf

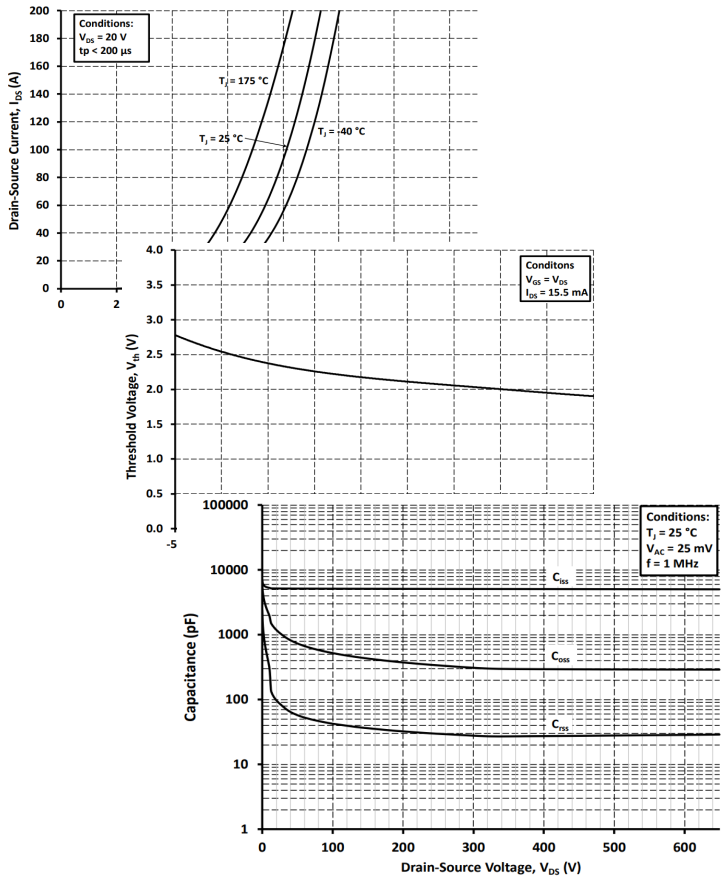
# Switching Loss



# Switching Loss




## Dynamic Parasitic Capacitance:

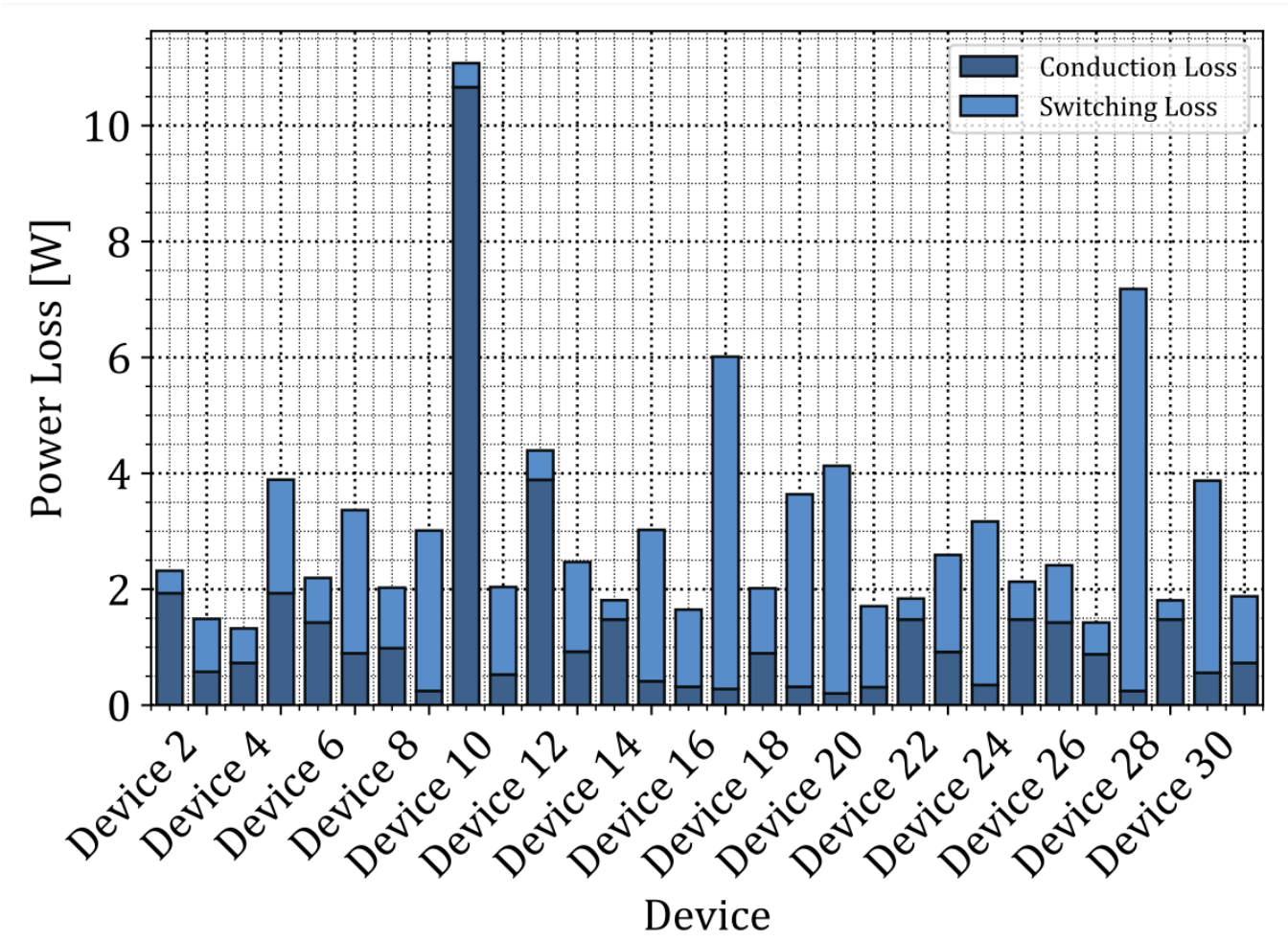
$$C_{x,eq} = \frac{1}{V_o}\int_0^{V_o} C_x(v)dv, x = iss, oss, rss$$

## Curve fitting transconductance:

$$i_{\text{ch}} = g_m\left(i_{\text{ch}}\right)\left(v_{\text{gs}} - V_{\text{th}}\right)$$

# Case study: a comparison of multiple devices

| Operating Condition (half bridge) |
| --- |
| V=50V |
| I=5A |
| f=50kHz |
| D=0.5 |



# Fast MOSFET Selection, Faster and better design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# Thanks for Listening

Fanghao Tian, KU Leuven - EnergyVille