

# Comparisons of Board-side and Back-side Thermal Management Techniques for eGAN FETs in a Half-Bridge Configuration

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## Credits

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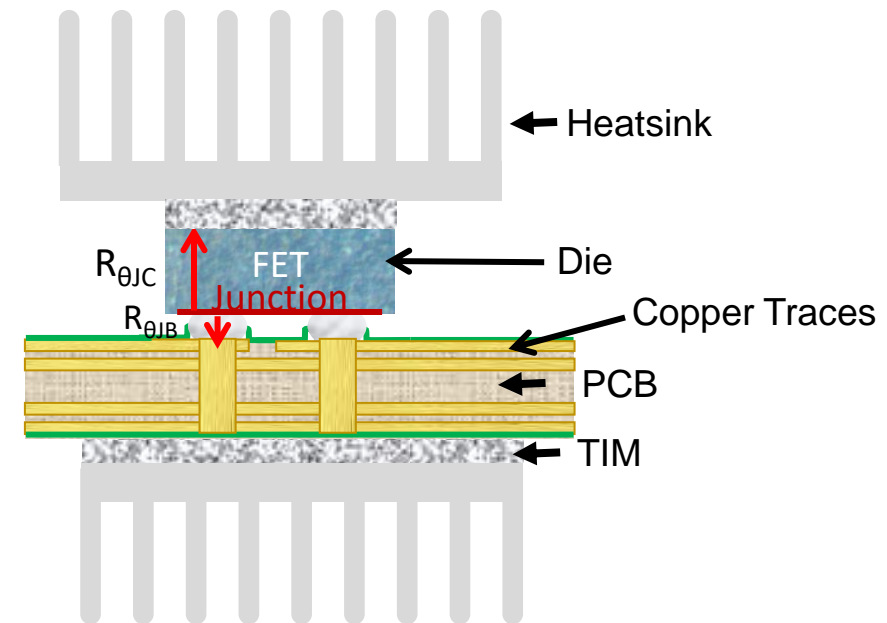
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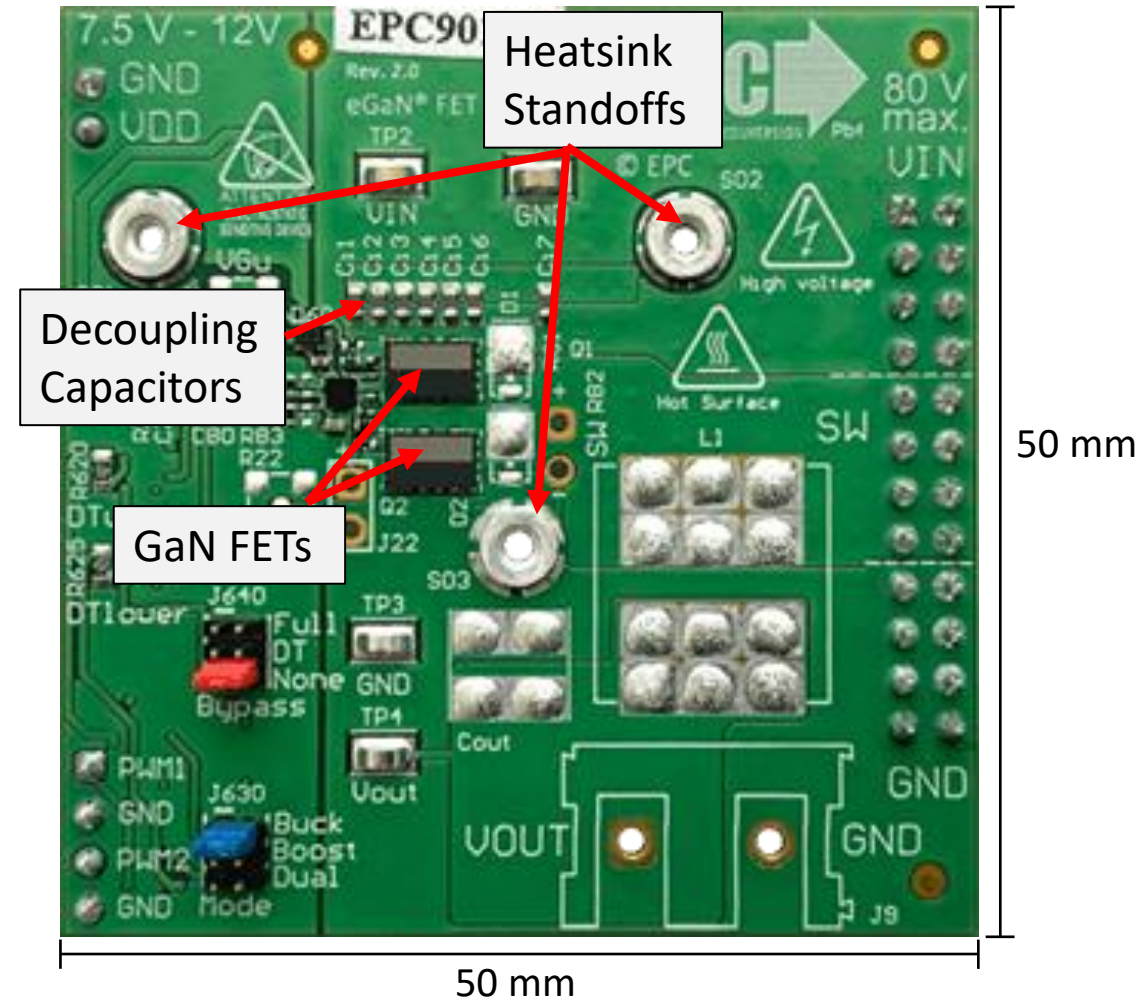
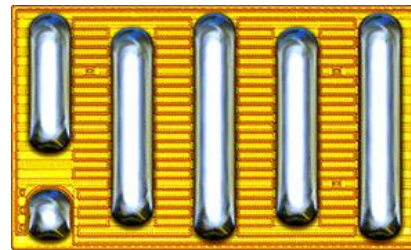
# Problem Definition

- eGaN FETs offer high power-density with ultra-fast switching and low on-resistance; improving thermals increases converter current capability
- Three cooling conditions compared:
  - PCB only cooling
  - Bottom side cooling: heatsink attached to the bottom of the PCB
  - Backside cooling: heatsink attached directly to the back of the FETs using a thermal interface material (TIM)



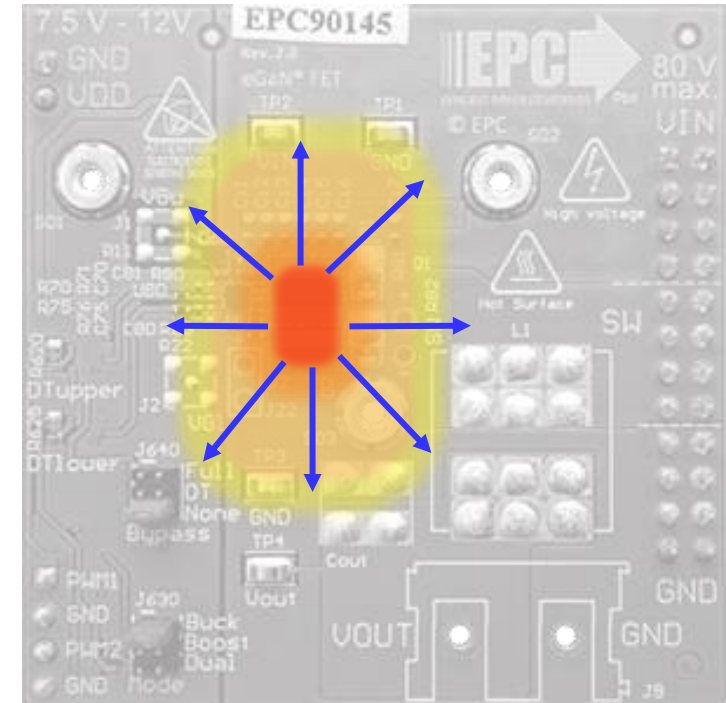
# Baseline and Analysis Overview

- 4-layer 50 mm x 50 mm PCB
- FET is EPC2619
  - 2.5 x 1.5 mm
  - $R_{\theta_{JB}} = 2.6 \text{ K/W}$
  - $R_{\theta_{JC}} = 1 \text{ K/W}$
- Simulated in CelsiusEC FEA software
- Experimentally verified



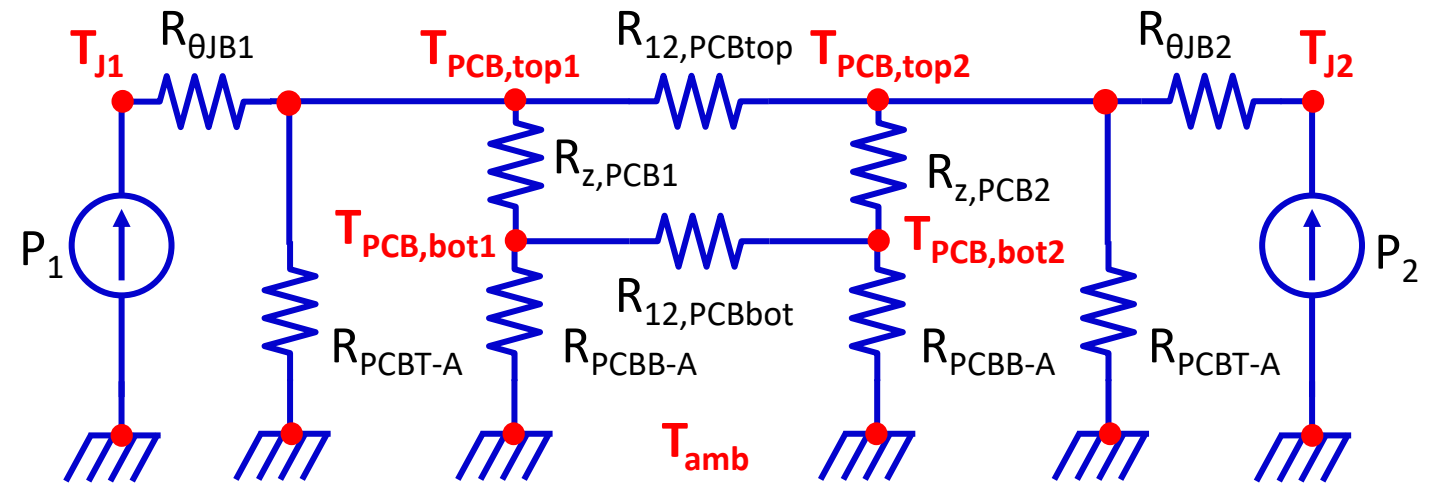
# PCB Cooling Motivation

- Determine how  $R_{\theta JA}$  can be lowered using only PCB characteristics
- Relies on heat spreading
- Suitable for low heat-flux applications



# PCB only - Thermal Resistance Network

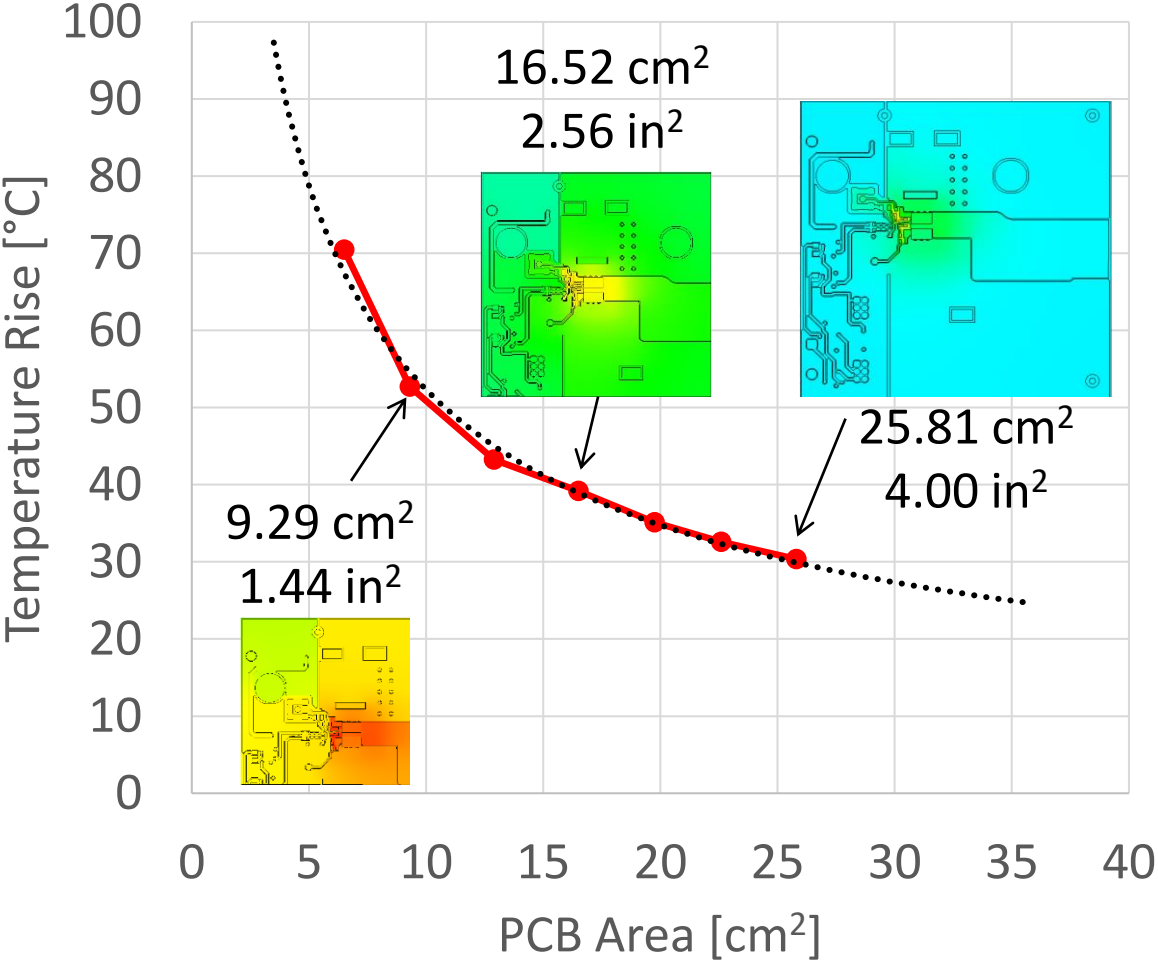
- Half-bridge configuration
- A thermal resistance network was modeled to approximate  $R_{\theta JA}$
- Includes coupled heat flux exchange



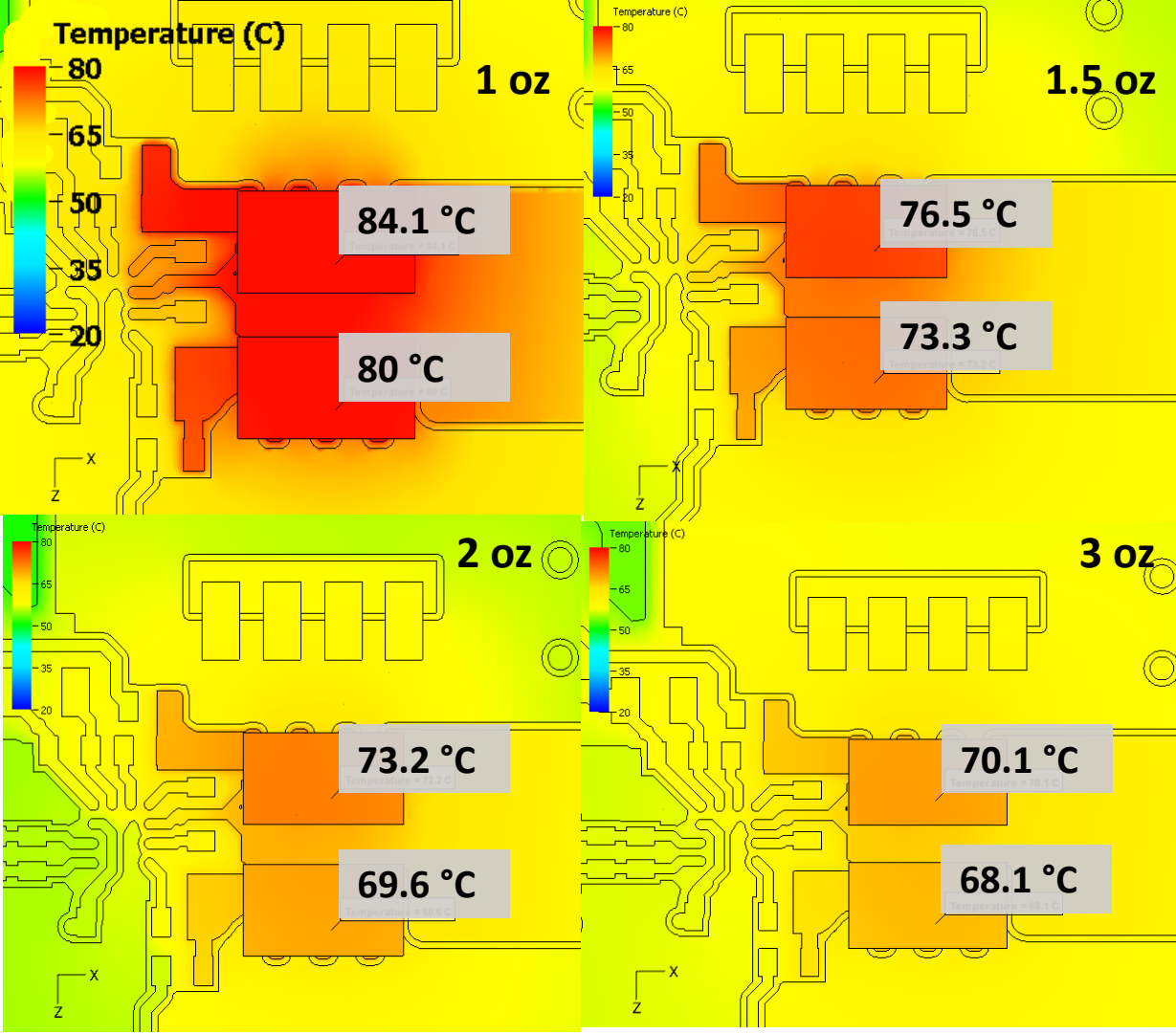
PCB-cooling thermal resistance network

# PCB Cooling Factors Evaluated

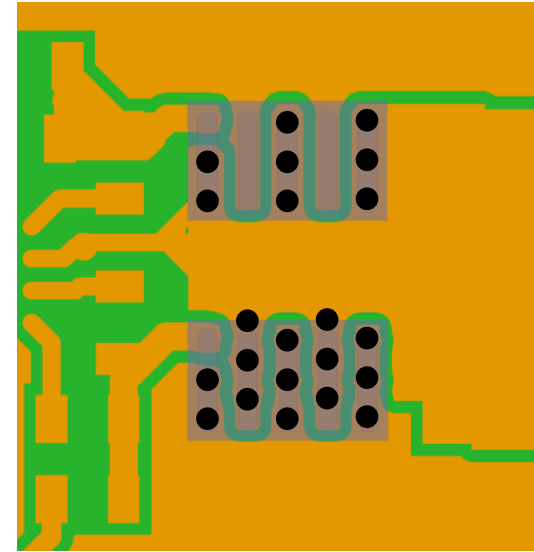
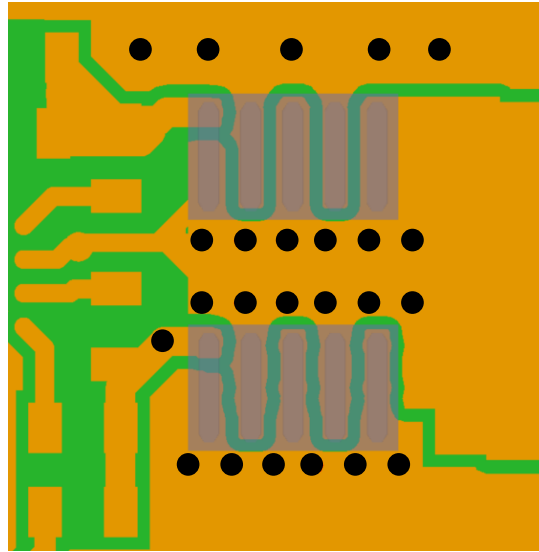
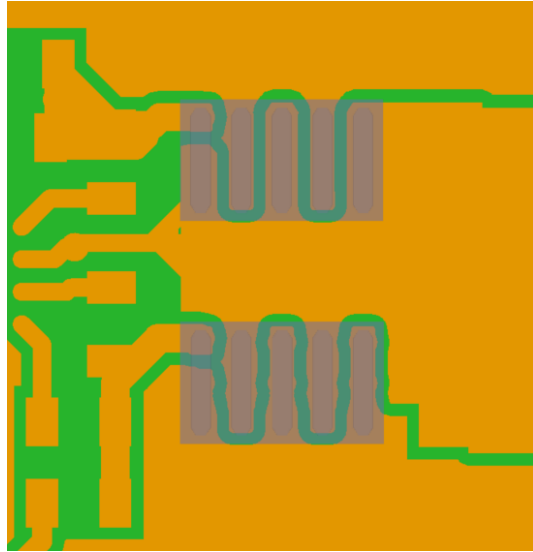
**Board Area**



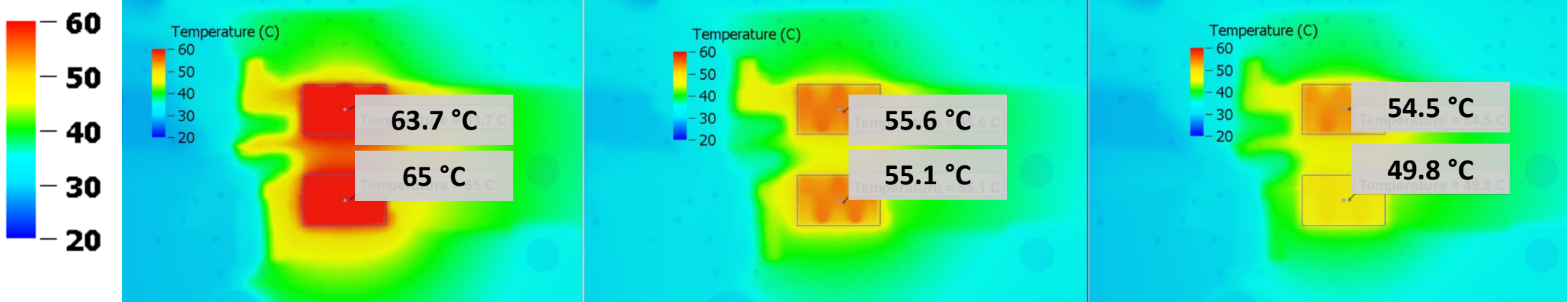
**Copper Thickness**



# PCB Cooling Factors Evaluated: Vias



Temperature (C)



$R_{\theta, JMA} = 45 \text{ K/W}$

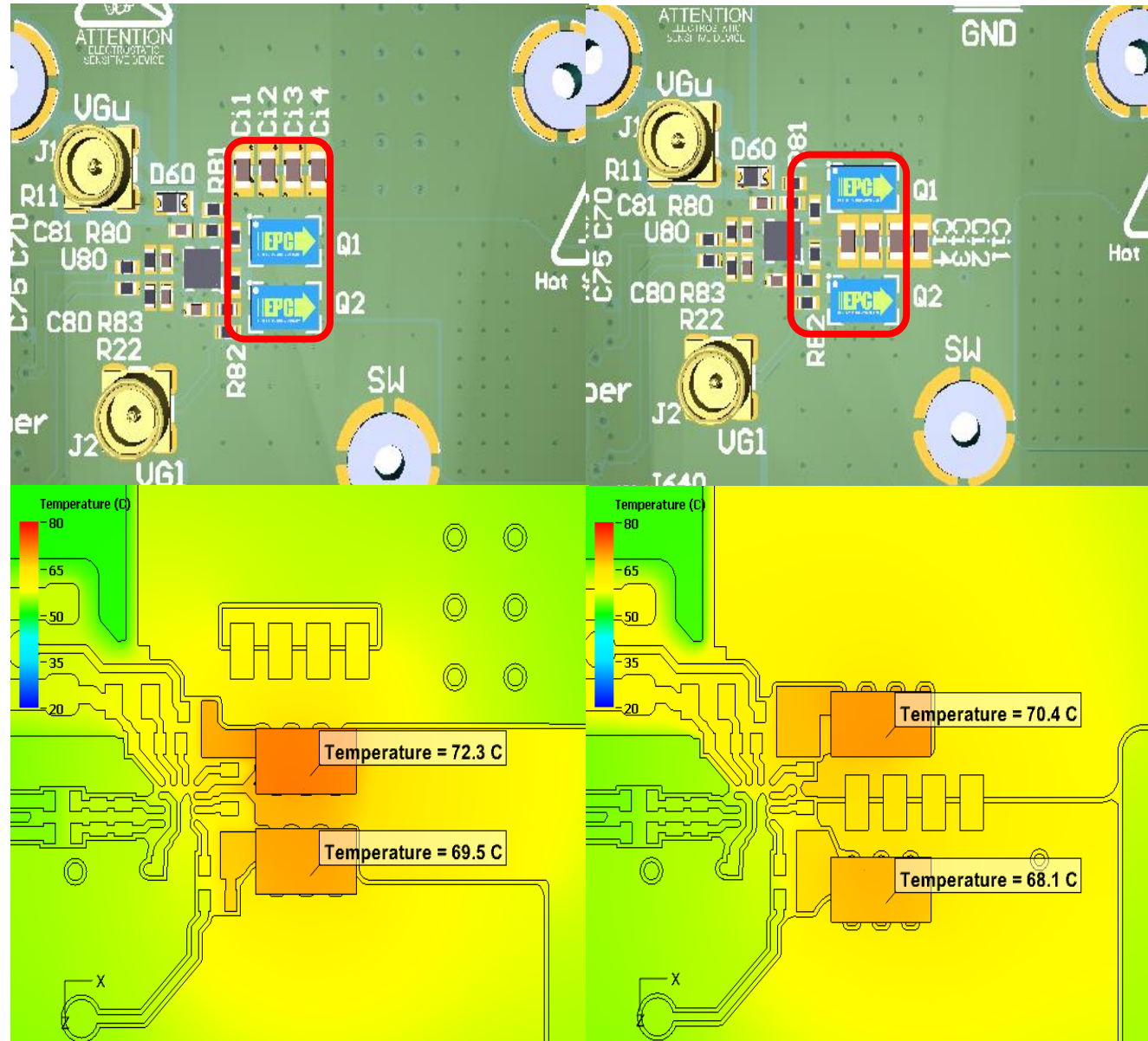
$R_{\theta, JMA} = 35 \text{ K/W}$  (22% ↓)

$R_{\theta, JMA} = 30 \text{ K/W}$  (33% ↓)



# PCB Cooling Factors Evaluated

## Device Spacing



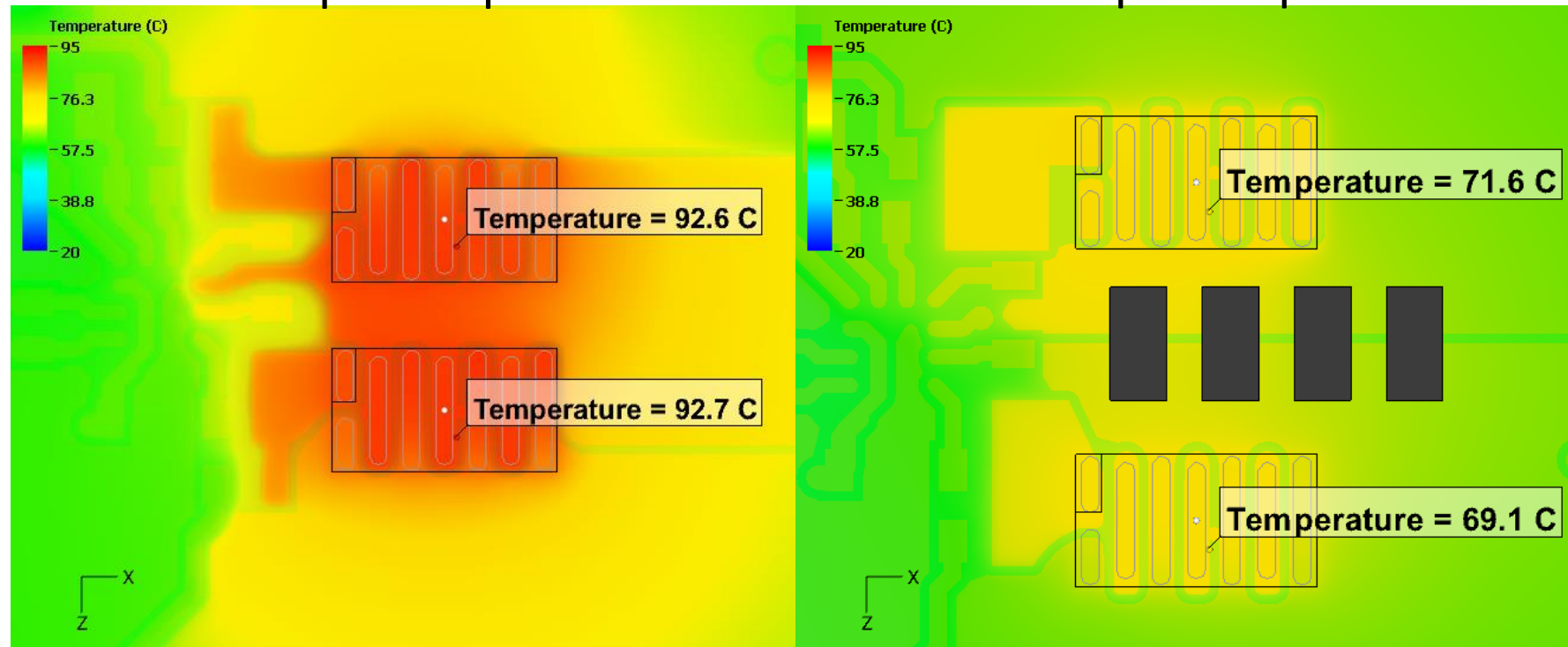
**4-5% decrease  
in  $R_{\theta JA}$**

# Combined Effectiveness

$\Delta T = 21^\circ\text{C}$ , 35% decrease in  $R_{\theta JA}$ , Natural Convection

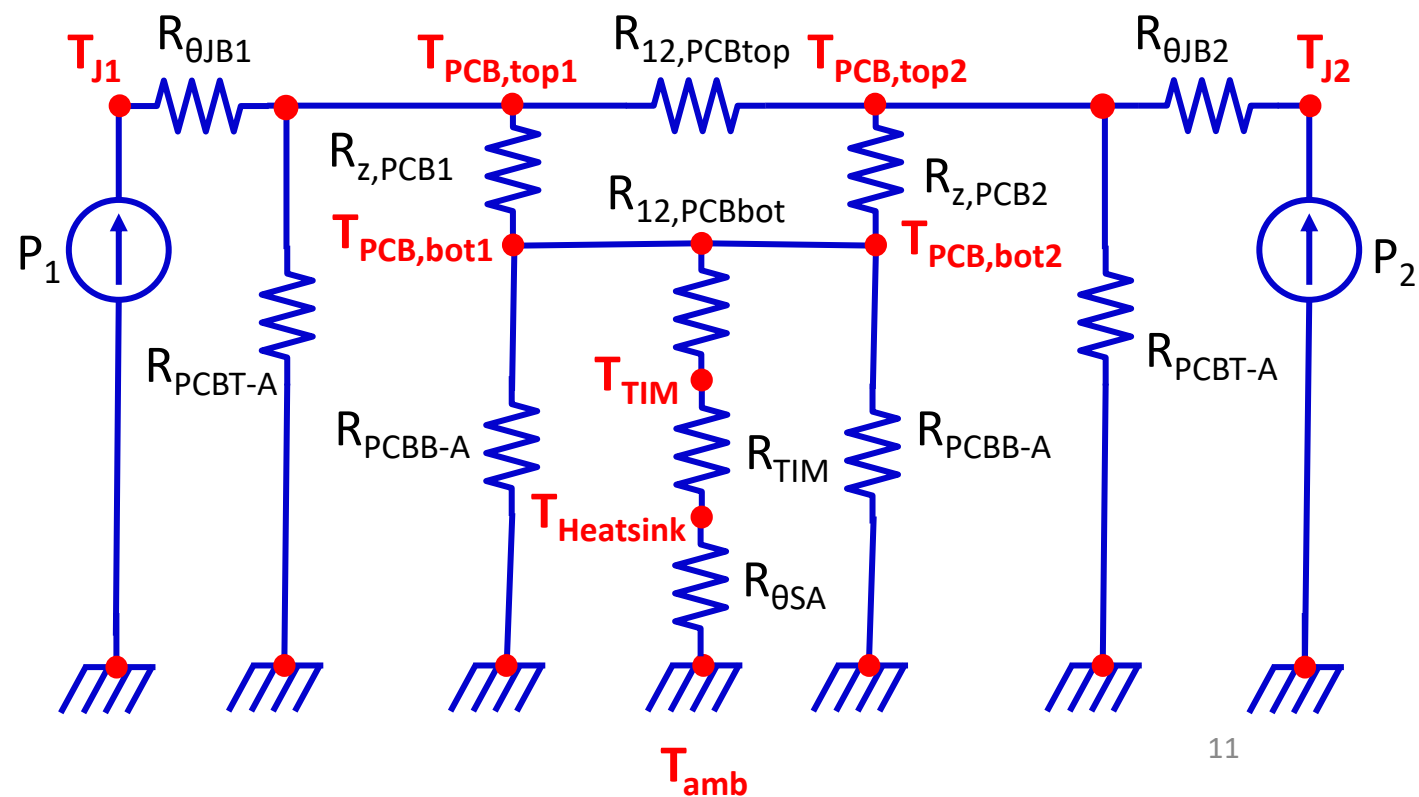
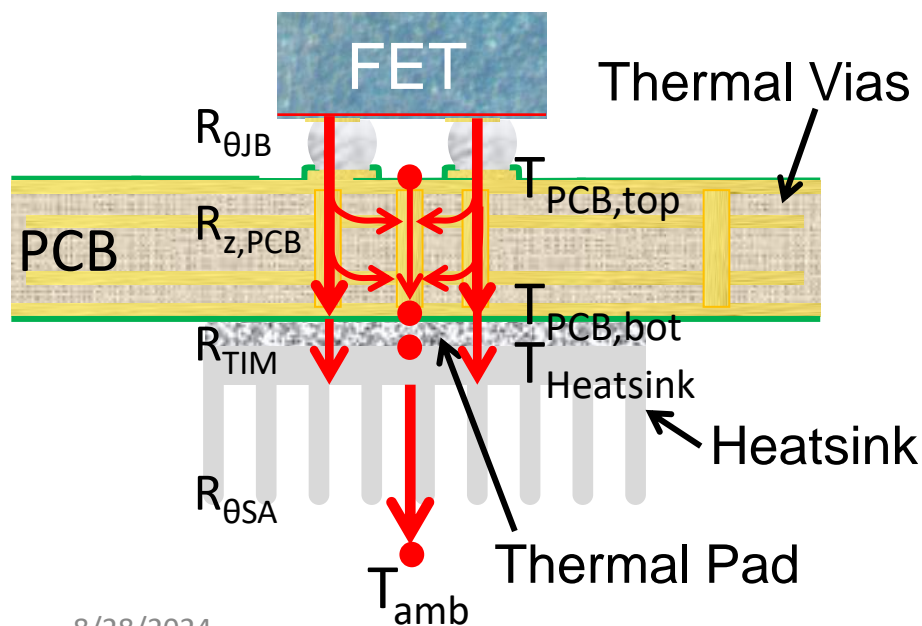
No techniques implemented

All techniques implemented



# Bottom-side Heatsink Cooling Motivation

- Increase current capability over PCB only – increased heat flux
- Simple to attach – requires no bottom side components present
- No mechanical stress on the devices



# TIM Analysis Overview

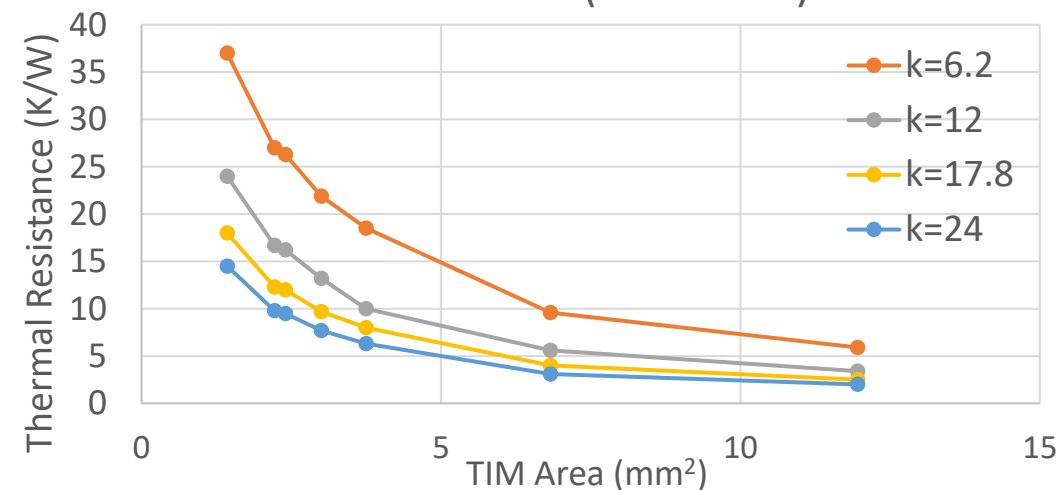
## TIM requirements

- Electrical isolation
- Low thermal contact impedance

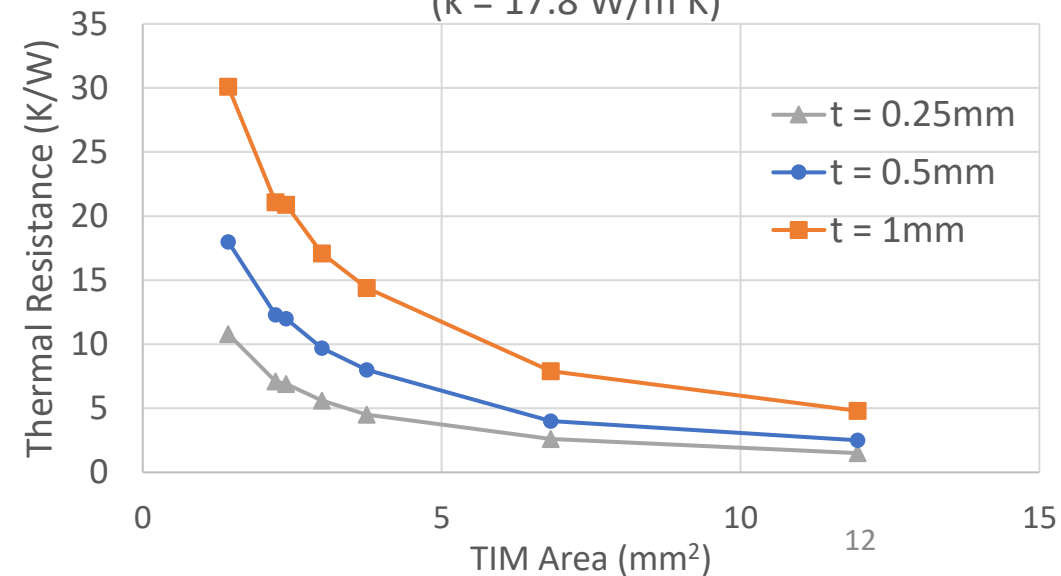
## Analysis overview

- Thermal resistance from junction to heatsink
  - Various TIM areas
  - Various TIM thicknesses
- For large bottom side PCB area, TIM thickness importance is low

Resistance with Different Thermal Conductivities (t = 0.5mm)



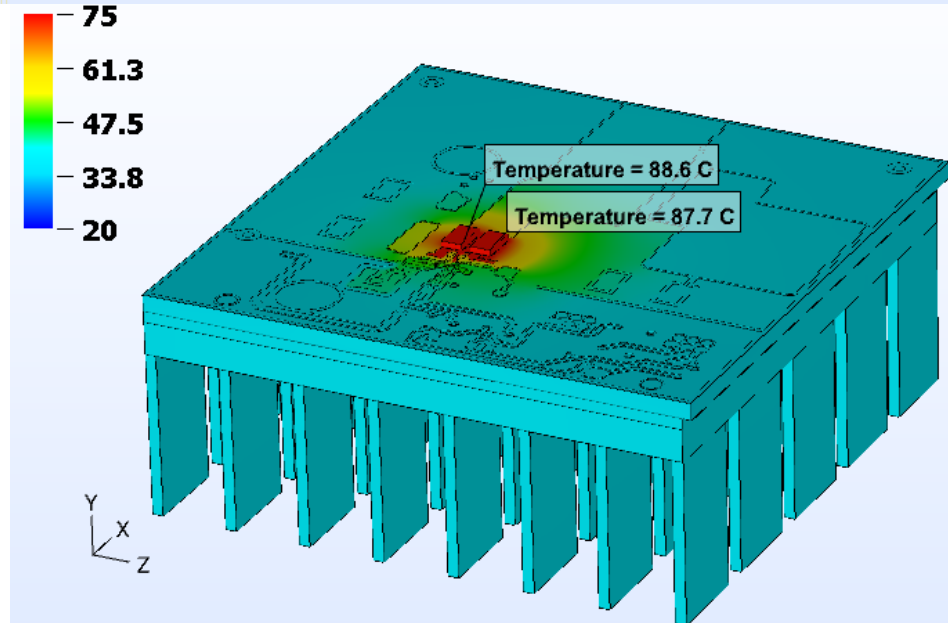
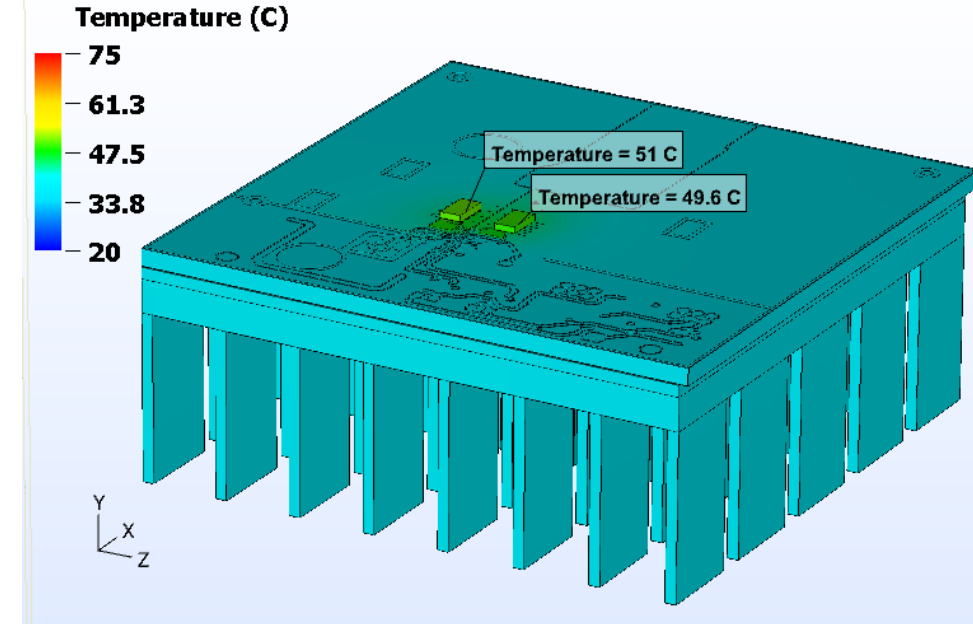
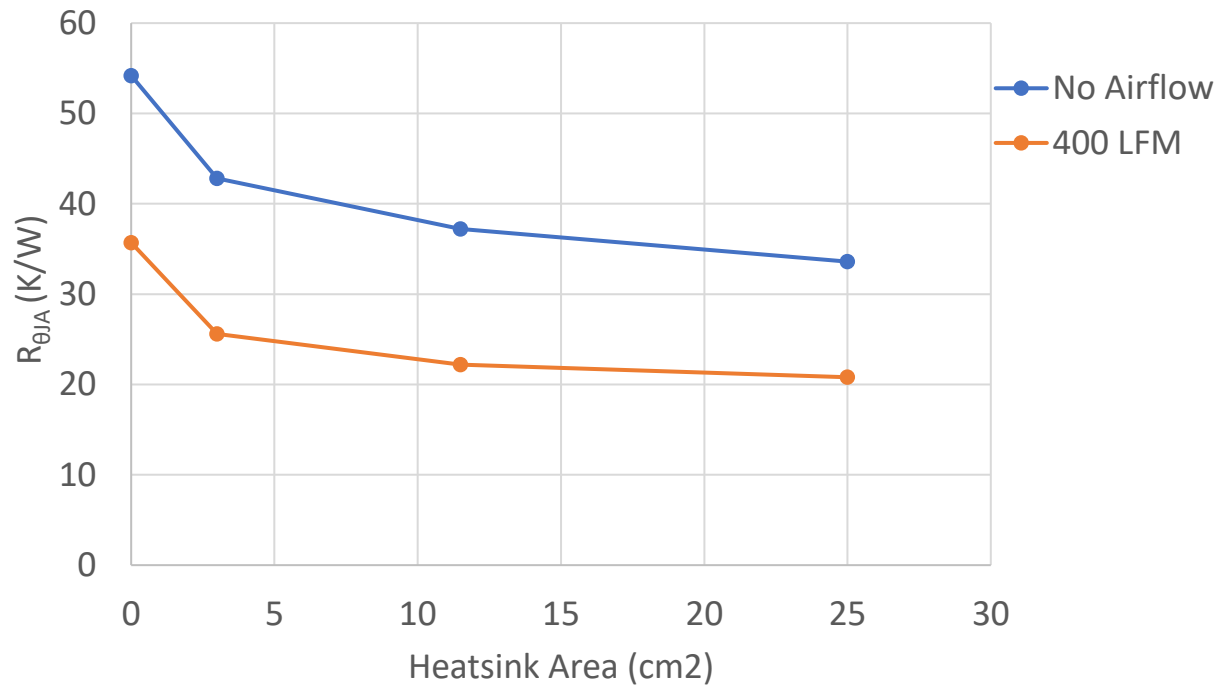
Resistance with Different TIM Thickness (k = 17.8 W/m K)



# Bottom side Simulation Results

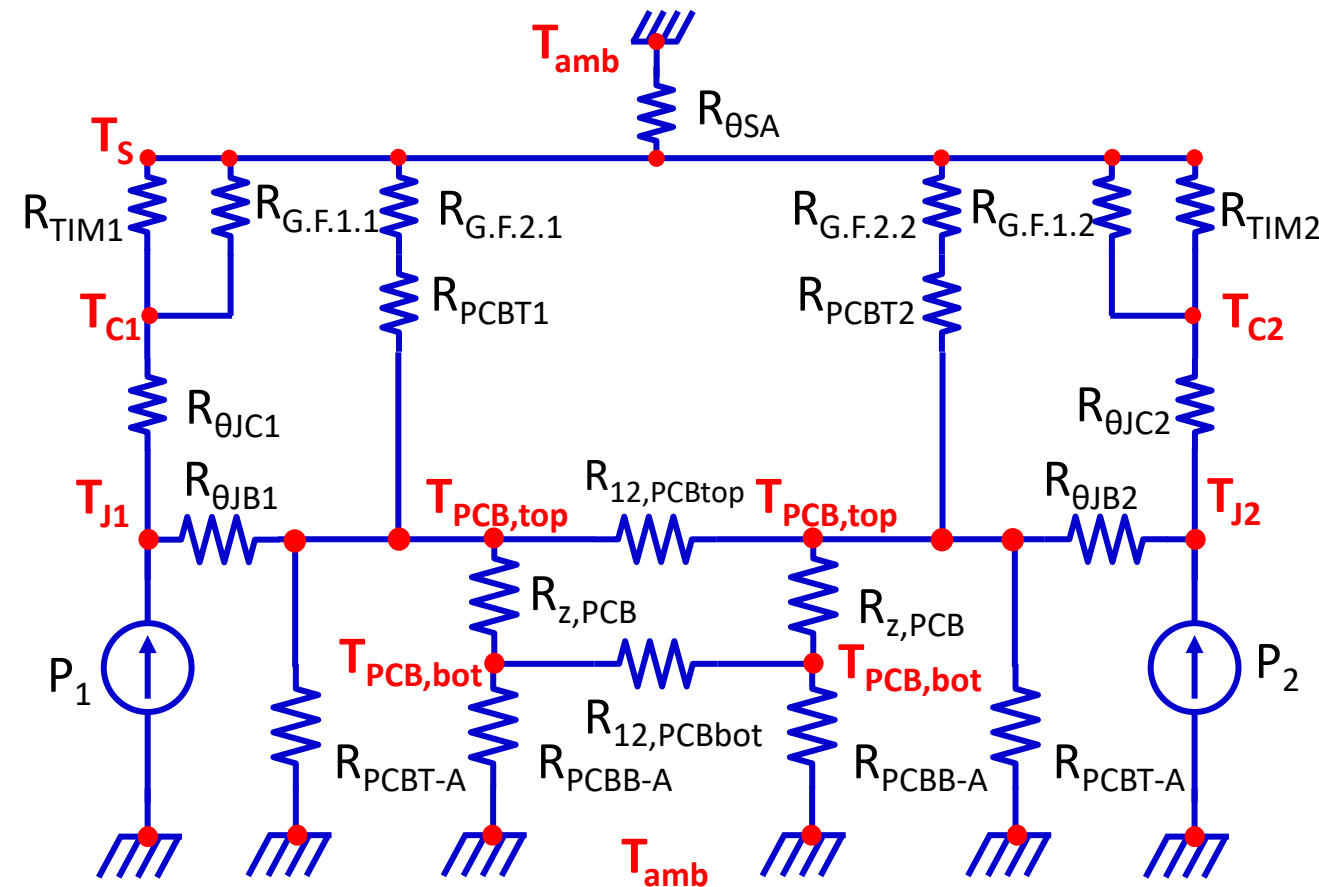
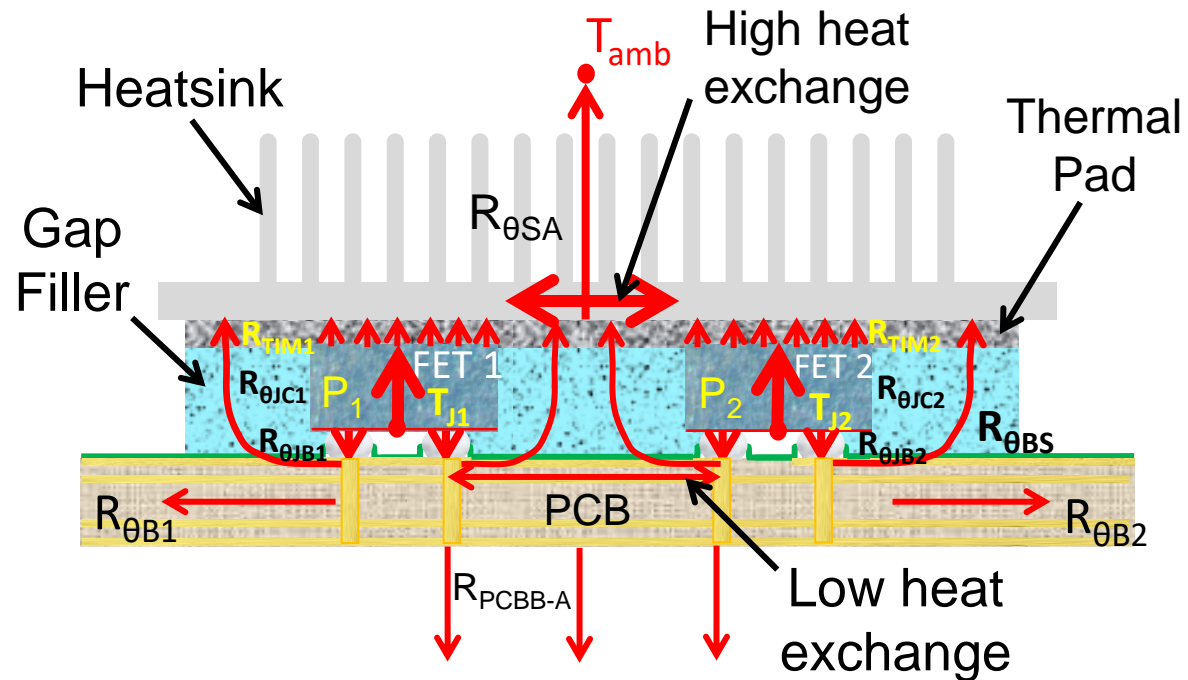
- 30-40% improvement in  $R_{\theta JA}$
- Requires all PCB-only cooling techniques

Bottom-Side Heatsink Thermal Resistances



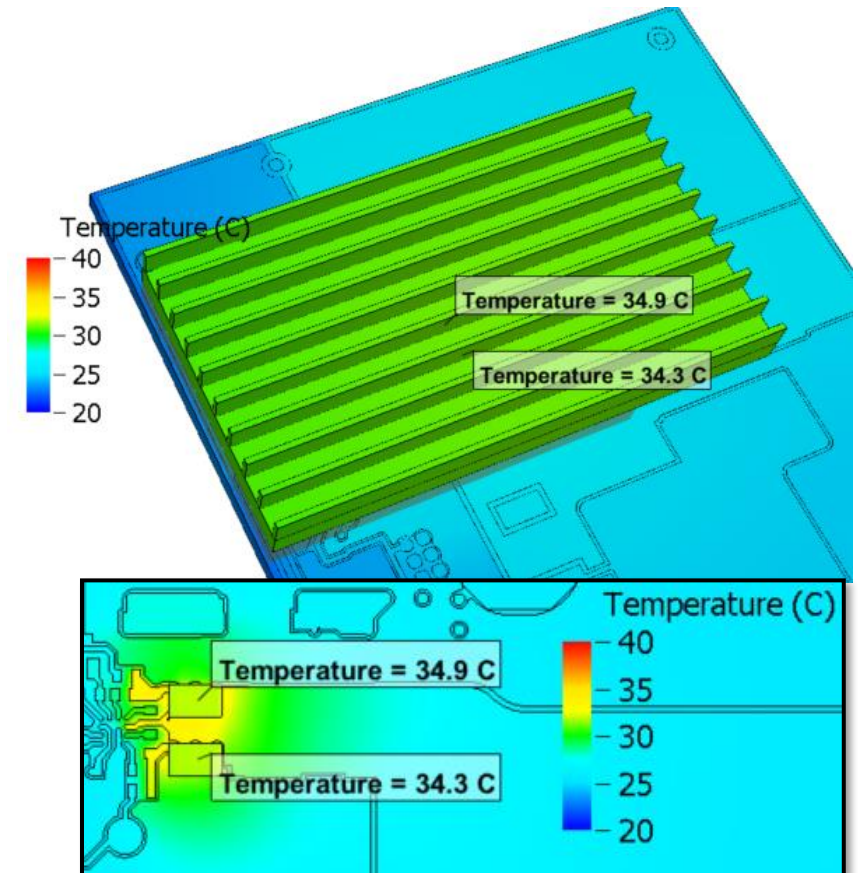
# Back-Side Cooling Motivation

- Most effective cooling path
  - Leverages the lower  $R_{\theta JC}$  value of eGaN FETs
- Higher conductivity TIMs needed
  - Device area is small



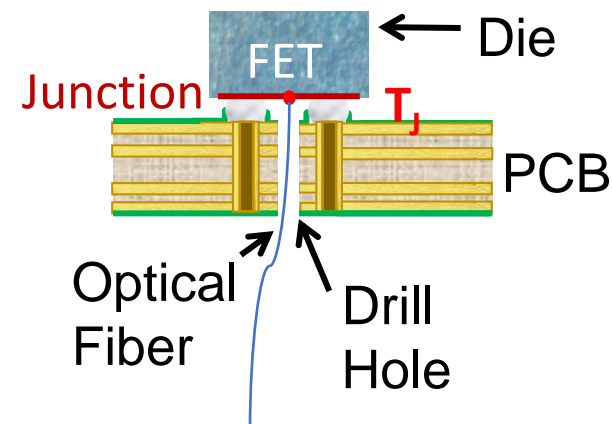
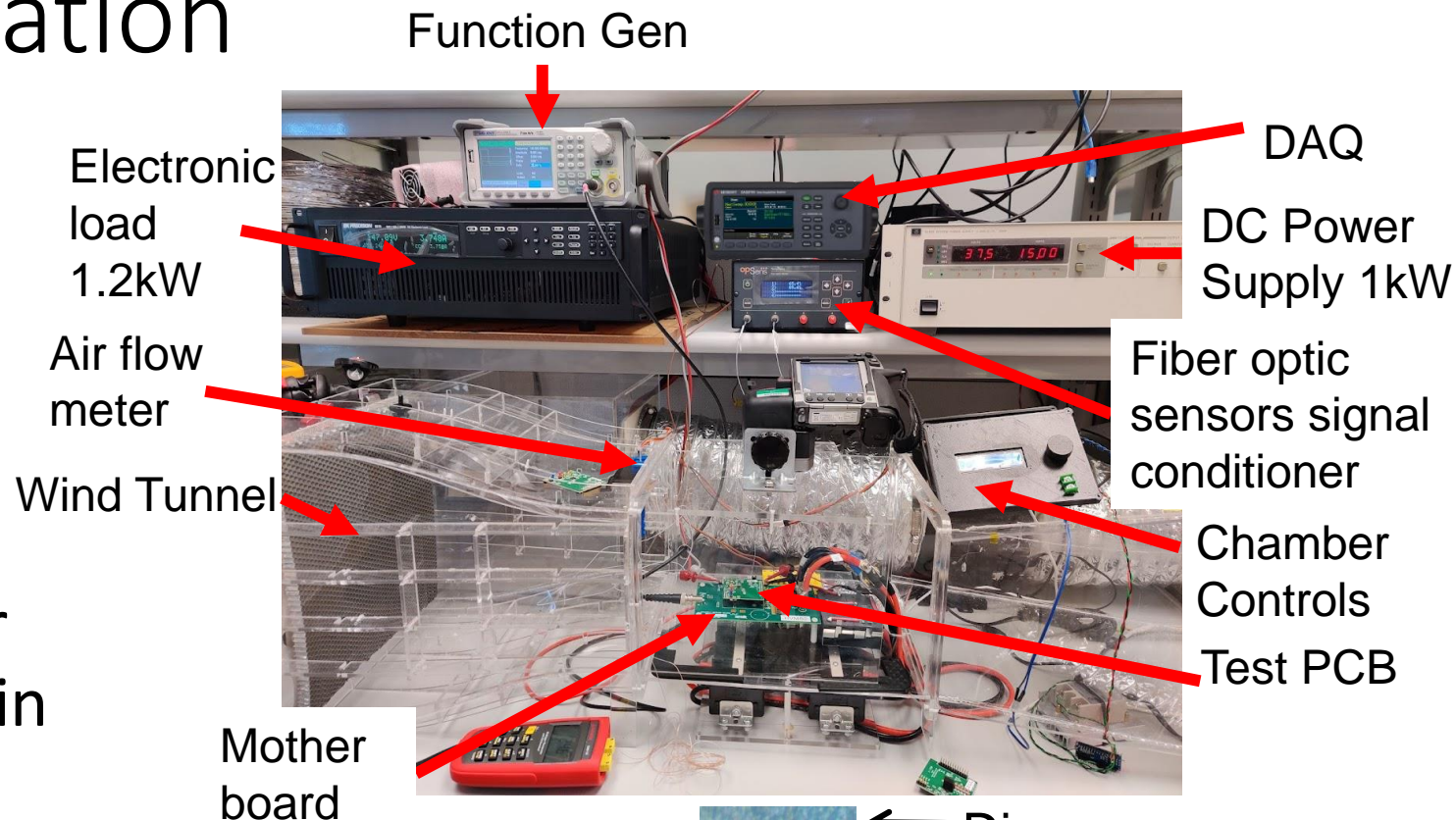
# Back-side cooling Simulation Results

- TIM of  $\kappa = 17.8 \text{ W/m}\cdot\text{K}$  and  $10 \text{ cm}^2$  aluminum heatsink
  - $R_{\theta JA} = 14.9 \text{ K/W}$
  - 32% improvement over  $12 \text{ cm}^2$  bottom-side heatsink case
- Can be further improved with a thinner TIM or more optimized heatsink
  - $R_{\theta JA}$  can be  $< 10 \text{ K/W}$  with TIM  $< 1 \text{ mm}$  thick



# Experimental Validation

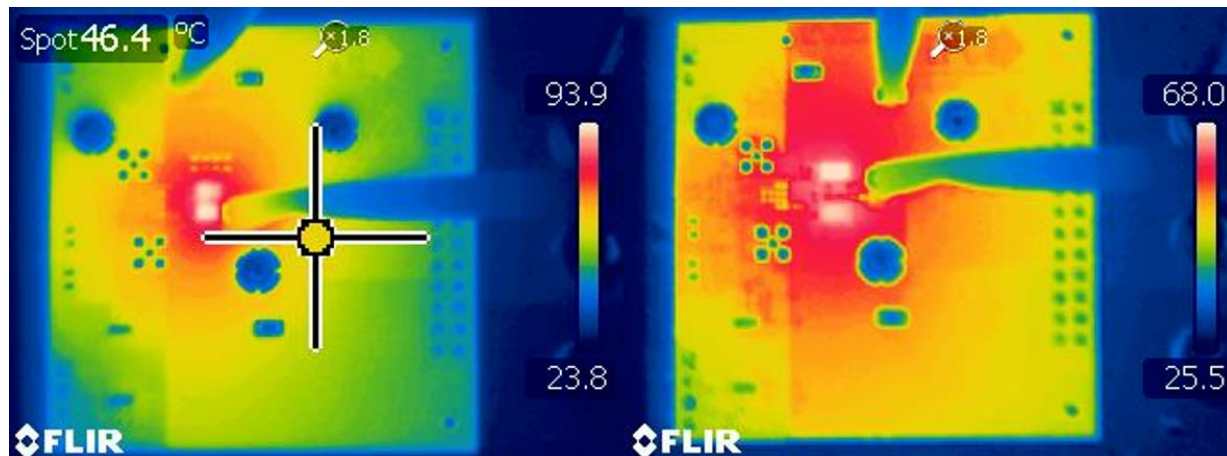
- PCB-only and Back-side heatsink configurations
- Two EPC2619 on a test board mounted to motherboard; connected as shown in image
- OpSense<sup>®</sup> OTG-F sensor used for temperature measurement within 0.1°C
- Placed in a wind tunnel to control airflow





# Experimental Validation Results

PCB-only Cooling



0.5 oz Cu, minimal vias, adjacent FETs

2 oz Cu, vias under the FETs, separated FETs

- PCB-only cooling cases show a close match with the simulated results

Backside Cooling

Airflow	Sim. $R_{\theta JA}$ [K/W]	Exp. $R_{\theta JA}$ [K/W]
200 LFM	18.8	21.06
400 LFM	14.9	17.2
600 LFM	14.6	15.92

- Around ~10% error
- Simulation underestimates  $R_{\theta JA}$

# Conclusions

For GaN FETs:

- PCB cooling techniques such as vias in pad and thicker copper can double current carrying capability
- Bottom-side cooling about 30% more effective than PCB-only cooling
  - Uses a large area TIM
  - Requires implementation of all PCB-cooling techniques
- Back-side cooling solution is the most effective for reducing  $R_{\theta JA}$ 
  - $R_{\theta JC}$  is the most direct heat path
  - 30% improvement over bottom-side cooling
  - Must manage mechanical stress

**Thank you for your time. Any questions?**