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A 150 & 200mm engineered substrate increasing SiC power device current density up to 30%

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AGENDA

1. Introduction to SiC engineered semiconductor substrate technology
2. SiC engineered substrate characterization
3. Lifecycle analysis and process simplification
4. Device results
5. Takeaways and next steps

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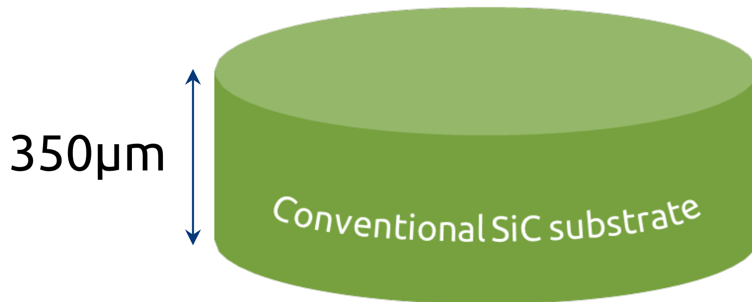
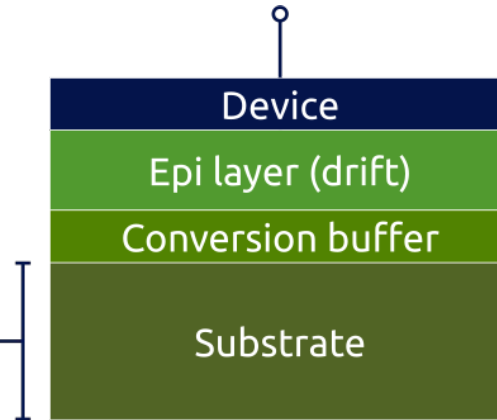
SiC Engineered Substrate: optimum design for Performance & Value

Current Industry Solution (single crystal bulk SiC)



SiC Device Structure

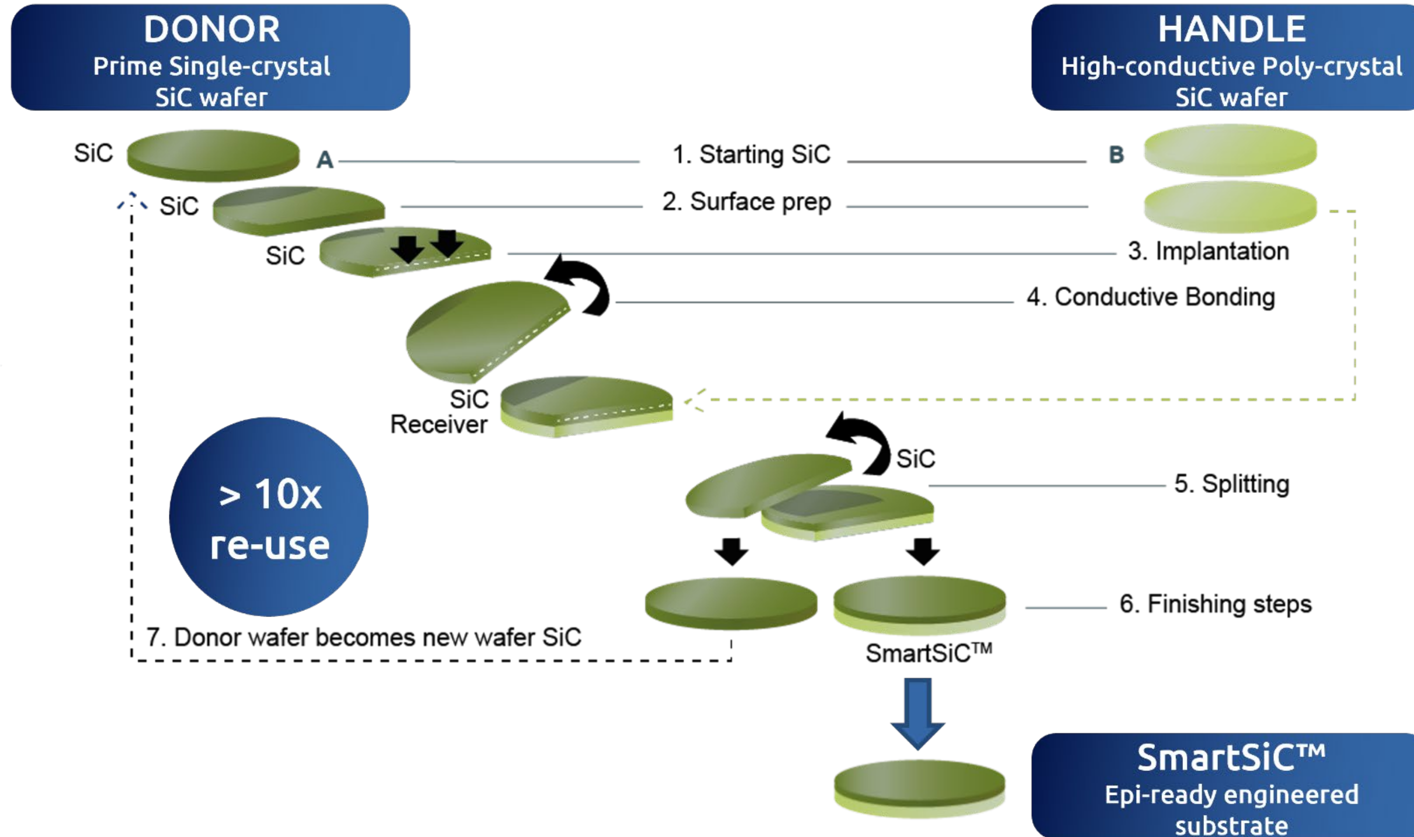


SiC engineered substrate

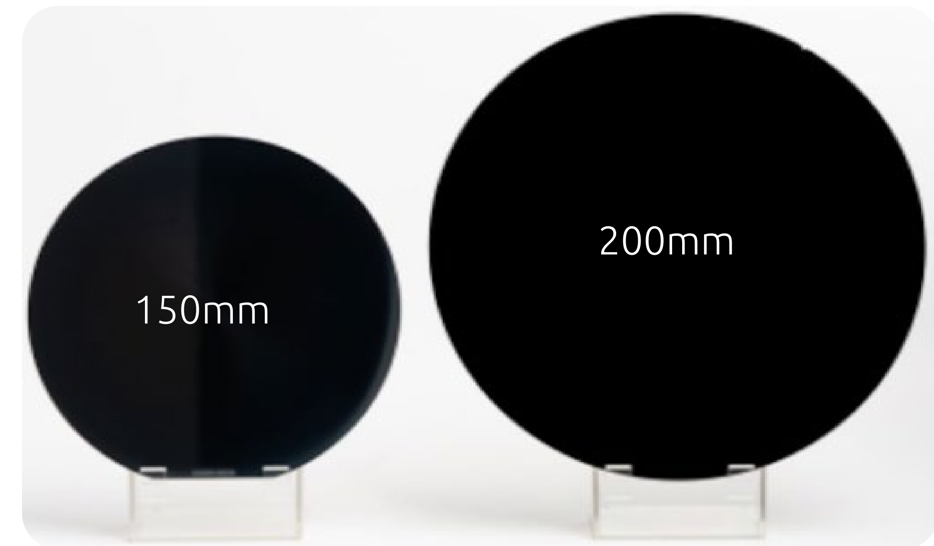
A unique value proposition

- **Smaller size / Higher current** density
- **Higher** manufacturing **yield**
- **Simpler & cheaper** manufacturing **process**
- Improved **Power Cycling** robustness
- **Bipolar Degradation** ruggedness
- **Fastest path to 200mm** transition

SmartSiC™: Smart Cut™ Process Adapted to SiC



HVM 150mm & 200mm



Leveraging Soitec's 30-year High Volume Manufacturing Expertise

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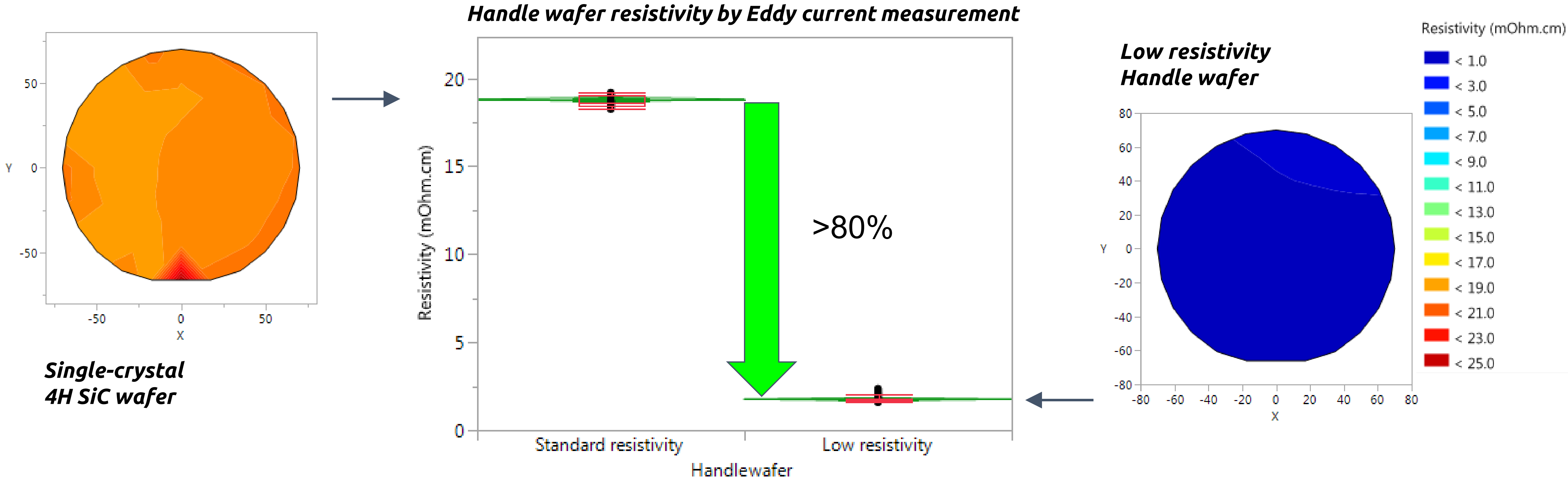
Polycrystalline SiC: electrical transport properties



Substrate resistivity decreased by one order of magnitude

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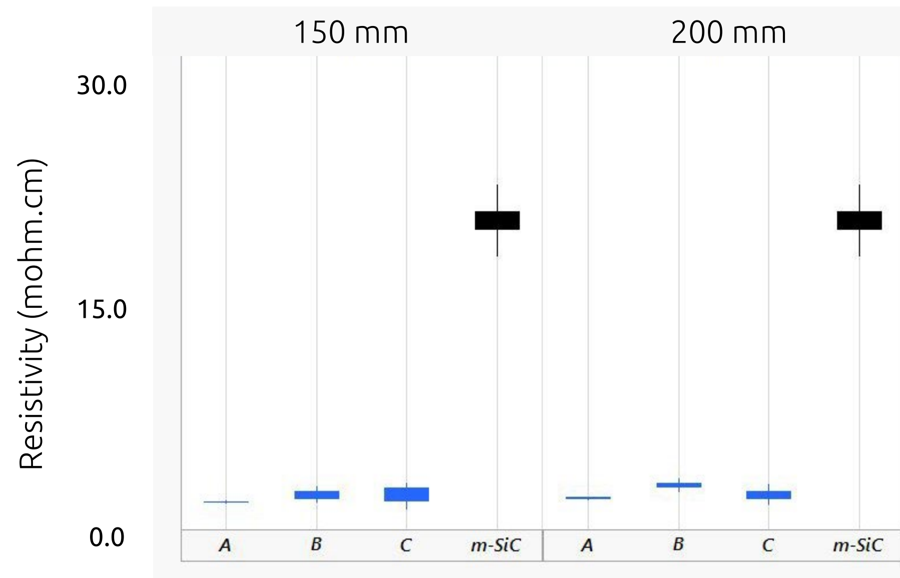
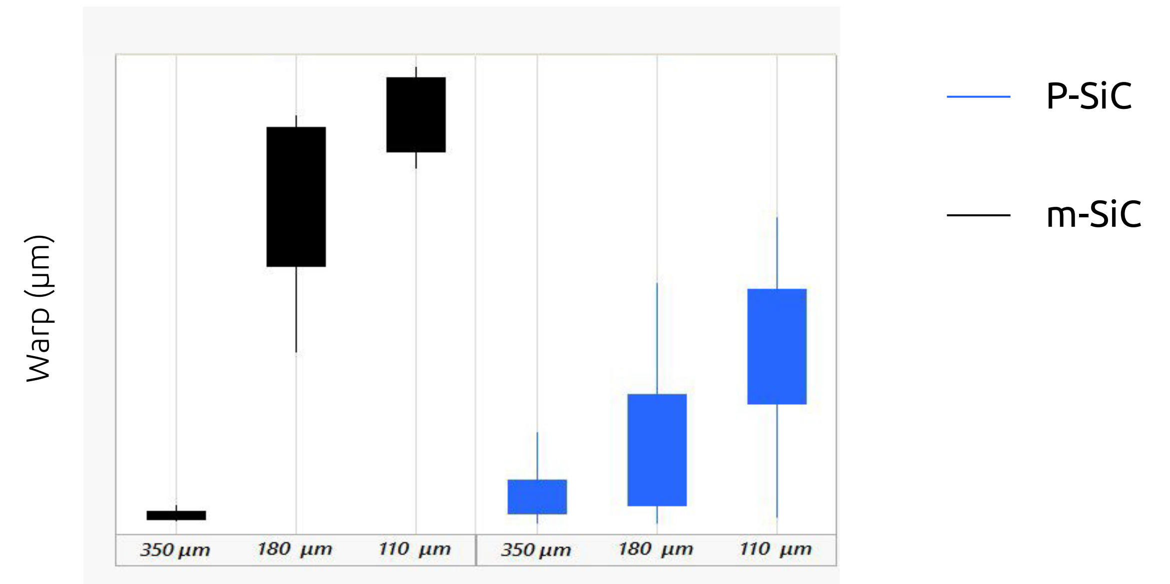
Polycrystalline SiC: scalable and stable supply chain

ELECTRICAL RESISTIVITY BY SUPPLIER AND WAFER SIZE



WAFER SHAPE VS THICKNESS



- Tight control of electrical resistivity and wafer shape
- Easy scalability from 150 & 200 mm wafers size (cost, performance, volume)

Currently in mass production for EV market

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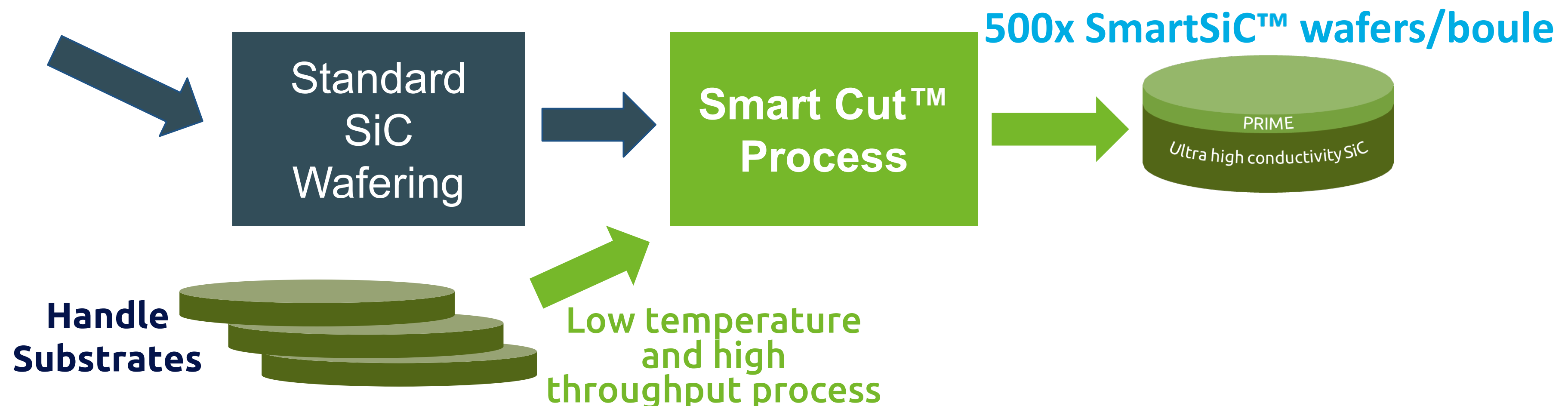
SiC engineered substrate: optimum reuse of energy intensive mSiC

Standard SiC wafer manufacturing approach

SmartSiC™ wafer manufacturing approach



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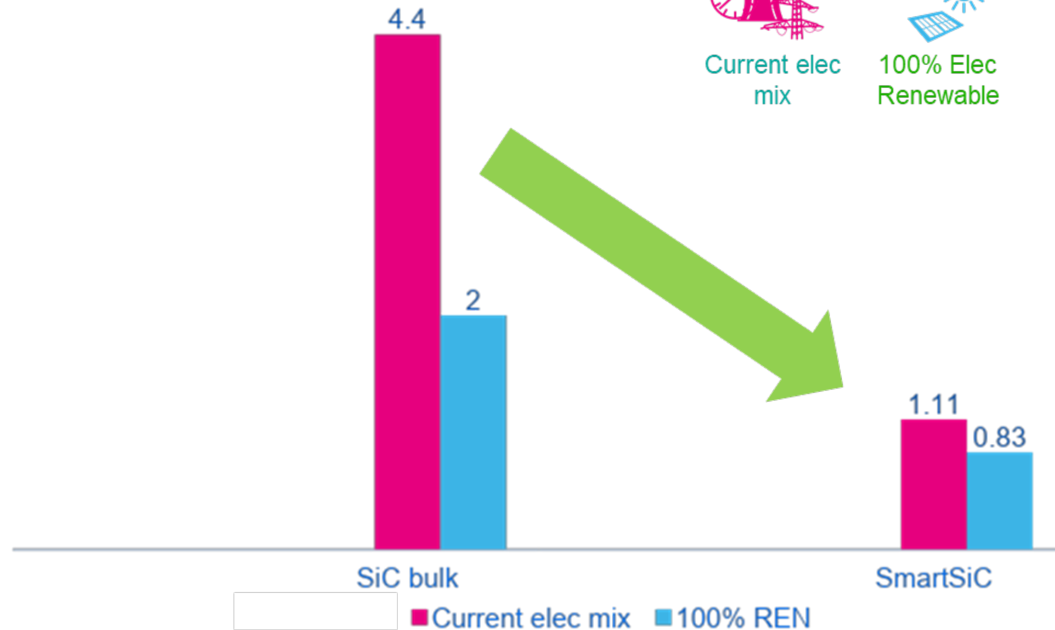
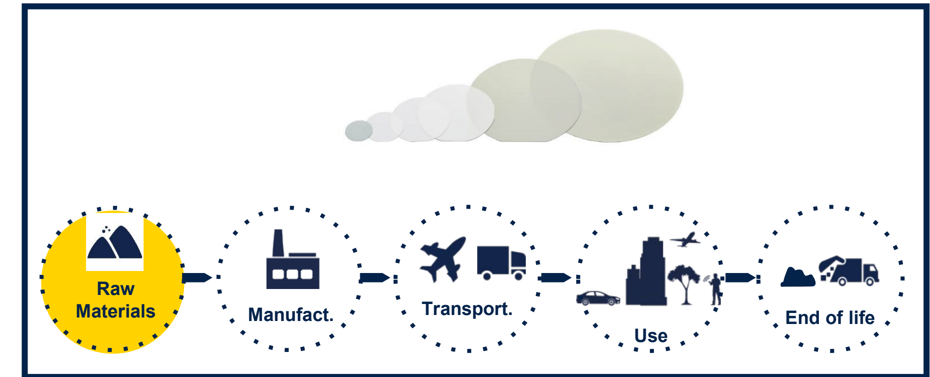
SiC engineered substrate: reduced CO_2 footprint SiC



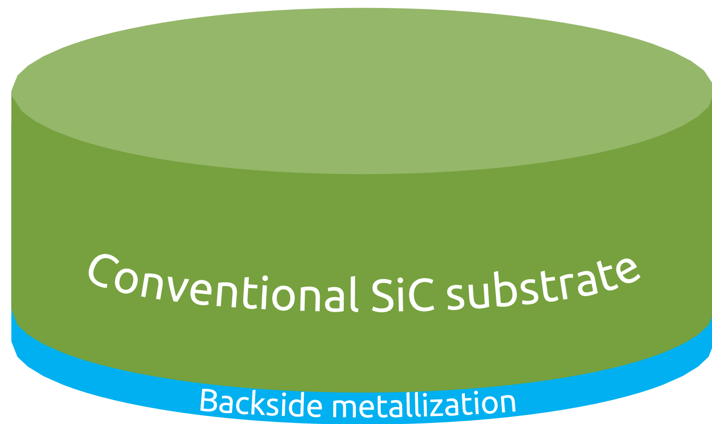


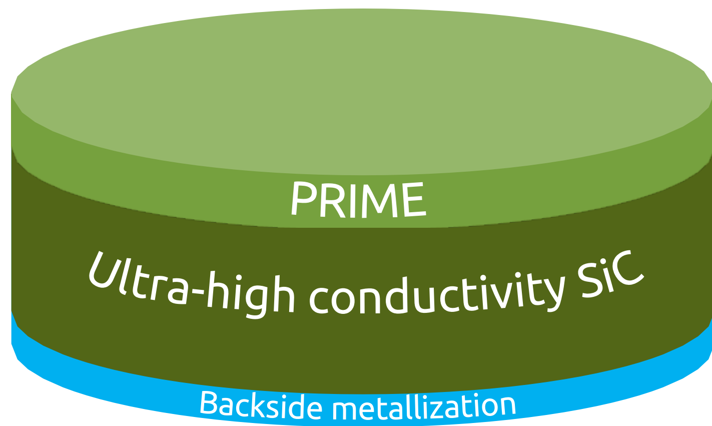
Source of data:

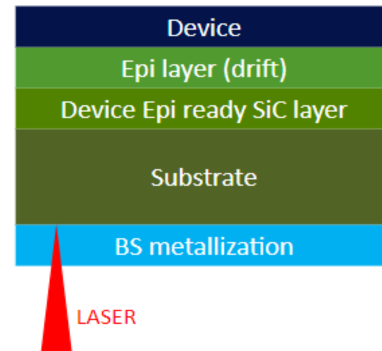
- Carbon emissions for wafers production following a life cycle analysis protocol
- Normalized results per mm² based on current and future electrical mix, and manufacturing data

Divide by 4 the CO_2 emissions to manufacture SiC wafers

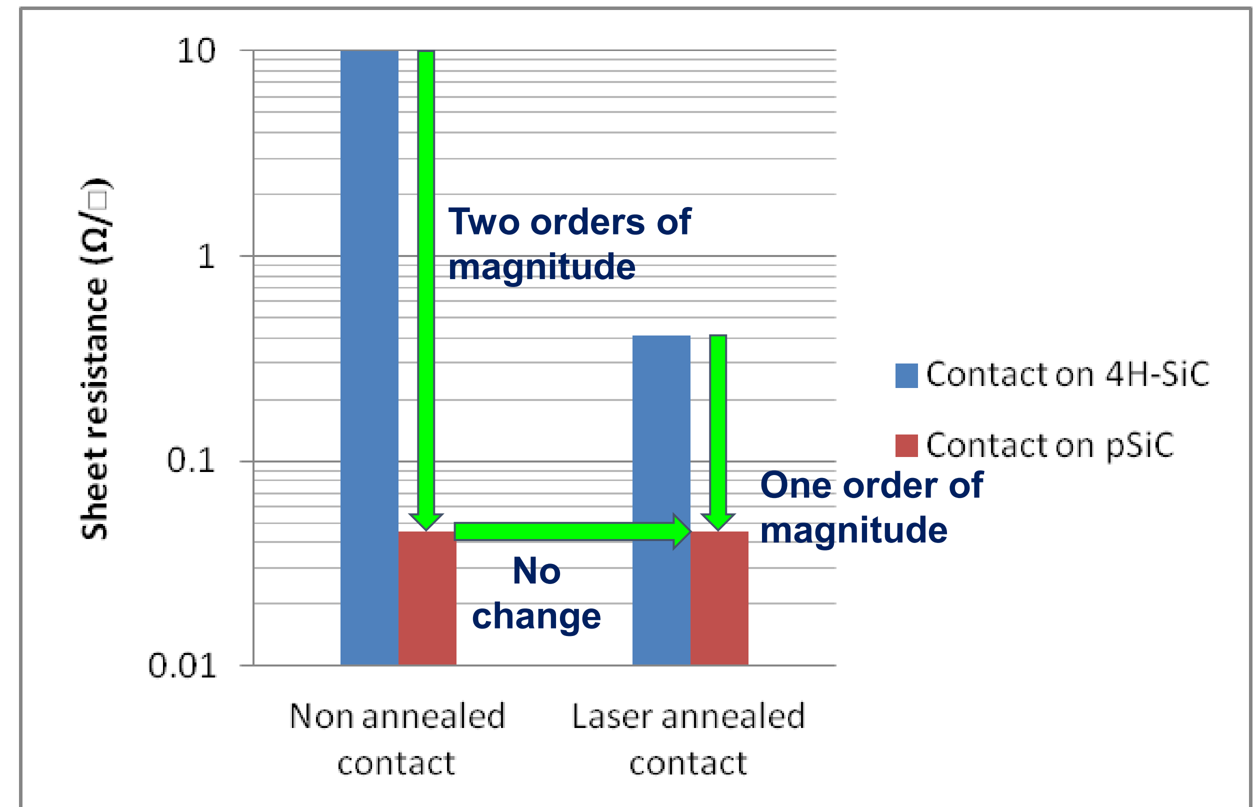
SiC engineered substrate: No Need for Backside Laser Annealing





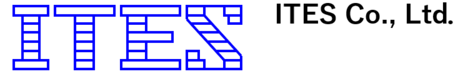


Ohmic contact without backside laser annealing



Higher Yield / Less CAPEX & OPEX

BPD stressing through UV illumination



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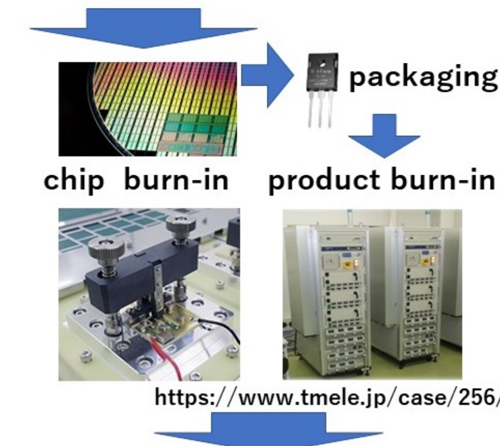
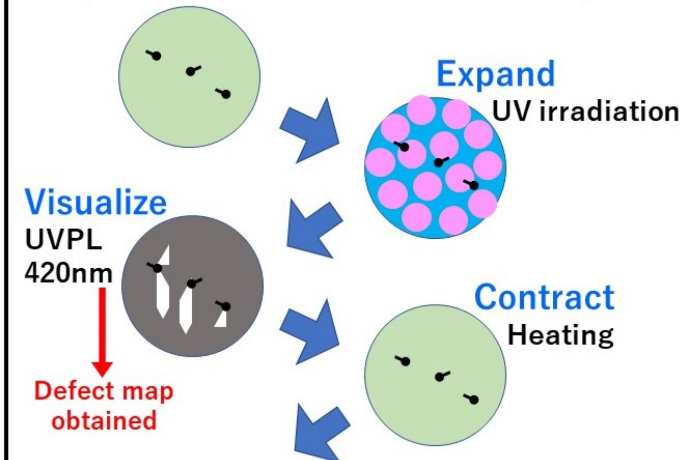
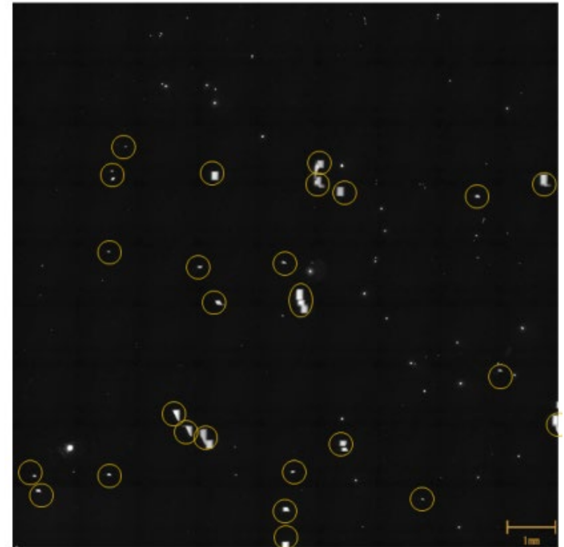
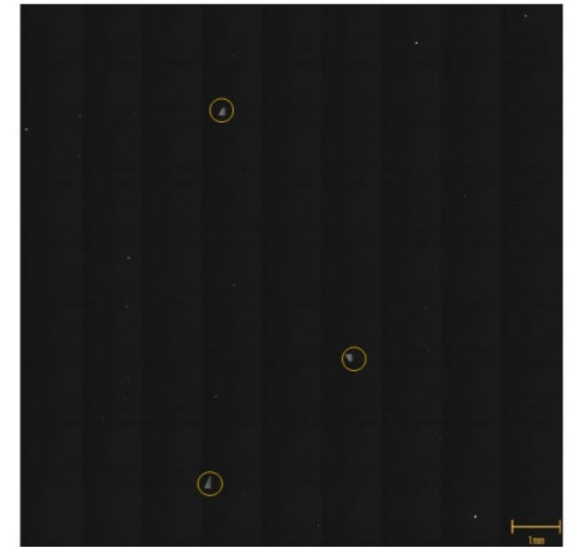






bulk SiC+10µm drift epi



SmartSiC™+10µm drift epi

SiC engineered substrates are intrinsically robust against bipolar degradation

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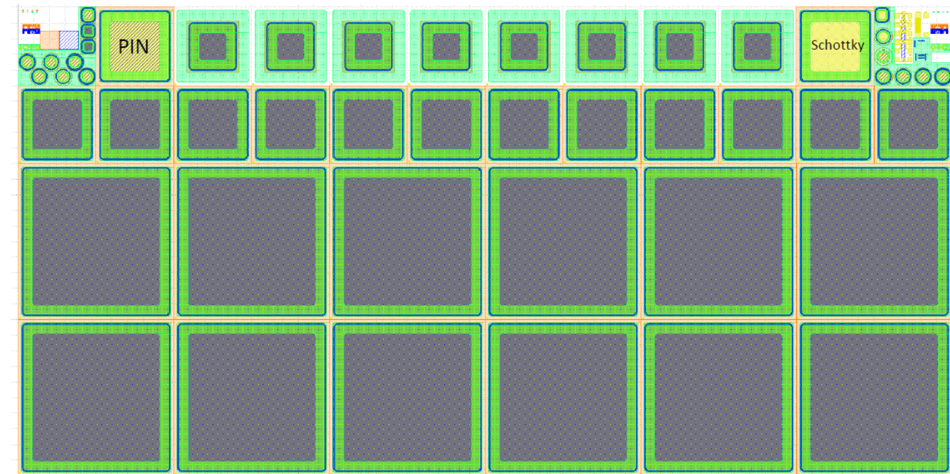
Design and experimental conditions of SiC diodes

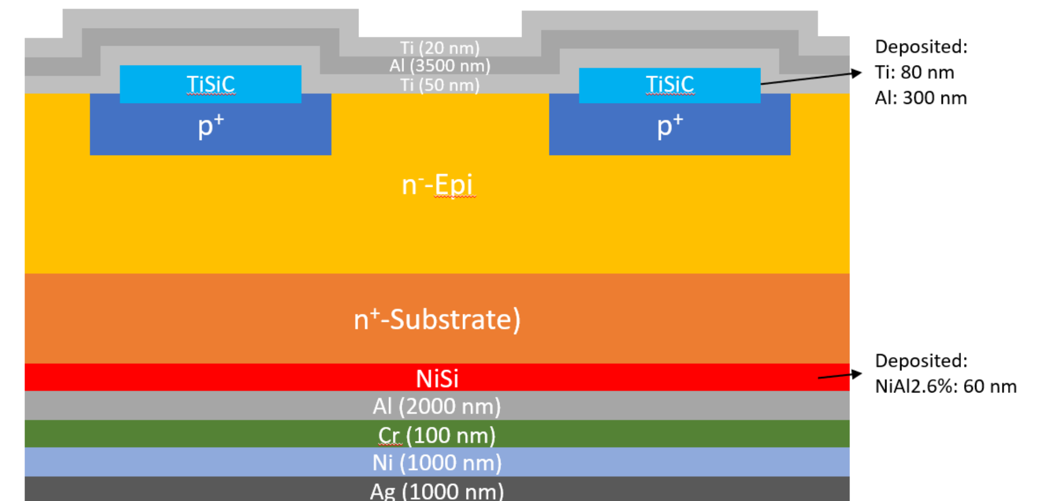
Multi project diode mask:

- JBS: 340x340µm ➔ 0.2 Amp
- PIN: 1.6x1.6mm
- MPS: 1.6x1.6mm ➔ 4 Amp
- MPS: 2.5x2.5mm ➔ 9 Amp

Process details:

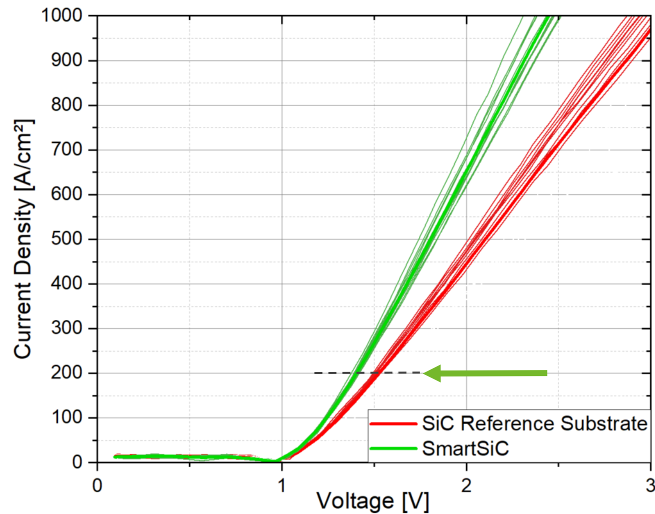
- Drift layer epitaxy done with Aixtron G5 reactor
  - Drift thickness: 11µm
  - Drift doping: $1e^{16}.cm^{-3}$
- P+ implanted regions:
  - Depth: 500 nm
  - Width: 2.5 µm
- Die thickness: 340µm (10µm grinding)
- Back side ohmic contact:
  - Laser annealing for 4H-SiC
  - No laser annealing for SiC engineered substrate



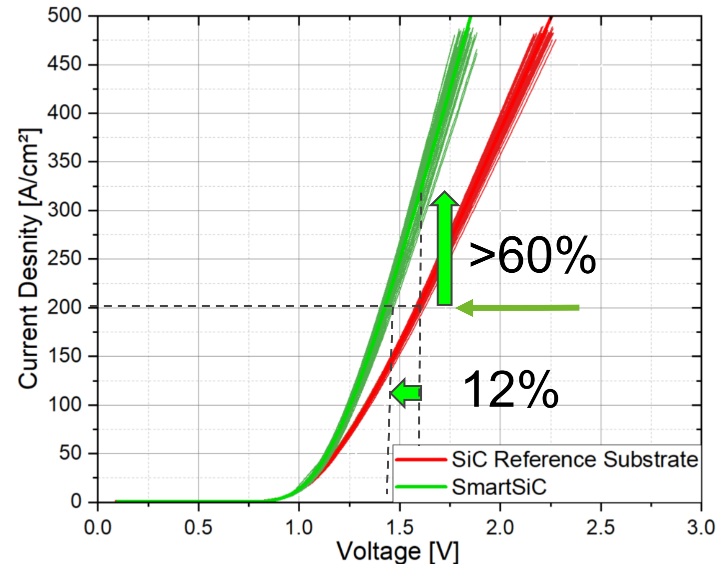


Diodes on Engineered Substrates: forward characteristics

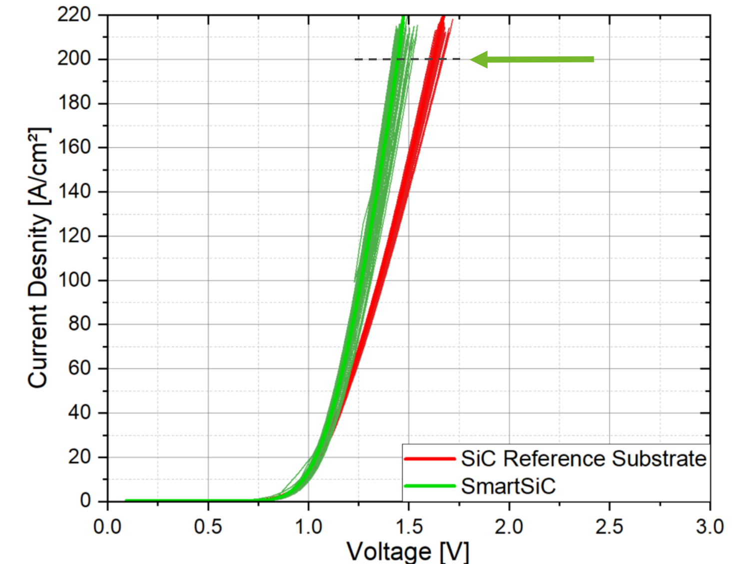
JBS diodes
340x340µm
0.2A current rated



MPS diodes
1.6x1.6mm
4A current rated



MPS diodes
2.5x2.5mm
9A current rated

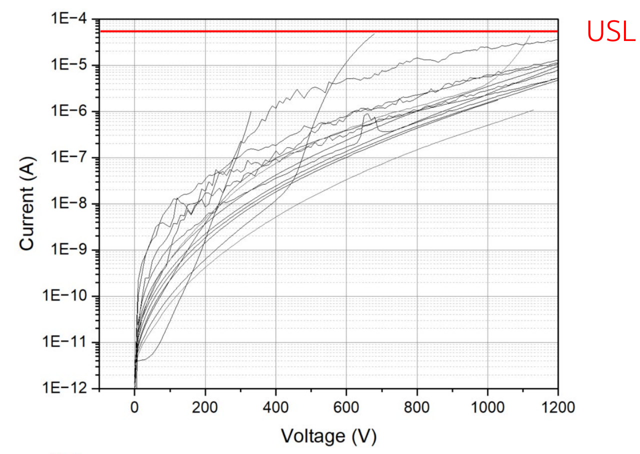


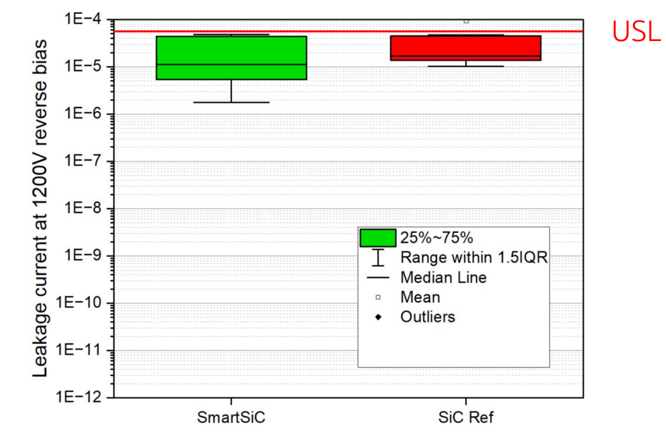
- 12% gain in V_F (@ 200 Amp/cm²) for all diodes
- 60% gain in forward current at constant forward voltage

In line with engineered substrate characteristics

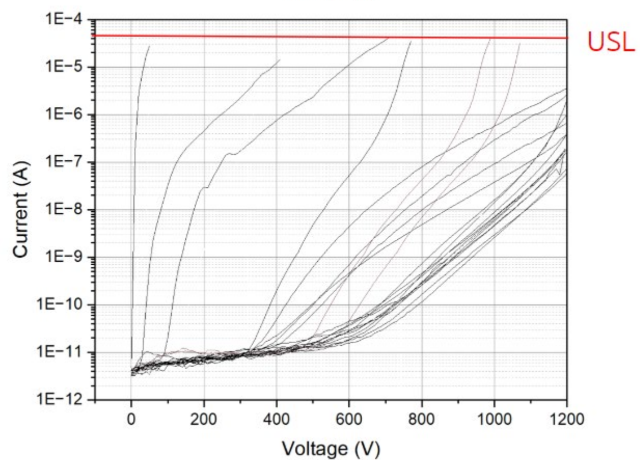
Diodes on Engineered Substrates: reverse characteristics

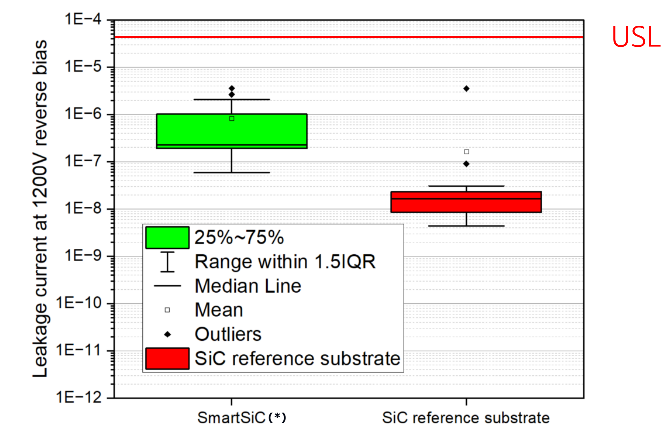
JBS diodes





PIN diodes





(*) 20% higher n- doping concentration

Reverse current within device specification limits

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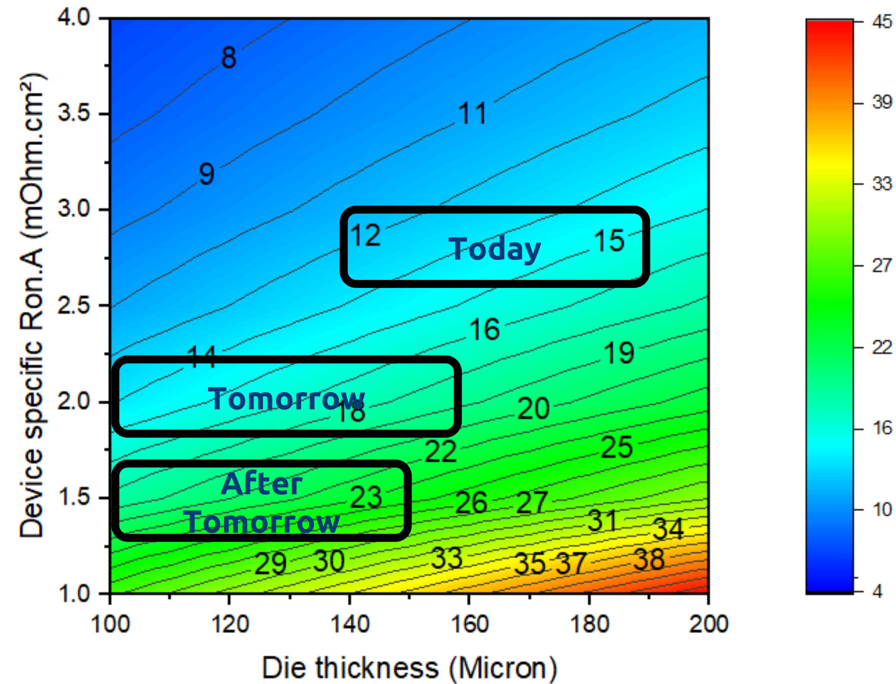
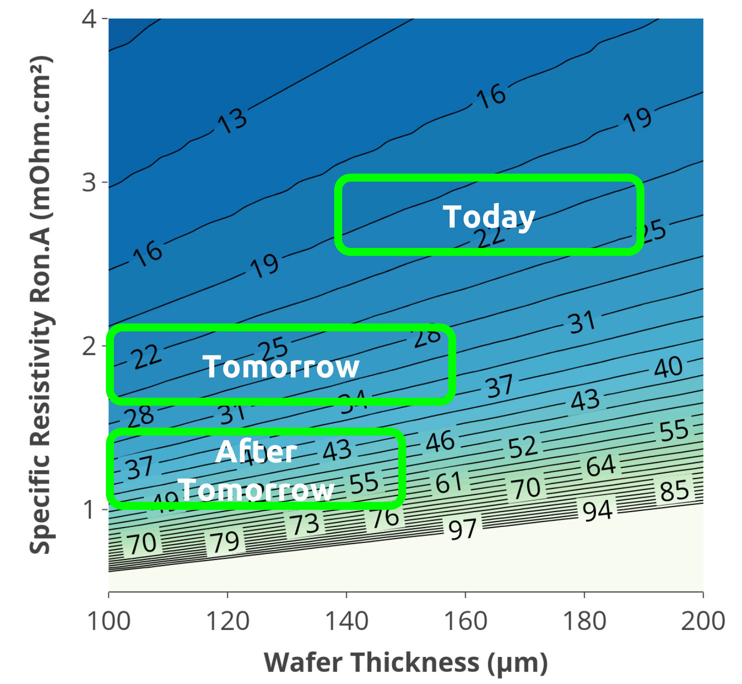
SiC Engineered Substrate: unleashing performance and productivity

Percentage of Ron.A gain vs. initial Ron.A and wafer thickness

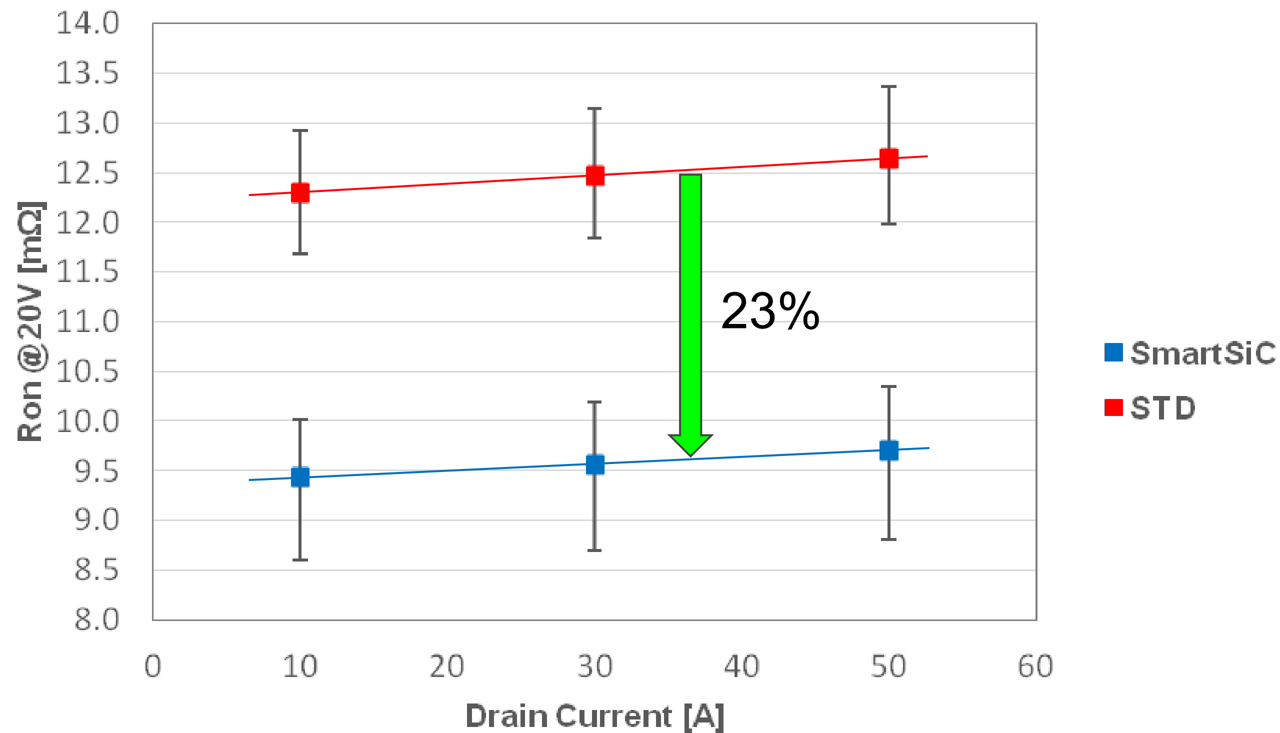


Percentage of Addtl. Good Die/Wfr vs. initial Ron.A and wafer thickness



Increasing manufacturing capacity at no additional CAPEX

Results from an HVM SiC MOSFET: gain equivalent to a generation leap



13mOhm 650V Gen 2 MOSFET

Funded by the Key Digital Technologies Joint Undertaking under Grant Agreement No. 101007237

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Bodo´s Power Systems®

23% Ron reduction, without any mask nor process step change

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Takeaways and Next Steps

- **SiC engineered substrates, based on the Smart Cut™ process, provide optimized characteristics from:**
  - Single-crystal 4H-SiC high-quality top layer
  - Ultra-high conductivity polycrystalline SiC base wafer

- **SiC engineered substrates offer unprecedented advantages**
  - Minimal substrate contribution to the total device resistance
  - CO_2 footprint reduced by a factor of 4 with respect to a standard SiC wafer
  - Capability to skip backside laser annealing, reducing CAPEX and OPEX
  - Ruggedness to bipolar degradation

- **Demonstrated improved performance for diodes and transistors equivalent to a generation leap**
  - Optimizing manufacturing capacity at no additional CAPEX

- **Next steps (submitted for ICSCRM 2024):**
  - Planar and trench MOSFETs: conduction and switching losses
  - Reliability assessment: current surge, short circuit

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感谢您的关注
THANK YOU FOR YOUR ATTENTION

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