pcim
ASIA

Current Sharing Issues of Paralleled SiC MOSFET

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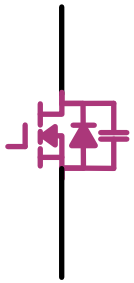
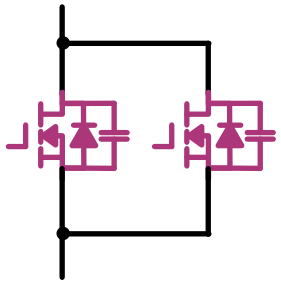
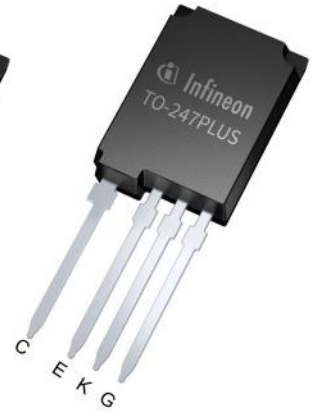
Parallelling for high power rating trend

– Low power rating

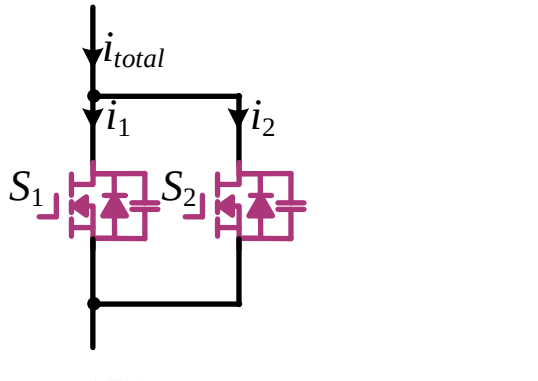


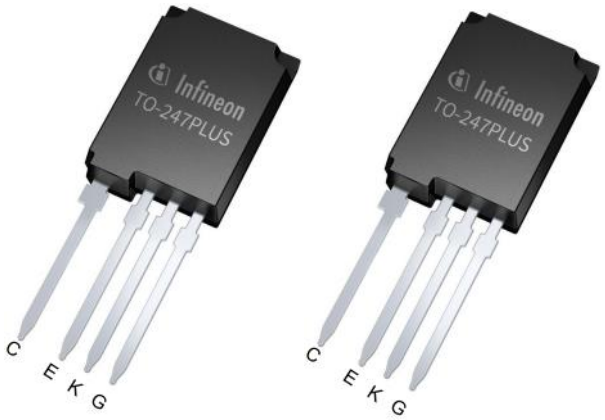
– High power rating



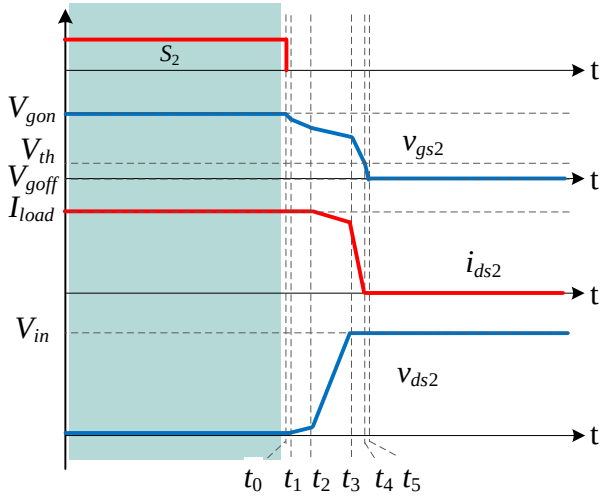


On-state / dynamic current sharing

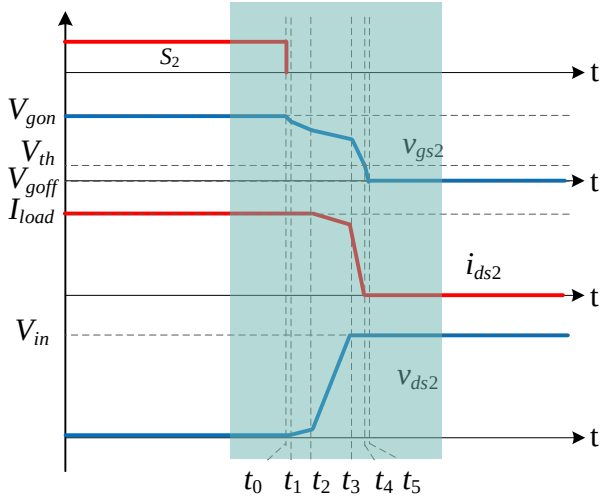




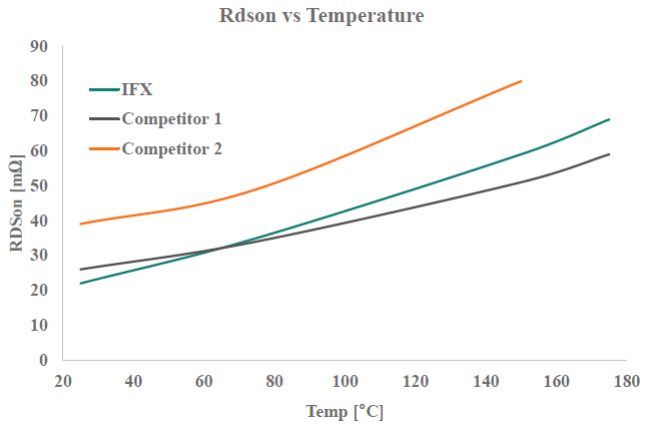
On-state current sharing

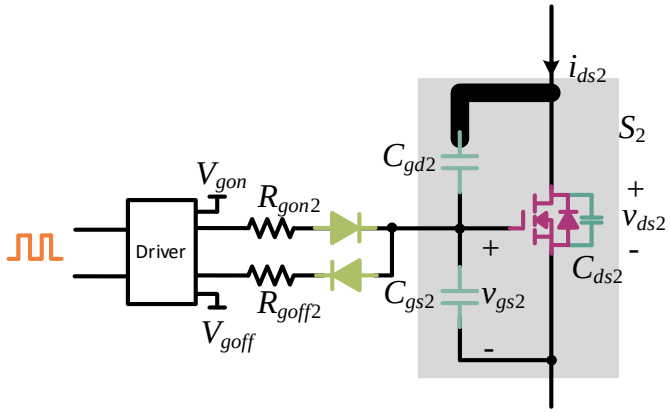


Dynamic current sharing



Infineon CoolSiC™ MOSFET2000 V





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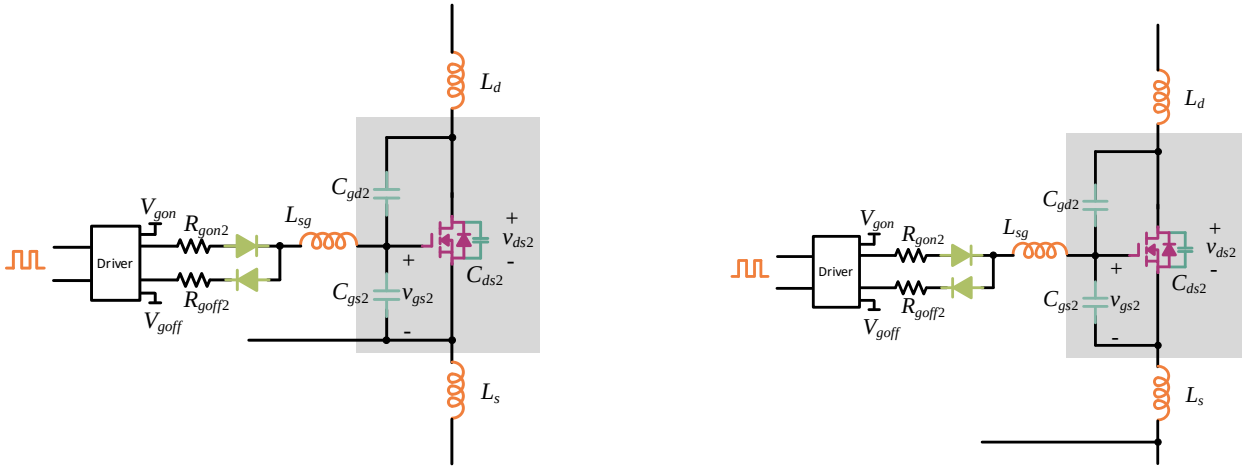
Parameters effect the current sharing of paralleled SiC MOSFET

	Semiconductor parameter	Circuit parameter
ON-state current sharing	ON resistance R_{dson}	Power loop stray inductance L_{sp}
Dynamic current sharing	Threshold voltage $V_{gs\text{-}th}$	Driver stray inductance L_{sg}
	Device capacitance	Source stray inductance L_s
	transconductance g_{fs}	
	Internal gate resistance $R_{g\text{-}in}$	

On-state current sharing

ON resistance R_{dson} & Power loop stray inductance L_{sp}



a. 4 pin stray parameters

b. 3 pin stray parameters

Fig. 1. Drain stray inductance L_d, source stray inductance L_s and driver stray inductance L_{sg} in circuit

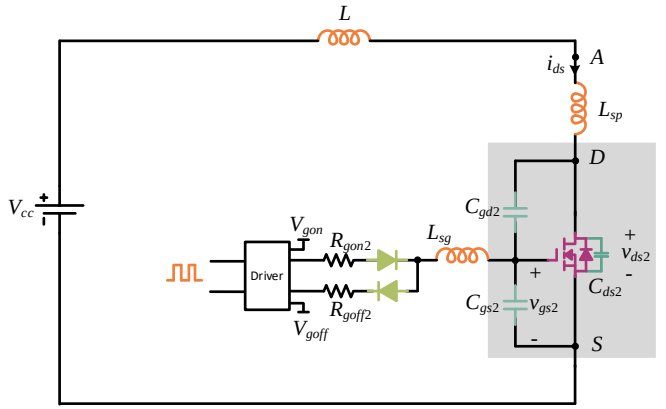


Fig. 2. Schematic for power loop stray inductance impact

$$V_{as}(t) = R_{dson} \times i_{ds}(t) + L_{sp}\frac{di_{ds}(t)}{dt}$$

$$i_{sum}(t) = I_o + \frac{V_{cc}}{L}t$$

$$i_{ds1}(t) = C \times e^{-\frac{2R_{dson}t}{L_{sp1}+L_{sp2}}} + \frac{LR_{dson}I_o + L_{sp2}V_{cc}}{2L \times R_{dson}} + \frac{V_{cc}}{2L}\left(t - \frac{L_{sp1}+L_{sp2}}{2R_{dson}}\right)$$

Where, $C = \frac{I_o}{2} + \frac{L_{sp1}V_{cc} - L_{sp2}V_{cc}}{4LR_{dson}}$

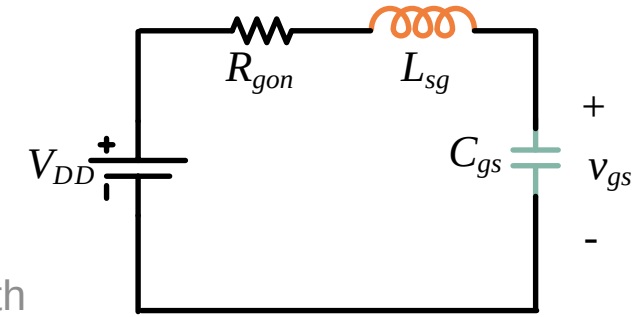
The more difference of L_{sp1} and L_{sp2}, there will be higher current difference between i_{ce1}(t) and i_{ce2}(t).

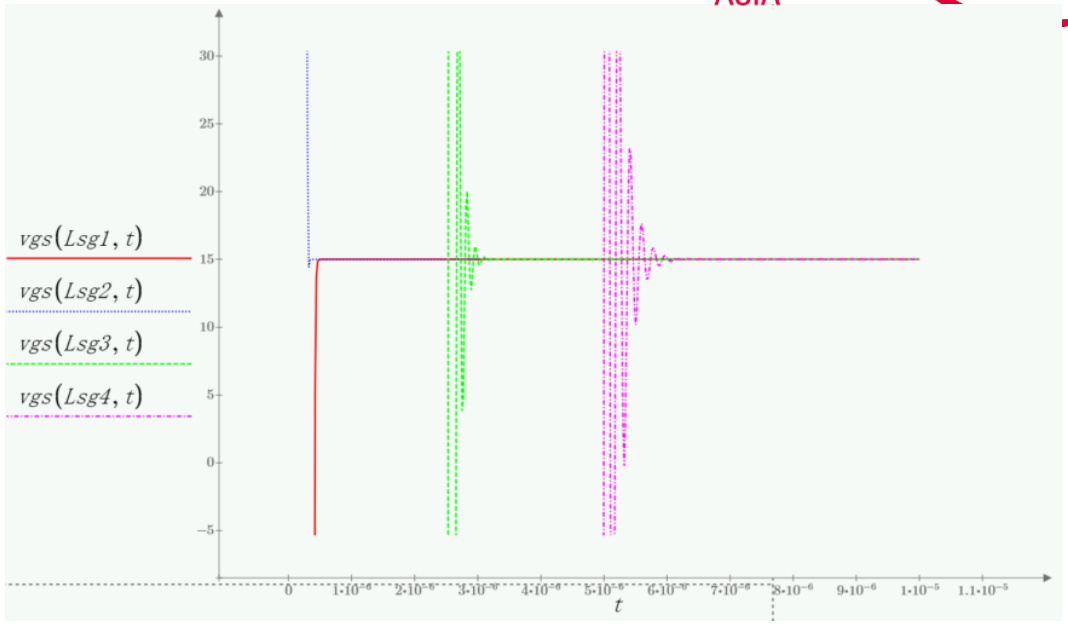
Dynamic current sharing

- Internal gate resistance Rg-in
- Transconductance gfs
- Device capacitance
- Threshold voltage Vgs-th
- Power loop stray inductance L_{sp}
- Driver Stray Inductance
- Source Stray Inductance

Dynamic current sharing

- ✓ Internal gate resistance Rg-in
- ✓ Transconductance gfs
- ✓ Device capacitance
- ✓ Threshold voltage Vgs-th
- ✓ Power loop stray inductance *Lsp*
- ☐ Driver Stray Inductance
- ☐ Source Stray Inductance





$$v_{gs}(t) = A_1 \times e^{\left(-\frac{R_{gson}}{2L_{sg}}+\sqrt{\frac{R_{gson}}{2L_{sg}}^2-\frac{1}{L_{sg}C_{gs}}}\right)t} + A_2 \times e^{\left(-\frac{R_{gson}}{2L_{sg}}-\sqrt{\frac{R_{gson}}{2L_{sg}}^2-\frac{1}{L_{sg}C_{gs}}}\right)t}$$

$$A_1 = \frac{V_{goff}-V_{gon}}{2} \times \left(\frac{\frac{R_{gson}}{2L_{sg}}}{\sqrt{\frac{R_{gson}}{2L_{sg}}^2-\frac{1}{L_{sg}C_{gs}}}}+1\right) \qquad A_2 = \frac{V_{goff}-V_{gon}}{2} \times \left(-\frac{\frac{R_{gson}}{2L_{sg}}}{\sqrt{\frac{R_{gson}}{2L_{sg}}^2-\frac{1}{L_{sg}C_{gs}}}}+1\right)$$

Lsg increases, current oscillation is getting worse and turn on delay time is getting longer.

Dynamic current sharing

- ✓ Internal gate resistance Rg-in
- ✓ Transconductance gfs
- ✓ Device capacitance
- ✓ Threshold voltage Vgs-th
- ✓ Power loop stray inductance *Lsp*
- ✓ Driver Stray Inductance
- ☐ Source Stray Inductance

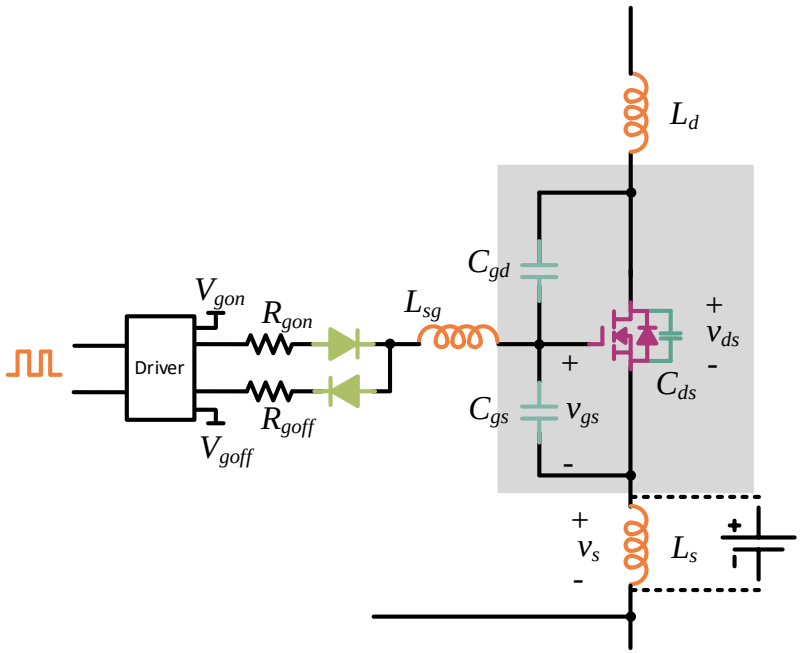


Fig. 5. Source stray inductance effect during turn on process in 3pin device

$$v_s(t) = L_s \frac{di_{ds}(t)}{dt} \qquad V_{gs}(t) = V_{gon} - R_{gon} \times i_{gs}(t) - L_s \frac{di_{ds}(t)}{dt}$$

Lsg increases, current oscillation is getting worse and turn on delay time is getting longer.

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Infineon's SPICE model

Infineon's SPICE model can be divided into L1(level 1), L2(level 2) and L3(level 3).

- L1 is the behavioral modelling approach
- L2 is physics-based modelling approach
- L3 is coupled electro-thermal modelling

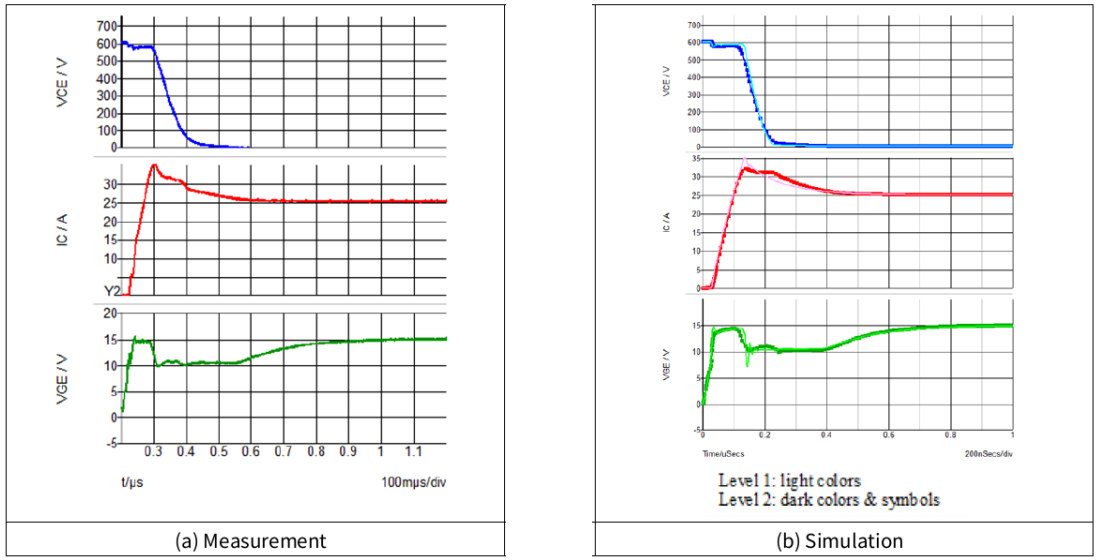


Fig. 7. L1 and L2 SPICE model simulation results

L1 : faster computation speed and reasonable accuracy within the calibrated range

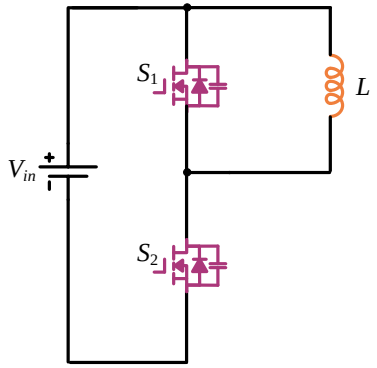
L2 : more precise representation of the switching transi-ents over a wide range of operating points, but slower simulation speed and convergence instability

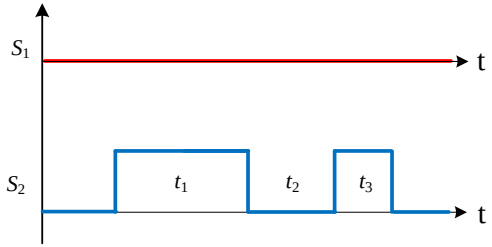
L3 : ???

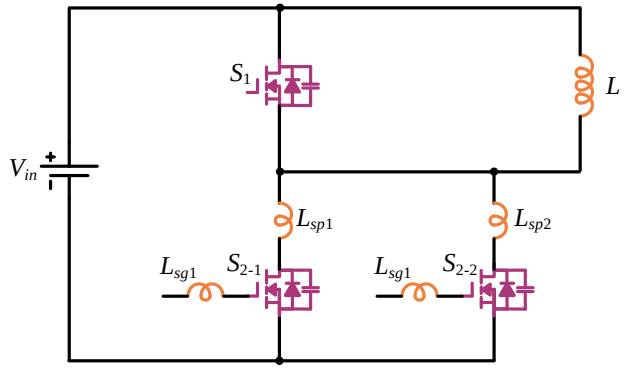
Simulation Results

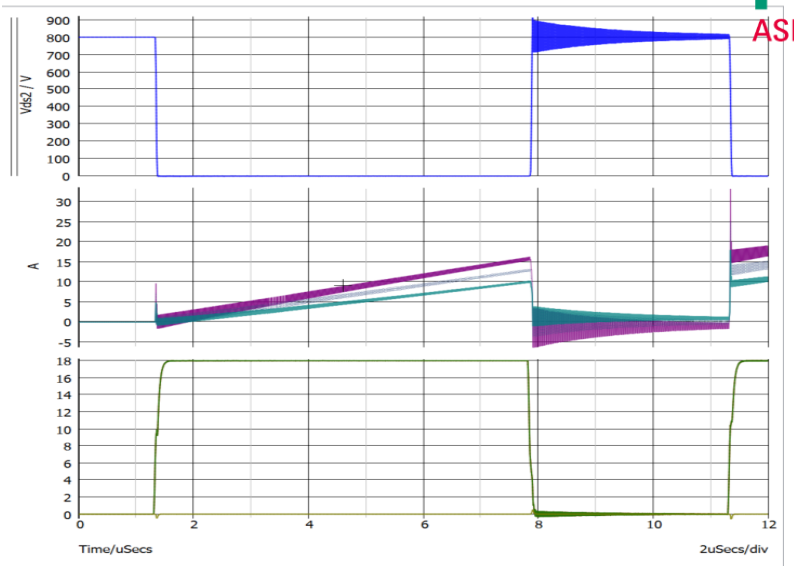
Tab. 2. Double pulse test parameters

	value	unit
Voltage	800	V
Inductance	200	uH
t1	6.5	us
t2	3.5	us
t3	2	us



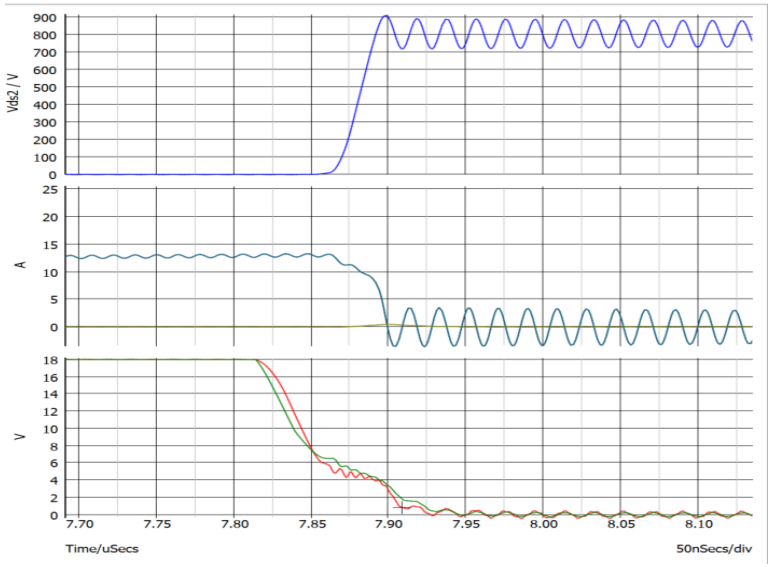






a. L_{sp1}=5nH

L_{sp2}=10nH



b. L_{sg1}=5nH

L_{sg2}=50nH

Excessive inductance L_{sp} causes V_{ds} drops sharply when the switches are turned on. With the increase of L_{sp} mismatch, the ON-state current sharing shows problem, unbalance current increases.

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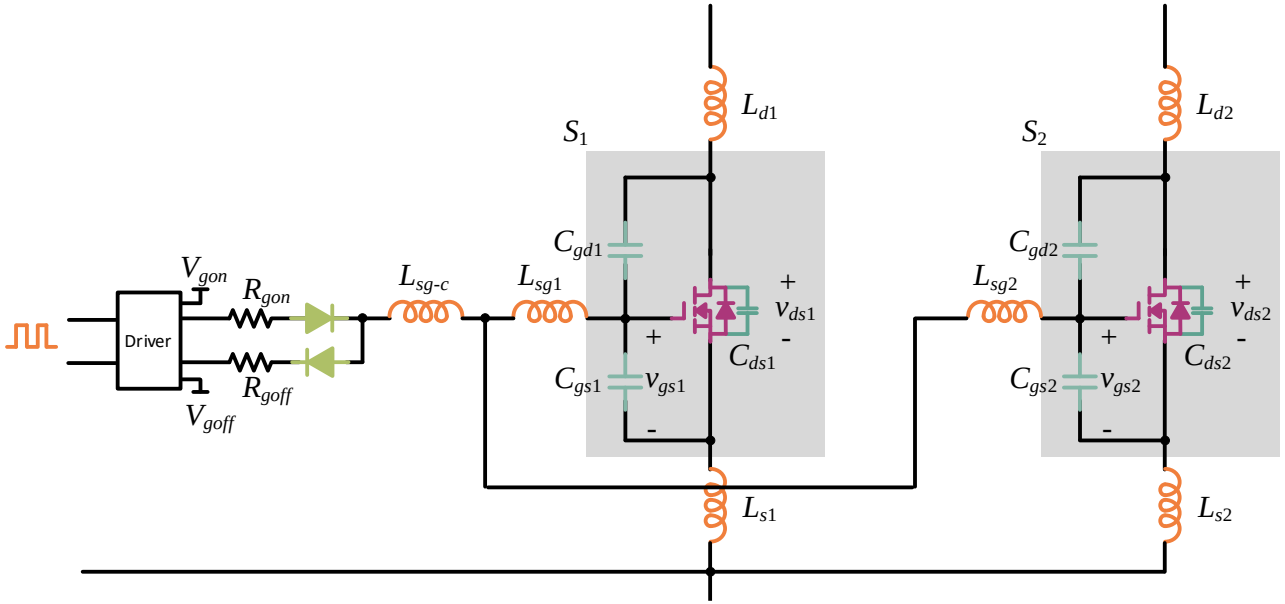
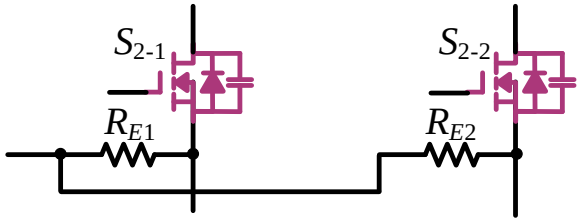
Driver Circuit Design: Coupling from Stray Parameters



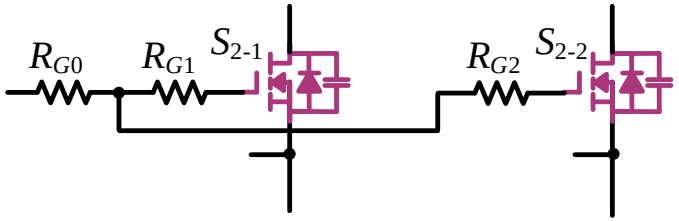
It's recommended to optimize PCB layout and achieve symmetric driver loop and power loop design.

Driver Circuit Design: Coupling from Device Parameters

Two methods to improve the parallel performance:



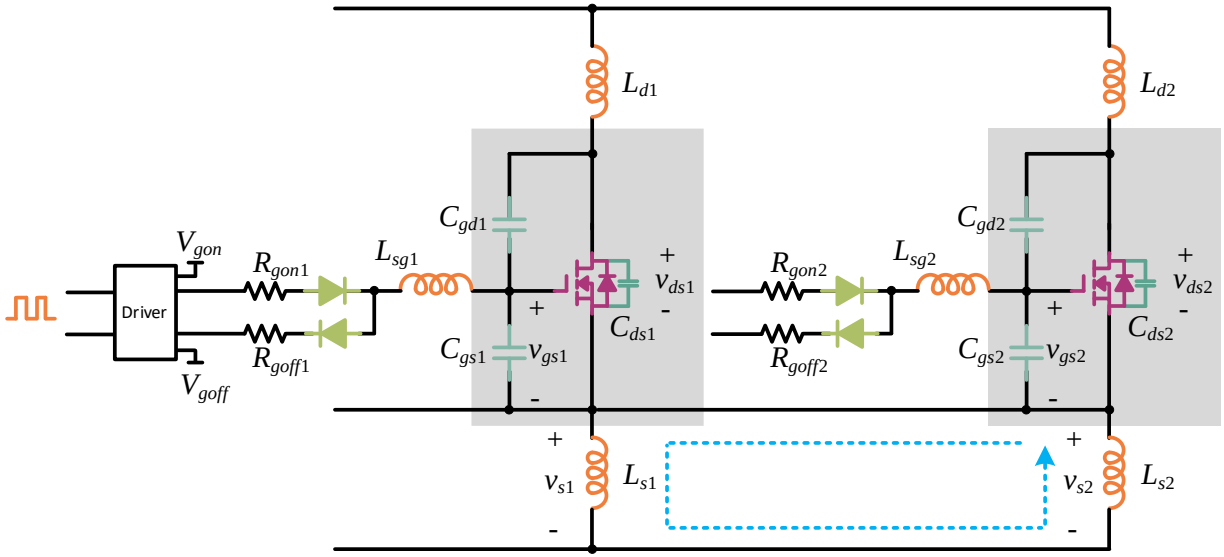
◆ method I



◆ method II

Take two 4pin SiC MOSFETs as example, the KS and S are connected separately and there will be a small source loop between L_{s1} and L_{s2}.

$$v_{s1/2}(t) = L_{s1/2}\frac{di_{ds1/2}(t)}{dt}$$



Driver Circuit Design: Coupling from Device Parameters

– **Method I**

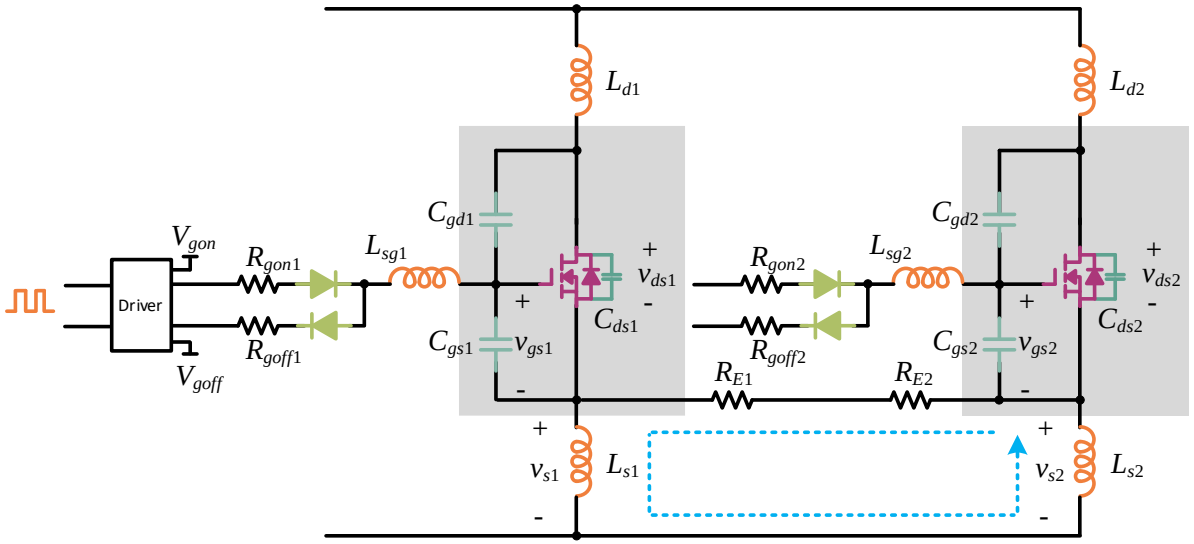


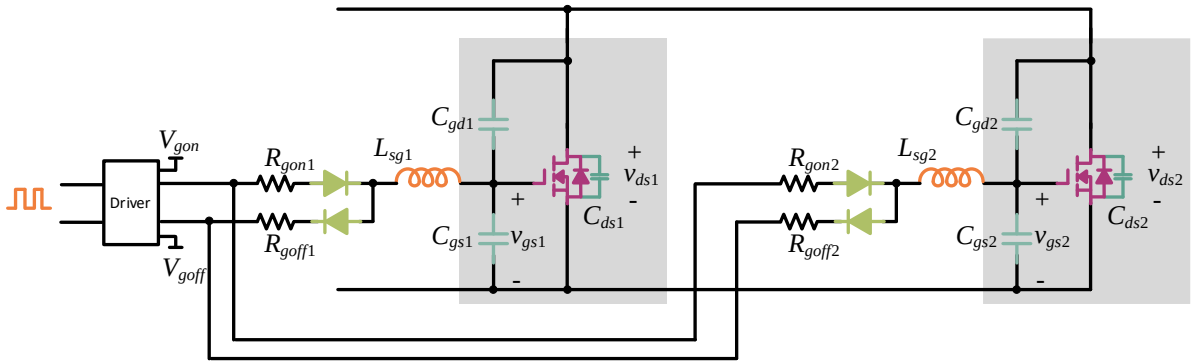
Fig. 13. R_{E1} and R_{E2} add extra resistance in source loop

The high current in small source loop is under control. Oscillation and EMI issue caused by the loop current can be avoided. Using method I, the gate resistor can be separated into Rg and RE, the driver performance remains same.

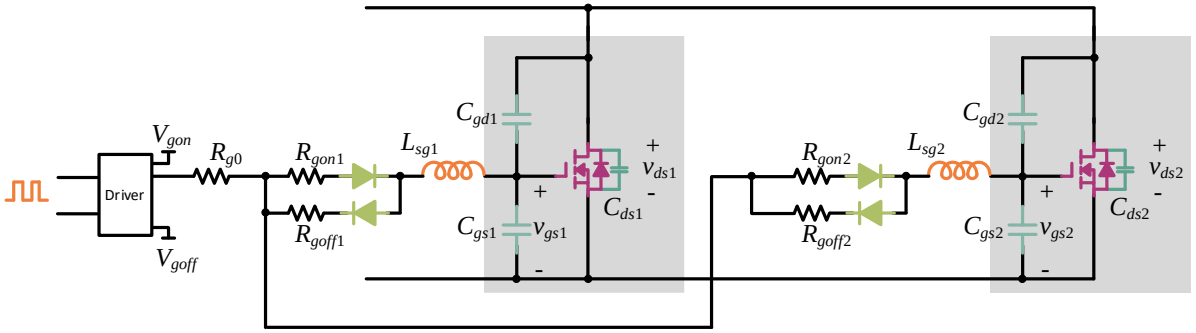
As a rule of thumb, the RE/Rg ratio is between 1/5 and 1/10. In order to achieve proper current limiting func-tion, RE should be selected more than 0.5 Ω.

Driver Circuit Design: Coupling from Device Parameters

– **Method II**



a. The traditional gate connection for paralleled device



b. Gate loop connection for paralleled device using method II

$$v_{gs}(t) = V_{gon} + (V_{goff} - V_{gon}) \times e^{-\frac{t}{C_{gs}R_g}}$$

$$i_{gs}(t) = \frac{(V_{gon} - V_{goff}) \times e^{-\frac{t}{C_{gs}R_g}}}{R_g}$$

Higher gate current builds a higher voltage on R_{g0}, which will slow down both S_1 and S_2. Adding R_{g0}, the imbalance can get smaller.

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Conclusion

- Mismatch of device parameters and inequality of circuit parameters all have impact on the paralleling performance.
- The theoretical analysis and SPICE simulation is presented to show the circuit parameters' influence on operation.
- From simulation result, Lsg difference would change the Vge waveform and Lsp difference causes the ON-state current difference.
- Two circuit design point is shown for better paralleling performance.


Infineon