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Analysis of the effect of system parasitic parameters on the switching of SIC devices

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2 Switching current oscillation

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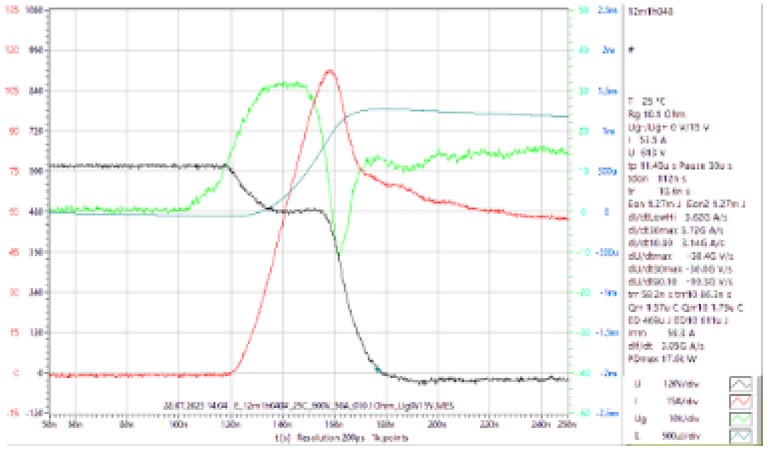
SIC-MOS turn-on process with different continuum diodes

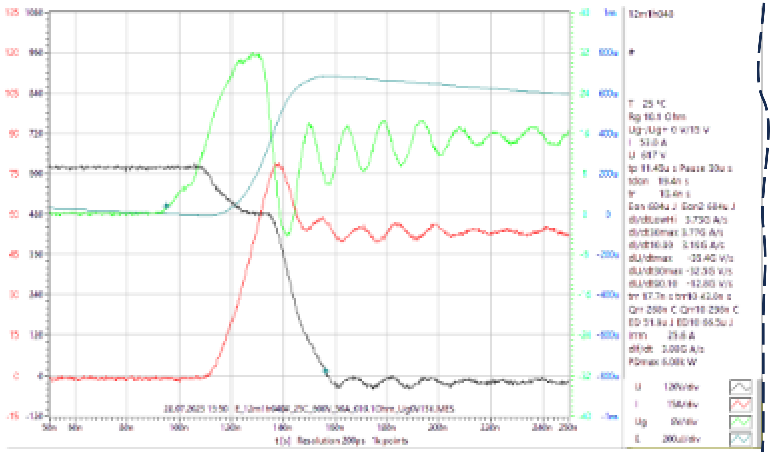
– Even if a Schottky diode is used, there is a turn-on current overshoot like reverse recovery

SIC MOS + SI Diode



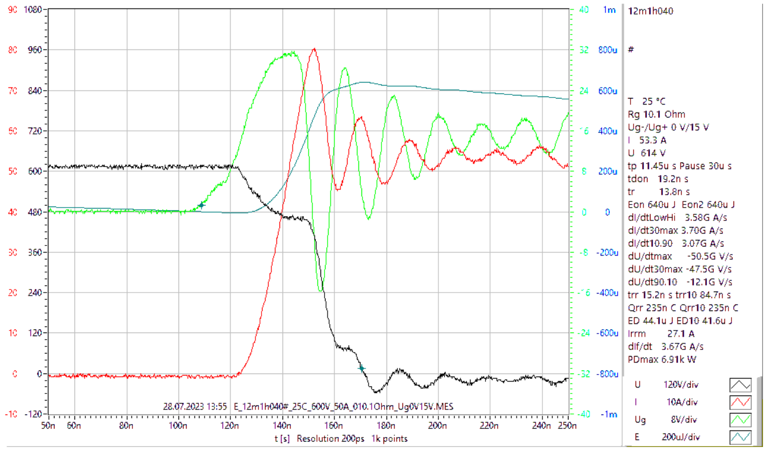
IMW120R040M1H+ 1200V 50A CH7 for reverse parallel Si Diode
RT, Rg on/off 10ohm/600VDC/ 50A /

SIC MOS + SIC Body Diode



IMW120R040M1H+ IMW120R040M1H body SiC diode
RT, Rg on/off 10ohm/600VDC/ 50A /

SIC MOS + SIC Schottky Diode

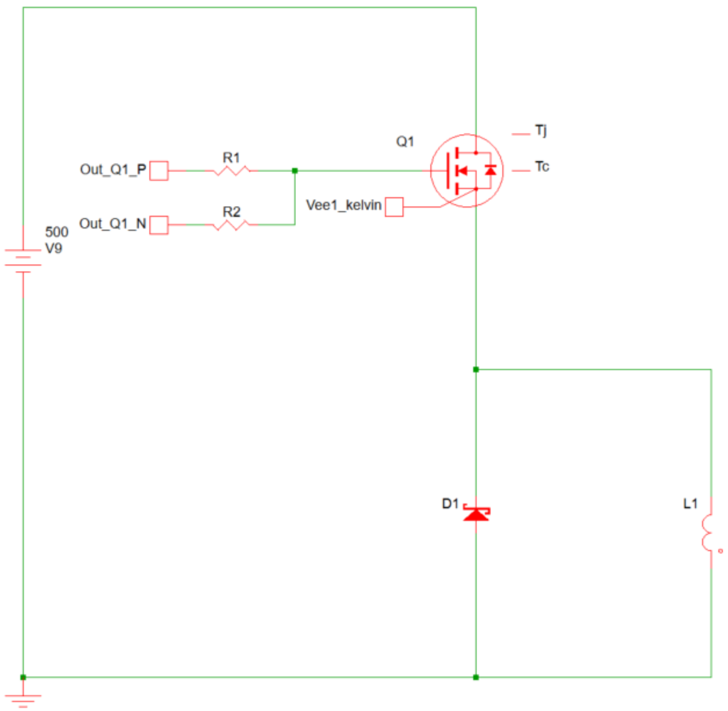


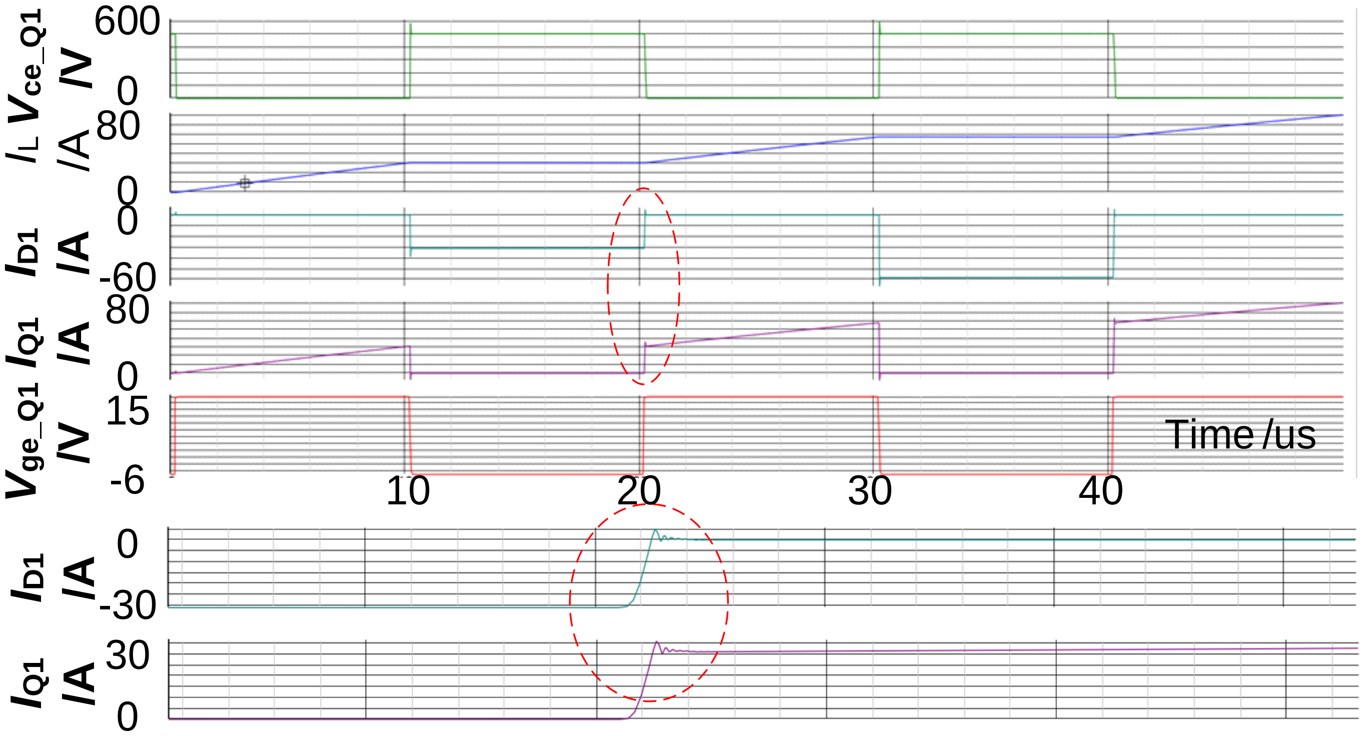
IMW120R040M1H+ 1200V 30A SiC Schottky diode

RT, Rg on/off 10ohm/600VDC/ 50A /

SPICE model-based simulation of SIC-MOS turn-on

– Simulations based on the Spice model also observe this current overshoot like reverse recovery



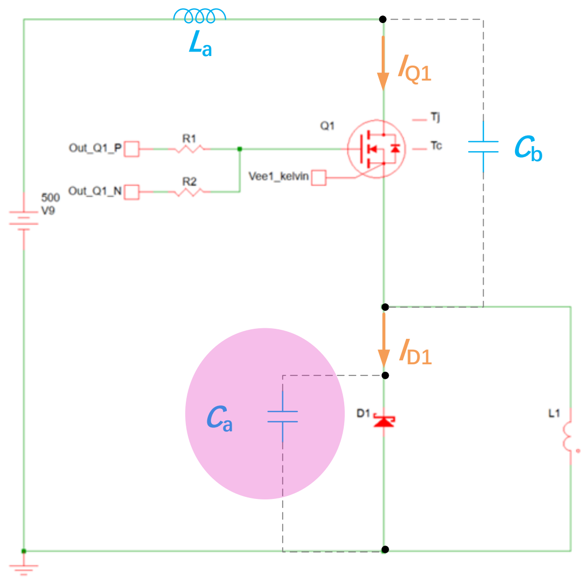


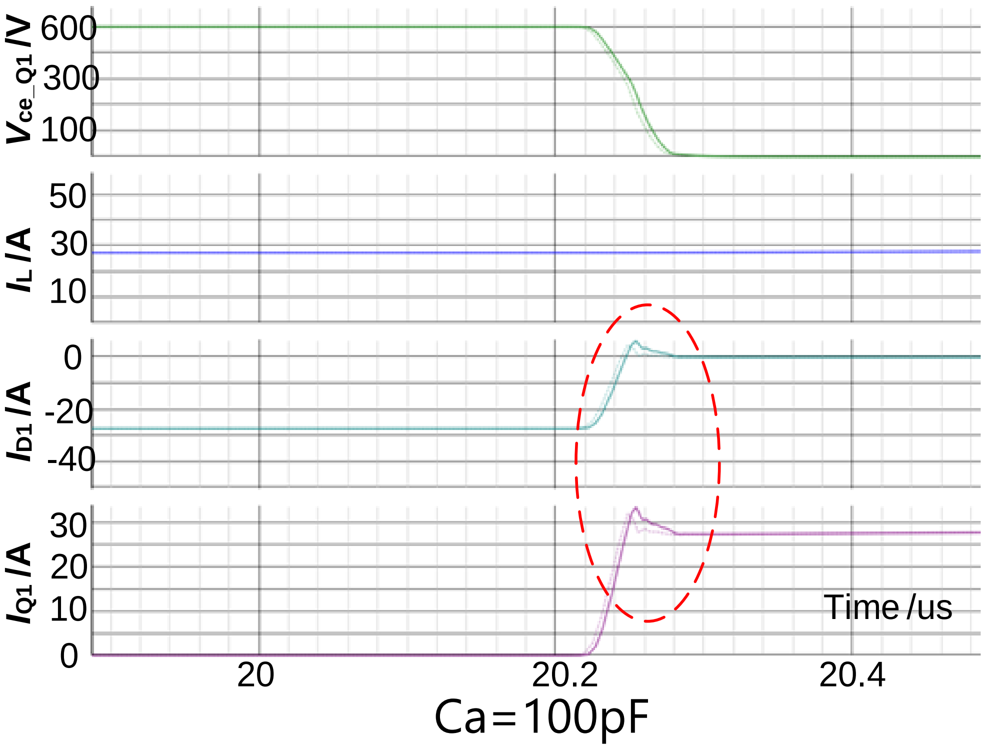
SPICE model-based simulation of SIC-MOS turn-on

– **Effect of parasitic capacitance of the freewheeling diode**

Parasitic capacitance parameters of IDW30G120C5B

Parameter	Symbol	Conditions	Value	Unit
Total Capacitance	*C*	V_R=1V, *f*=1MHz	990/1980	pF
		V_R=400V, *f*=1MHz	70/140	
		V_R=800V, *f*=1MHz	55/111	





SPICE model-based simulation of SIC-MOS turn-on

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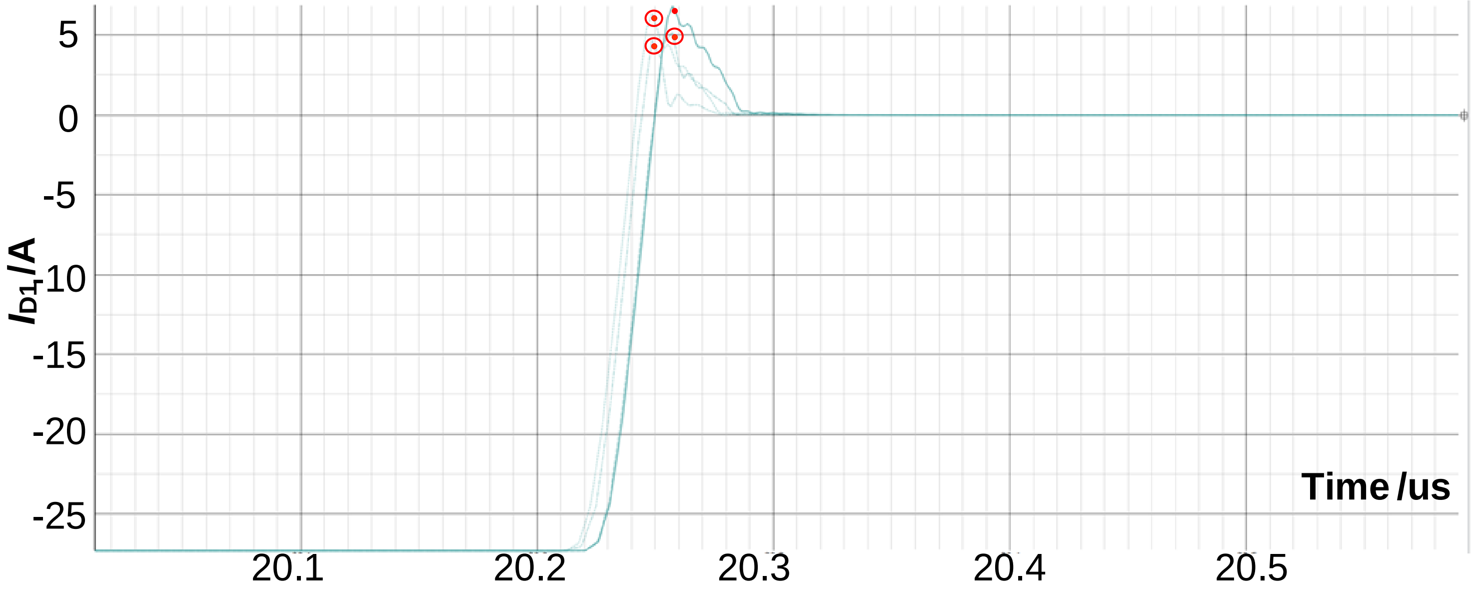
- Effect of parasitic capacitance of the freewheeling diode
- Overall, as the diode parallel capacitance increases, the equivalent ‘reverse recovery current’ increases

C_a(pF)	I_L(A)	I_{D1}(A)	I_{Q1}(A)	I_{Q1}- I_L(A)
/	27.3	4.68	31.98	4.68
100	27.3	5.18	32.47	5.17
200	27.3	6.27	33.61	6.31
300	27.3	6.65	33.99	6.69



(none, 100pF, 200pF, 300pF)

SPICE model-based simulation of SIC-MOS turn-on

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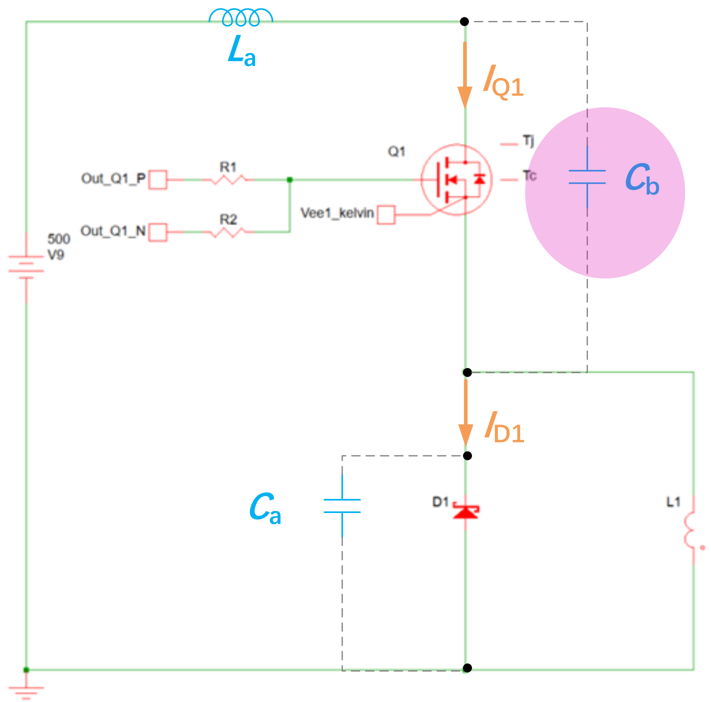
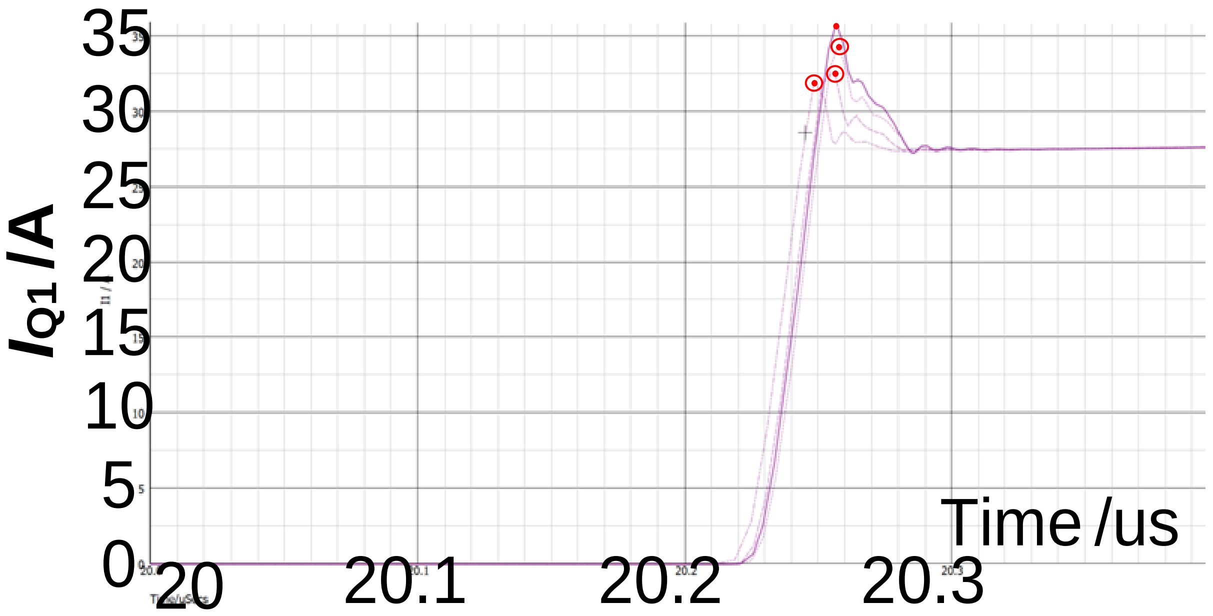
- **Effect of parasitic capacitance of the switching arm**
- the switching current I_{Q1} also tends to increase with the increase of C_b, which is mainly due to the parasitic capacitance of the MOS discharging to the channel at the on-time instant



C_b(pF)	I_L(A)	I_{D1}(A)	I_{Q1}(A)	I_{Q1}- I_L(A)
/	27.3	4.61	31.94	/
100	27.3	3.58	32.63	/
200	27.3	4.03	34.36	/
300	27.3	4.11	35.64	/



C_b (none, 100pF, 200pF, 300pF)

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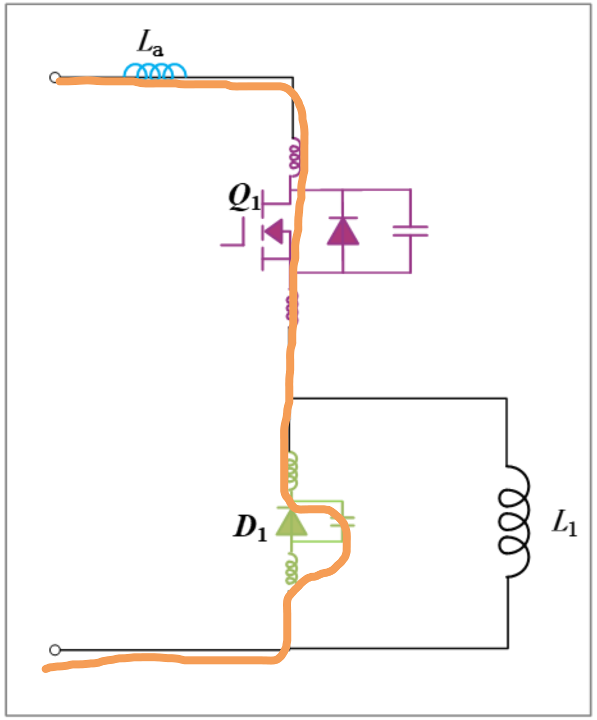
Switching current oscillation

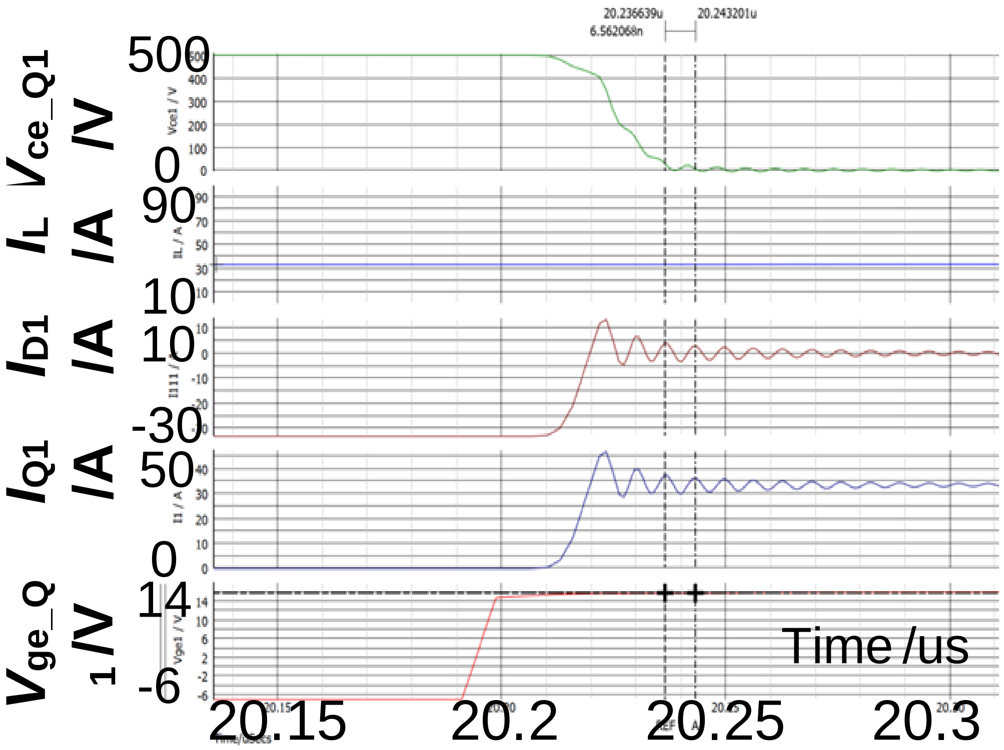
– SIC current oscillations are often encountered when using SIC devices

Switching current oscillation

– **Impact of freewheeling switch (or AC/bus-) Parasitic Capacitance on Oscillation**

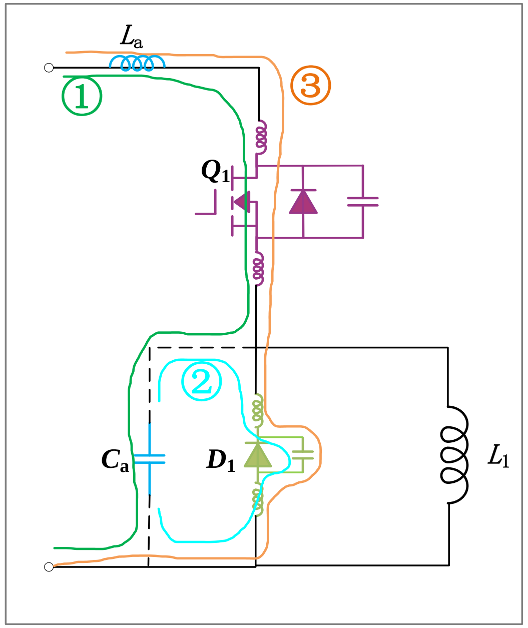


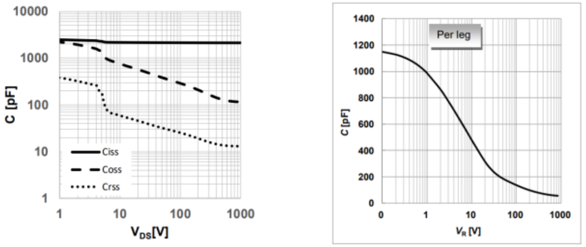
152MHz@Ca=none



Switching current oscillation

– **Impact of freewheeling switch (or AC/bus-) Parasitic Capacitance on Oscillation**





IMZ120R030M1H IDW30G120C5B

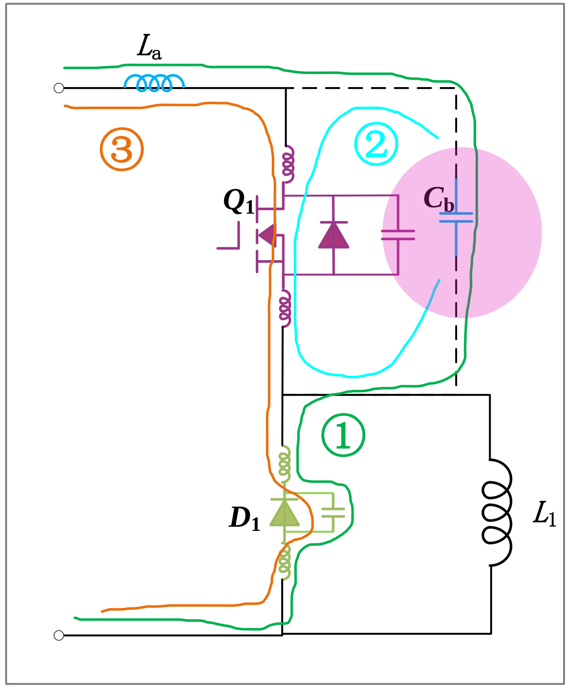
Fig. 9 Parasitic capacitance versus voltage curve

$$f = \frac{1}{2\pi\sqrt{LC}}$$

C_a (pF)	L_a (nH)	C_{equ} (pF)	L_{equ} (nH)	f_{sim} (kHz)	$f_{cal\text{-}loop1}$ (kHz)	$f_{cal\text{-}loop2}$ (kHz)	$f_{cal\text{-}loop3}$ (kHz)
/	/	60	13|6.5	**151**	/	/	**147**
100	/	60	13|6.5	**139**	**140**	322	147
200	/	60	13|6.5	**99**	**99**	291	147
300	/	60	13|6.5	**81**	**81**	279	147
/	15	60	15|13|6.5	**107**	/	/	**111**
100	15	60	15|13|6.5	**82**	**95**	322	111
200	15	60	15|13|6.5	**66**	**67**	291	111
300	15	60	15|13|6.5	**58**	**54**	279	111
/	30	60	30|13|6.5	**87**	/	/	**92**
100	30	60	30|13|6.5	**64**	**76**	322	92
200	30	60	30|13|6.5	**52**	**54**	291	92
300	30	60	30|13|6.5	**47**	**44**	279	92

Switching current oscillation

– **Impact of switch (or AC/bus +) parasitic capacitance on oscillation**



C_b (pF)	L_a (nH)	C_{equ} (pF)	L_{equ} (nH)	f_{sim} (kHz)	$f_{cal\text{-}loop1}$ (kHz)	$f_{cal\text{-}loop2}$ (kHz)	$f_{cal\text{-}loop3}$ (kHz)
/	/	60	13|6.5	**152**	/	/	**147**
100	/	60	13|6.5	**144**	322	140	**147**
200	/	60	13|6.5	**134**	291	99	**147**
300	/	60	13|6.5	**129**	279	81	**147**
/	15	60	15|13|6.5	**108**	/	/	**111**
100	15	60	15|13|6.5	**112**	177	140	**111**
200	15	60	15|13|6.5	**116**	160	99	**111**
300	15	60	15|13|6.5	**125**	153	81	**111**
/	30	60	30|13|6.5	**87**	/	/	**92**
100	30	60	30|13|6.5	**91**	136	140	**92**
200	30	60	30|13|6.5	**91**	123	99	**92**
300	30	60	30|13|6.5	**81**	118	81	**92**

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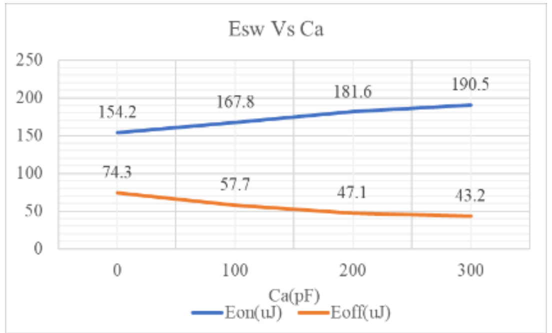
Effect of parasitic capacitance on SiC MOS switch performance

– **As the capacitance Ca increases, the frequency of oscillations decreases, and the peak value of the overcharge current increases.**

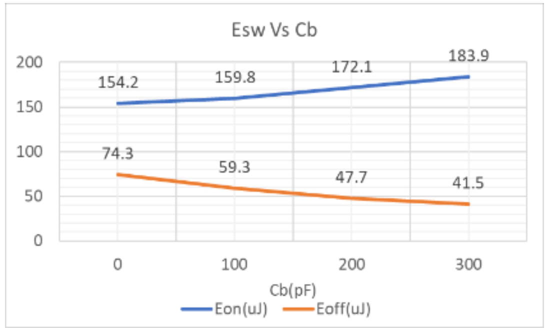
C_a=none, 100pF, 200pF, 300pF

Effect of parasitic capacitance on switching losses

- **As the capacitance Ca/Cb increases, the turn-on loss becomes larger, and the turn-off loss decreases**



C_a (pF)	I_L (A)	L_a (nH)	f_{sim} (kHZ)	I_{on_peak} (A)	E_{on} (uJ)	E_{off} (uJ)
/	33A	15	107	47.9A	154.2	74.3
100	33A	15	82	52.4A	167.8	57.7
200	33A	15	66	55.1A	181.6	47.1
300	33A	15	58	56.9A	190.7	43



C_b (pF)	I_L (A)	L_a (nH)	f_{sim} (kHZ)	I_{on_peak} (A)	E_{on} (uJ)	E_{off} (uJ)
/	33A	15nH	108	47.9	154.2	74.3
100pF	33A	15nH	112	50.9	159.8	59.3
200pF	33A	15nH	116	53.3	172.1	47.7
300pF	33A	15nH	125	55.9	183.9	41.5

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Effect of parasitic inductance on SiC MOS switch performance

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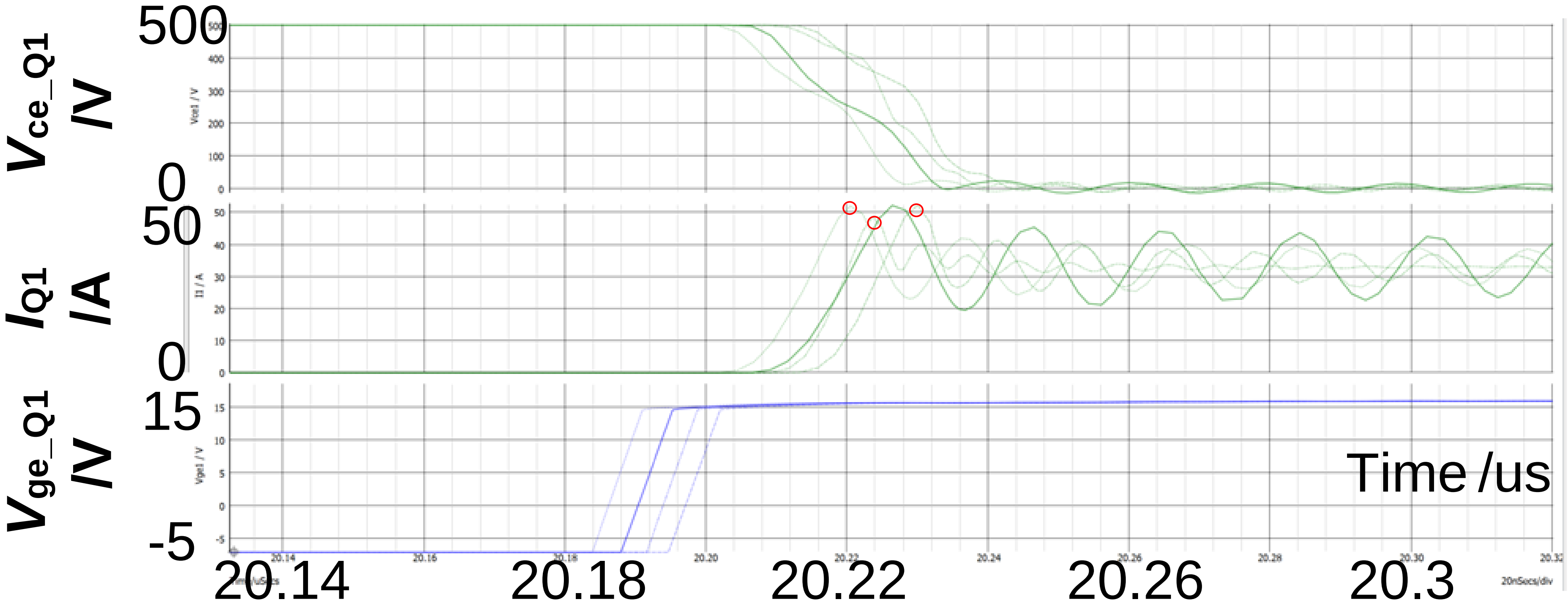
- With the increase of inductance La, the frequency of the oscillations decreases, the amplitude of oscillations is larger, and the speed of oscillations' attenuation

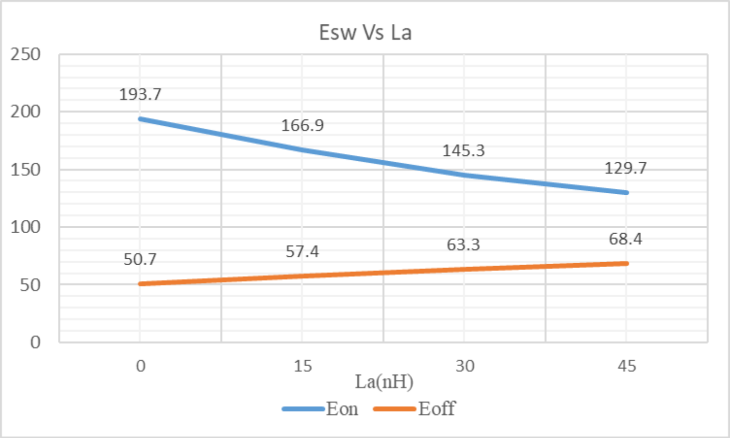


L_a=None/15nH/30nH/45nH

Effect of parasitic inductance on switching losses

– **Turn-on loss decreases and the turn-off loss increases as La increases**

C_b (pF)	I_L (A)	L_a (nH)	f_{sim} (kHZ)	I_{on_peak} (A)	E_{on} (uJ)	E_{off} (uJ)
100pF	33A	/	139	49.8	193.7	50.7
100pF	33A	15nH	83	51.9	166.9	57.4
100pF	33A	30nH	64	53.5	145.3	63.3
100pF	33A	45nH	53	53.2	129.7	68.4



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Effect of parasitic inductance on switching losses

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- **Over-current** during switch turn-on in SiC-MOS devices is **caused by the discharge** of switch bridge arm parasitic capacitance **and charging** of freewheeling diode bridge arm parasitic capacitance
- High-speed switching causes turn-on **current oscillation** due to the **resonance of parasitic inductance and capacitance** in the system circuit.
- System parasitic **inductance decreases** turn-on losses but **increases** turn-off losses, while system parasitic **capacitance has the opposite effect**.
- To optimize efficiency, designers need to pay attention to the negative impact of parasitic capacitance on turn-on losses in SiC devices during the design phase.

Thank you for your attention and time.