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Optimize Switching Transient of Paralleled SiC-MOSFETs by Using Adaptive Gate Current Shaping

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Agenda

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- Problem description & possible solutions
- Concept of this work: adaptive gate current shaping
- Measuring gate charge parameters (2 methods)
- Defining gate drive strength profiles
- Double pulse characterization test
- Alternative gate charge measurement characterization
- Conclusion & Outlook

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Problem description

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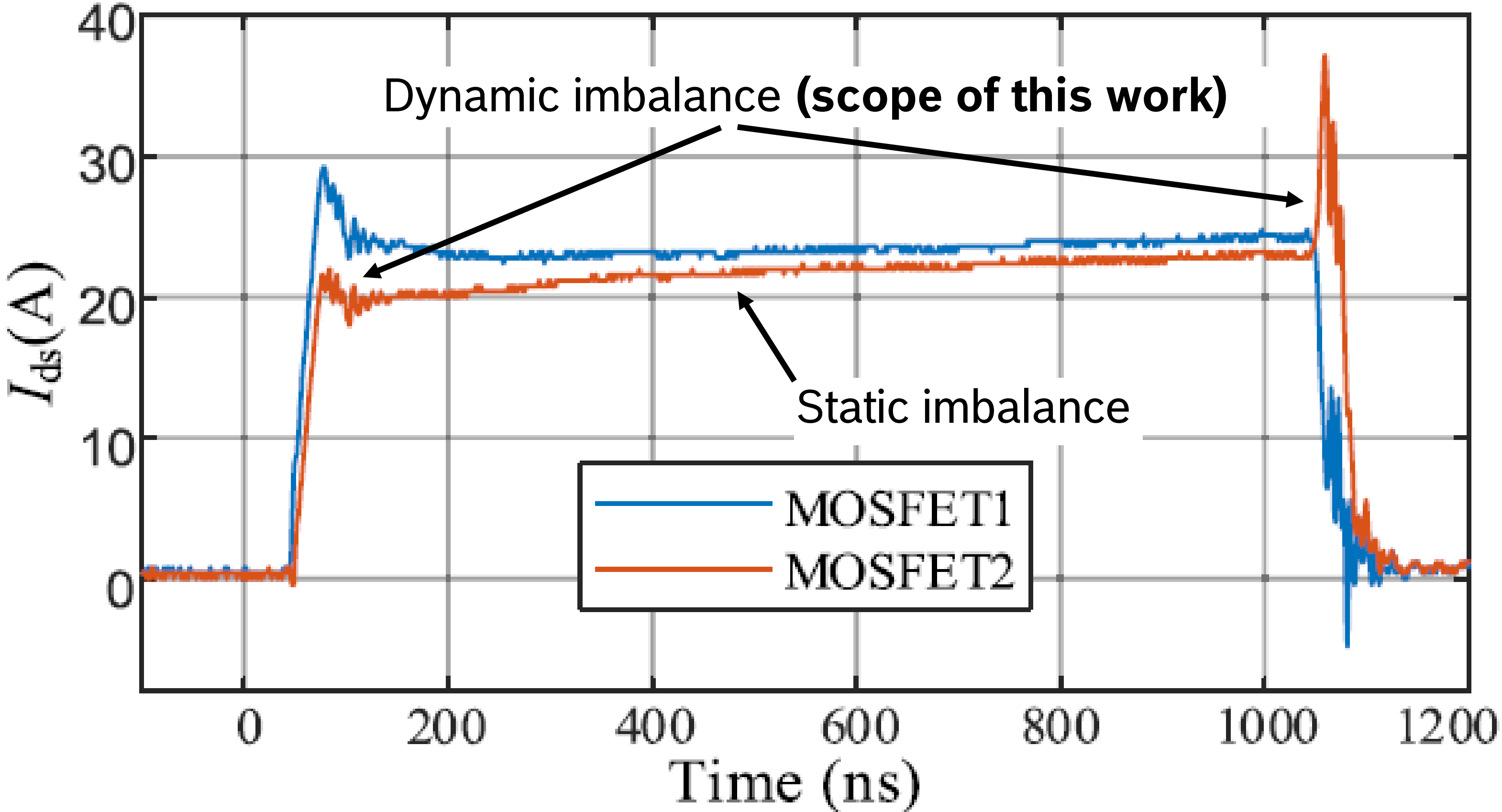

Resulting in huge variation of switching losses (requires oversizing), overshoots and EME & increased component stress

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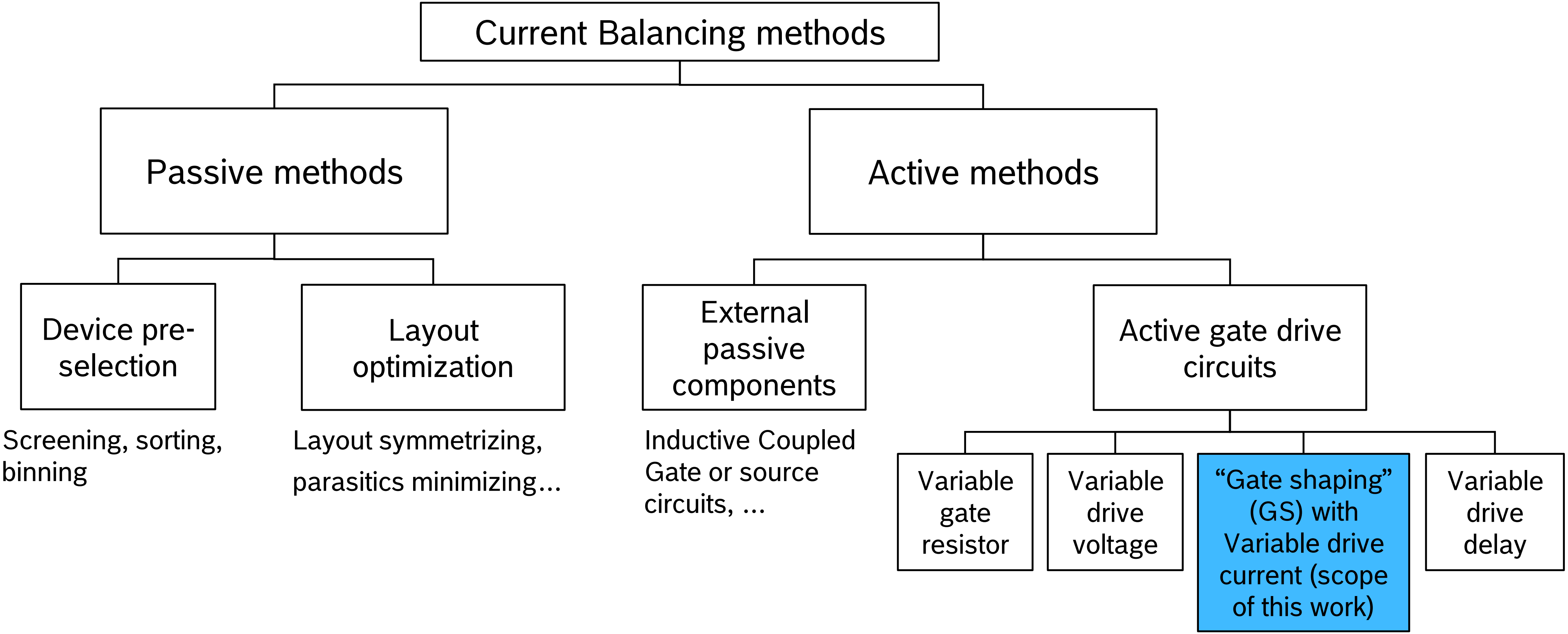
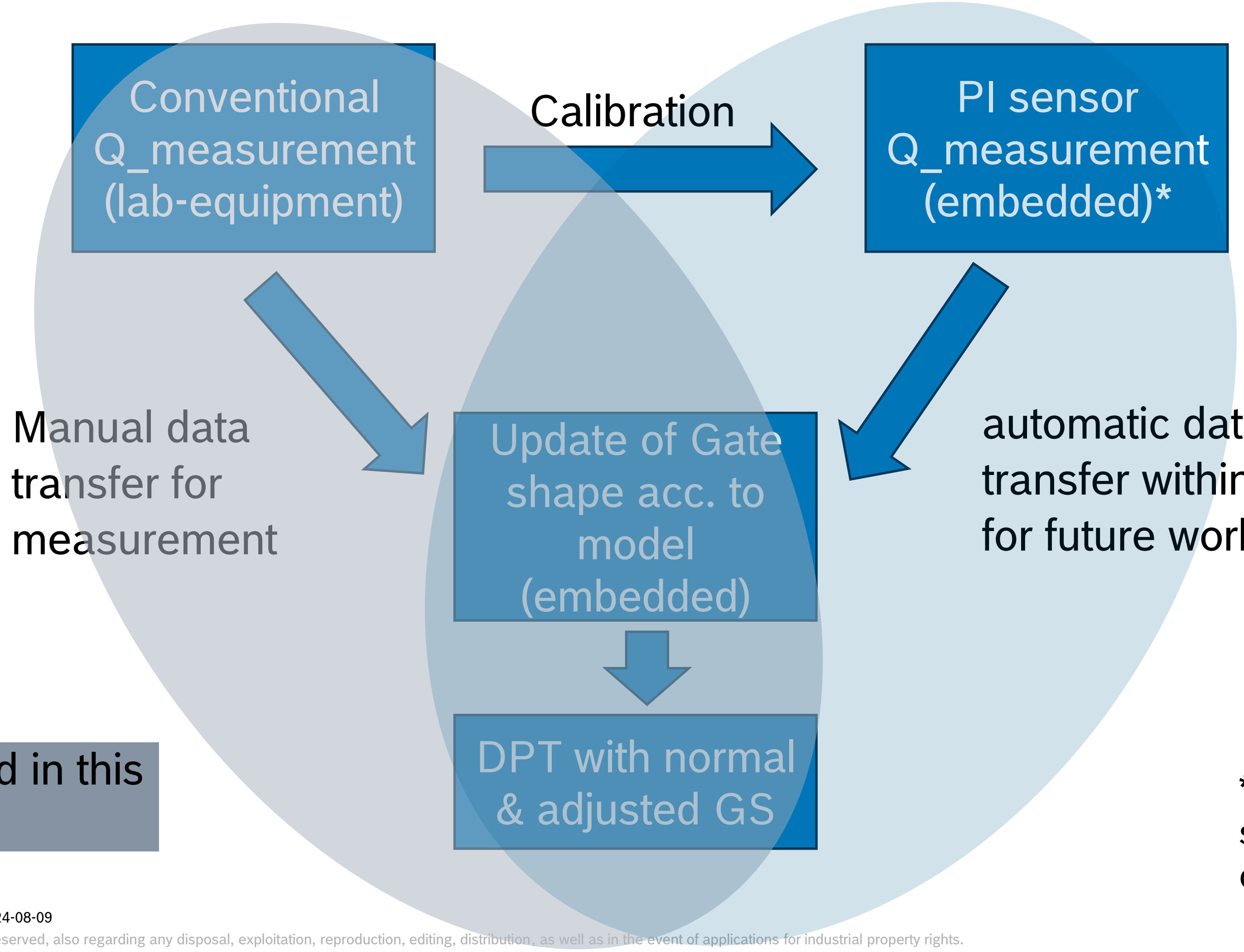
State of the art
Possible solutions



Adaptive gate current shaping
Concept



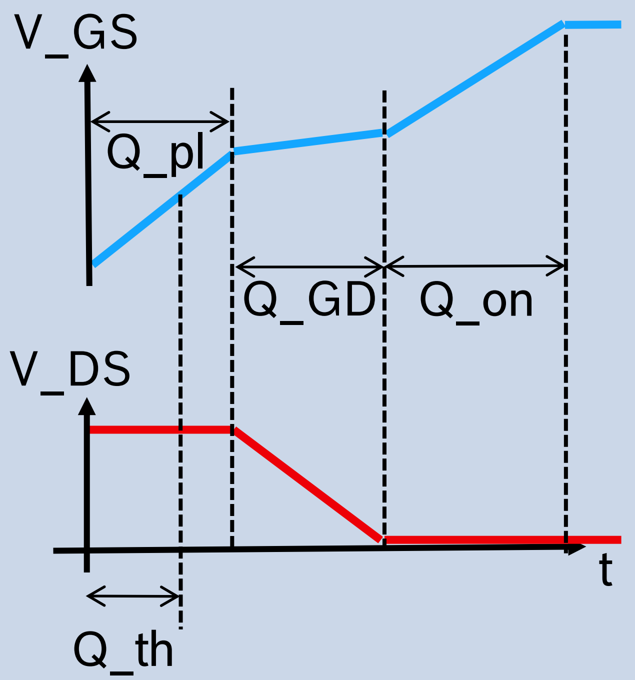
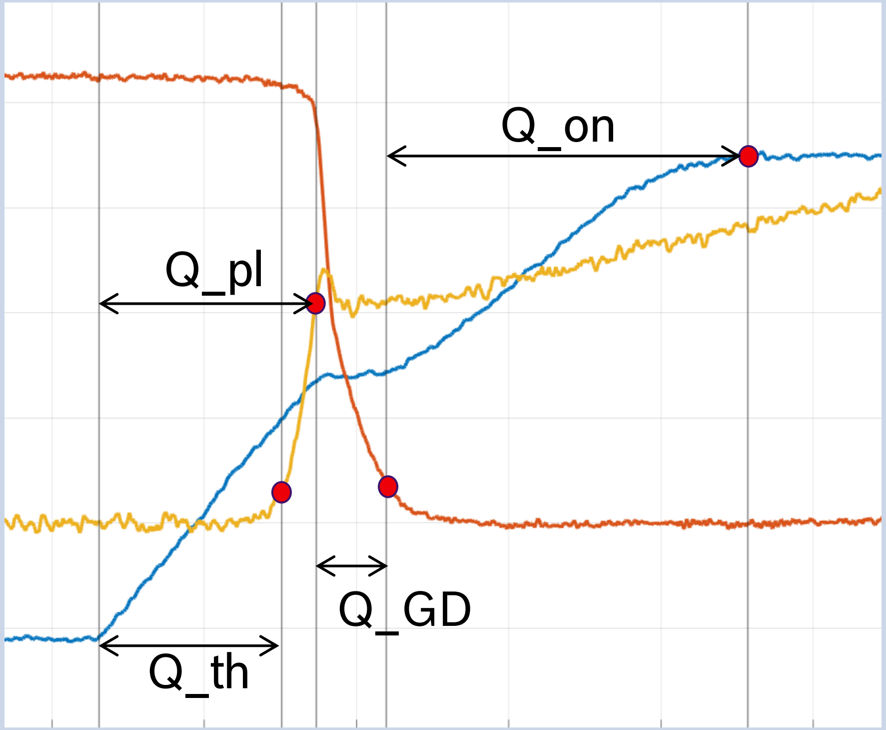
Charge Measurements done on each parallel MOSFET gate individually

Complete chain in future work

Fully used in this work

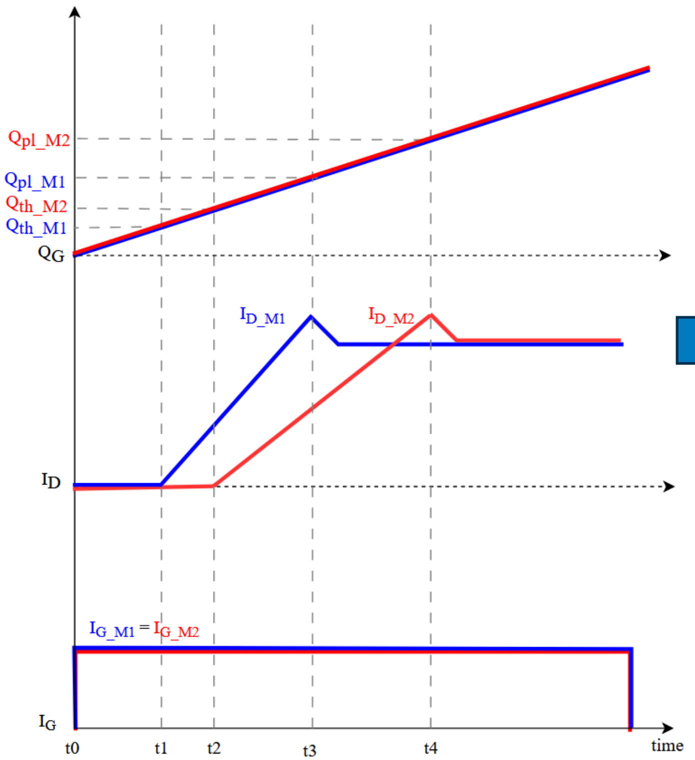
*Embedded PI sensor shown @PCIM Europe 2024 conference & exhibition

Measuring gate charge parameters
Conventional measurement

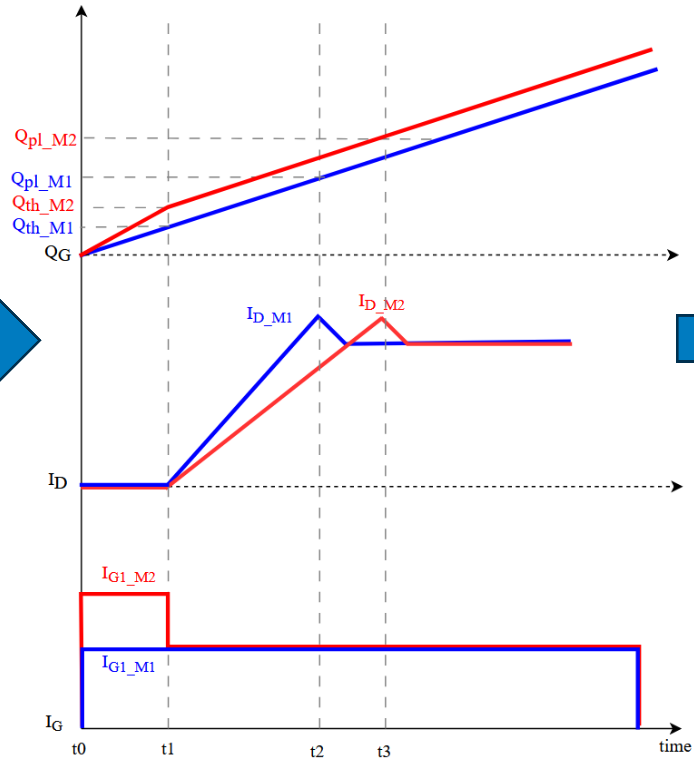
Gate-Charge-model	Oscilloscope measurement data	Parameters & criteria for charge integration
		- Charge till turn-on threshold Q_th: VEE -> I_D ~10% - Charge till Miller-plateau-begin: Q_pl: VEE -> I_D ~100% - Miller-plateau-charge Q_GD: till V_DS ~10% - Charge till full: Q_on: -> V_GS ~99%

Method to define gate current profiles (GS): Turn-on

1. Define a constant charge current for MOSFET M1 as reference profile
2. Adapt current profile for MOSFET M2 to reach the turn on threshold at the same time t1
3. Adapt current profile for MOSFET M2 to reach I_D ~100% at the same time t2

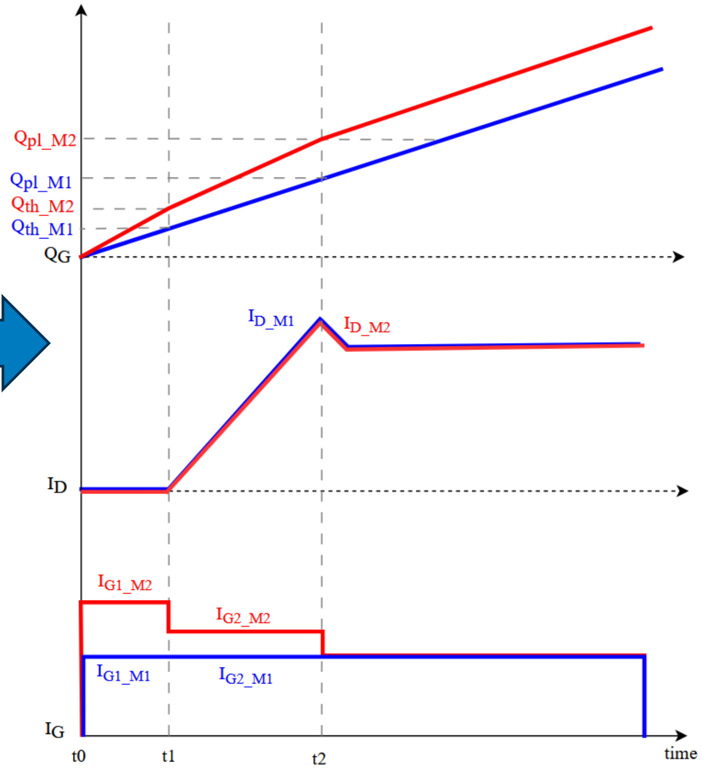


1. Before synchronization



2. Drain-Current edge synchronization

M1 and M2 reach their individual Q_th at the same time

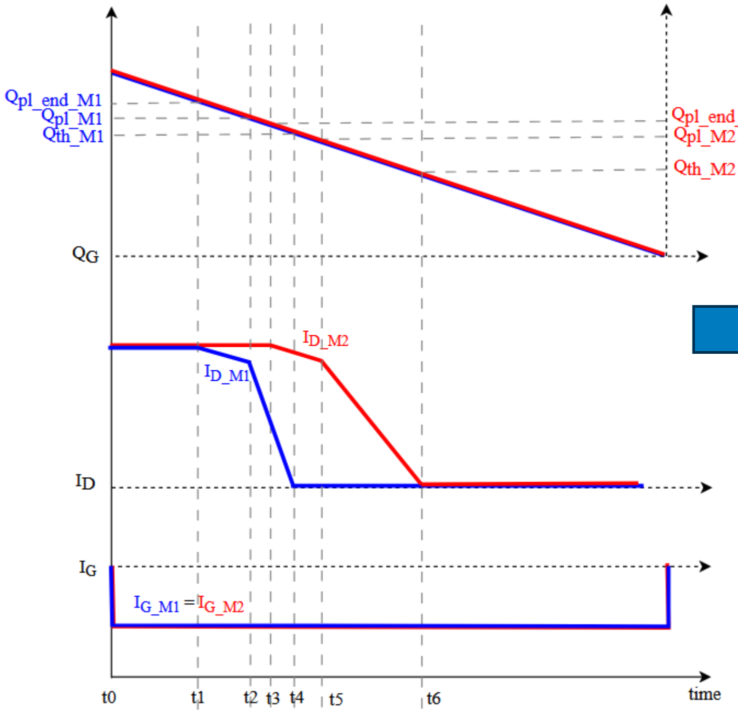


3. Drain-Current slope synchronization

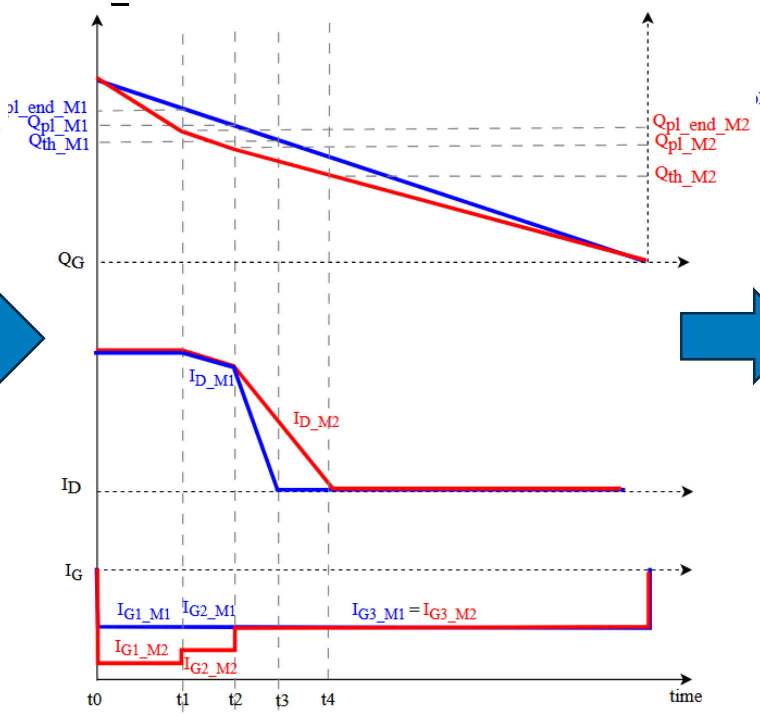
M1 and M2 reach their individual Q_pl at the same time

Method to define gate current profiles (GS): Turn-off

1. Define a constant discharge current for MOSFET M1 as reference profile
2. Adapt current profile for MOSFET M2 to reach Miller-plateau-end at the same time t1
3. Adapt current profile for MOSFET M2 to reach V_DS ~1% at the same time t2
4. Adapt current profile for MOSFET M2 to reach I_D ~1% at the same time t3

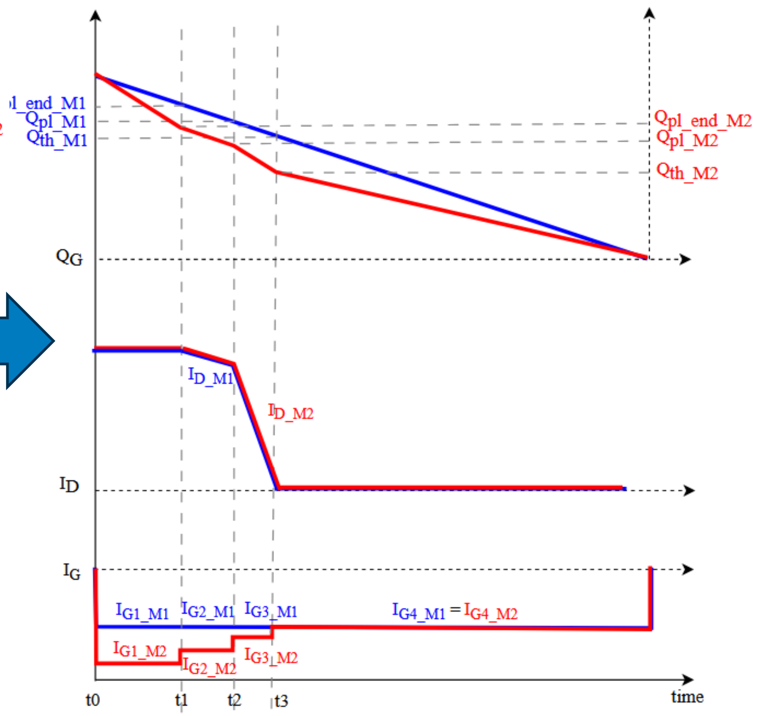


1. Before synchronization



2. & 3. Drain-Current edge synchronization

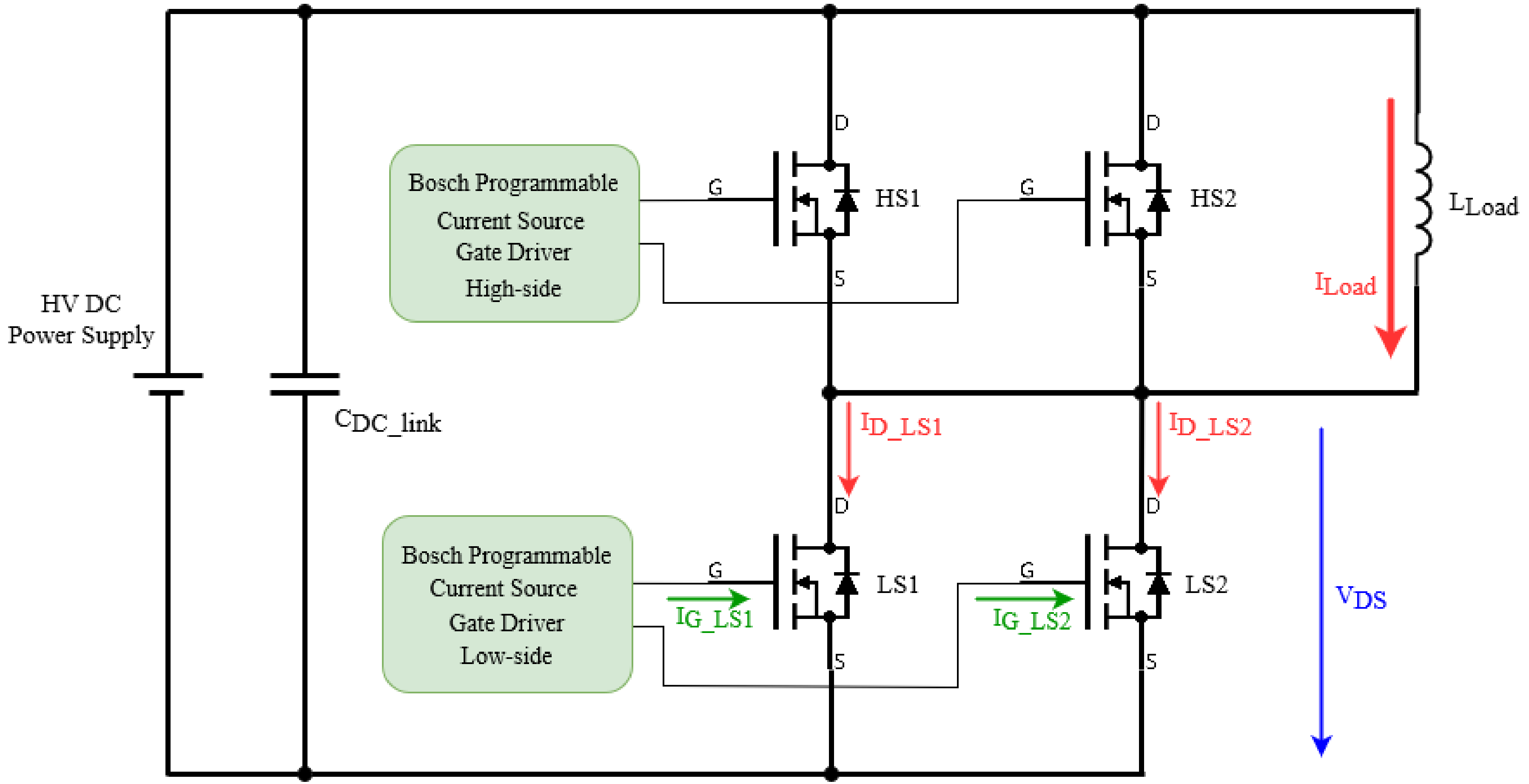
M1 and M2 reach their individual Qpl_end and Qpl at the same time



4. Drain-Current slope synchronization

M1 and M2 reach their individual Qth at the same time

Hardware setup: schematic
Double-pulse test on two parallel LS switches



Hardware setup: HV-double-pulse-test-bench

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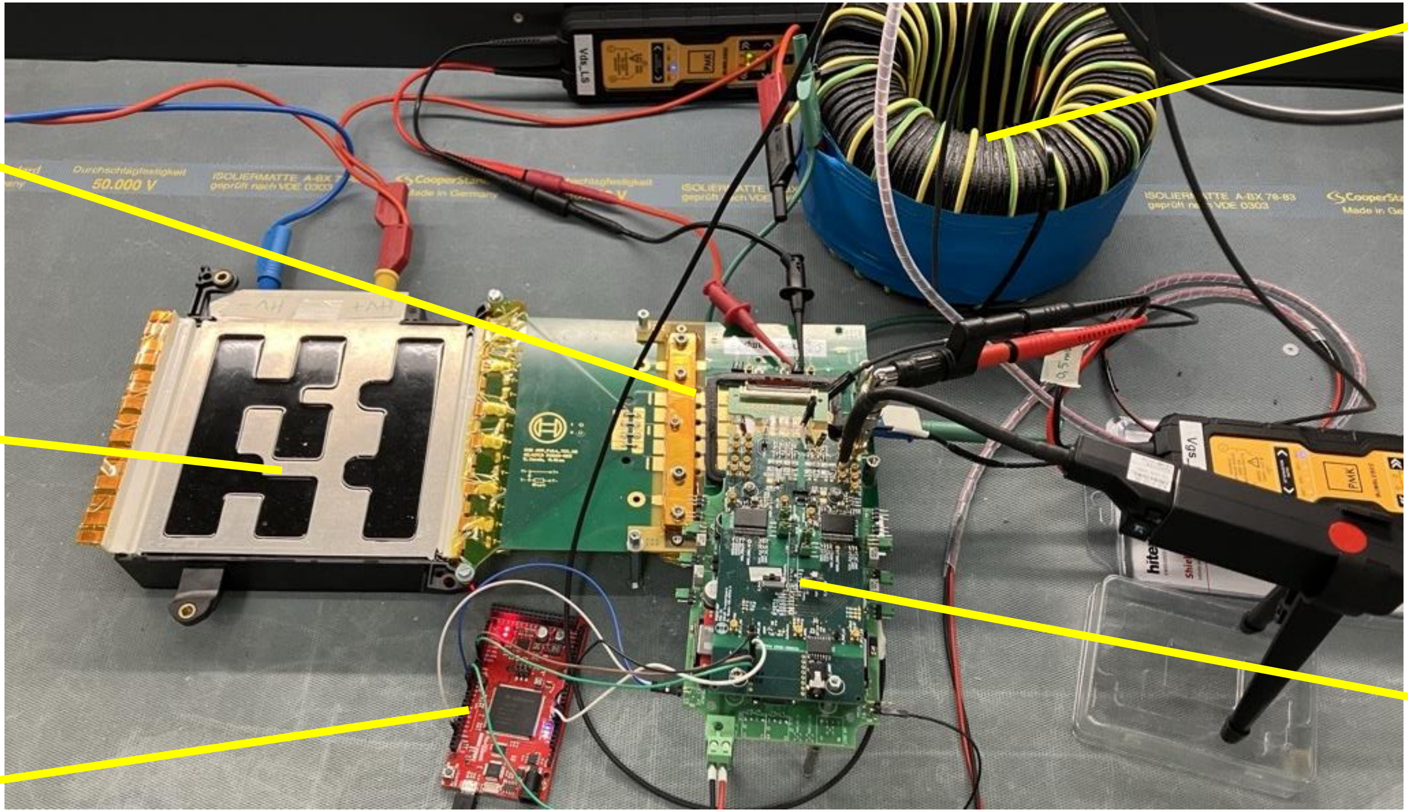
Power Module with paralleled MOSFETs

DCLink Capacitor

Microcontroller (Gatedriver IC Control + DP generator)

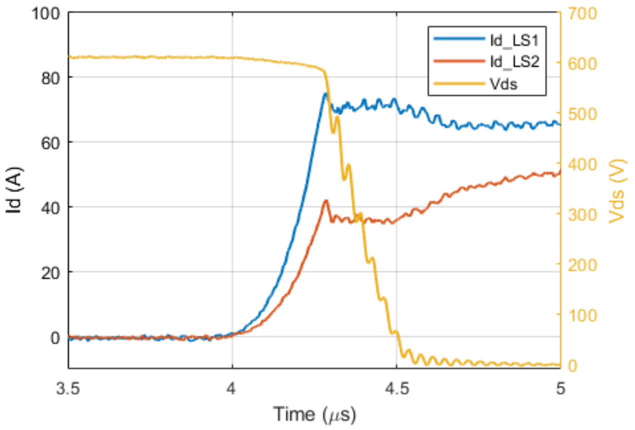


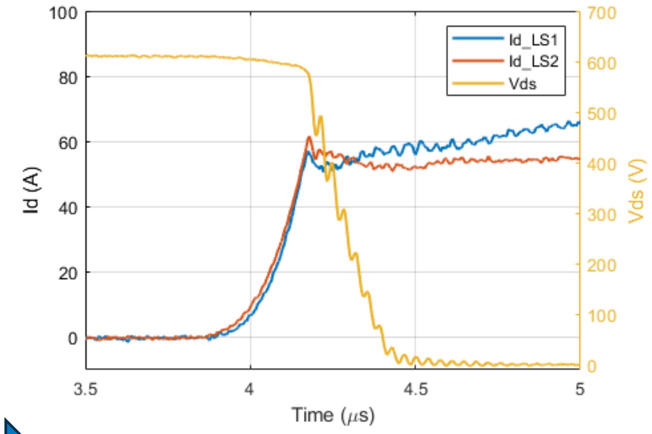
Load inductor

Gate Driver PCB

Lab validation

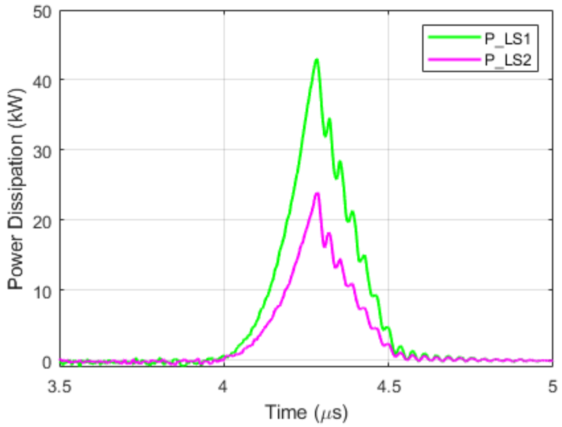
600V, 2*50A, turn-on

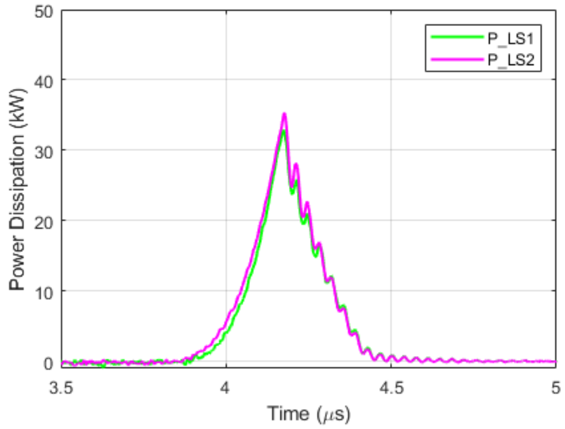




Turn-on w/o

Turn-on with balancing



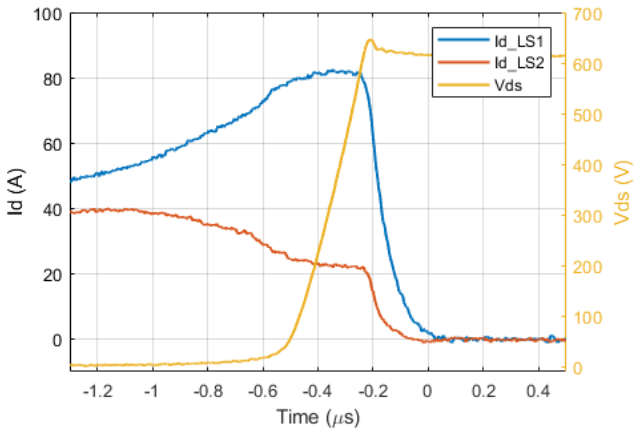


	Without balancing	With balancing
E_{LS1} (mJ)	8.83	6.45
E_{LS2} (mJ)	4.62	6.91
E_{total} (mJ)	13.45	13.36
E_{LS1}:E_{LS2}	66:34	48:52

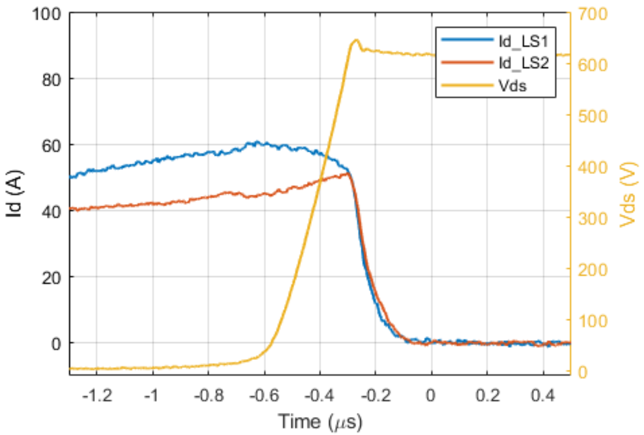
No total turn-on loss reduction but almost perfect balanced stress

Lab validation

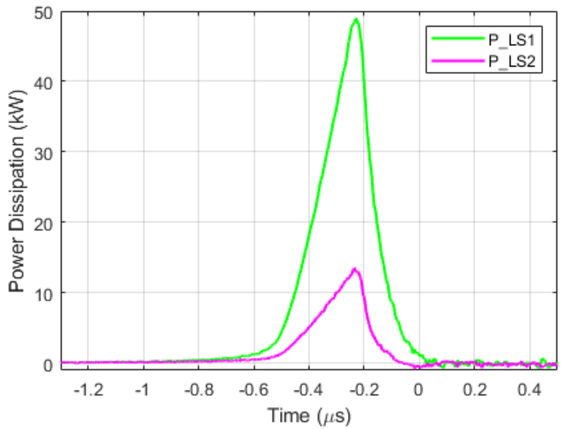
600V, 2*50A, turn-off

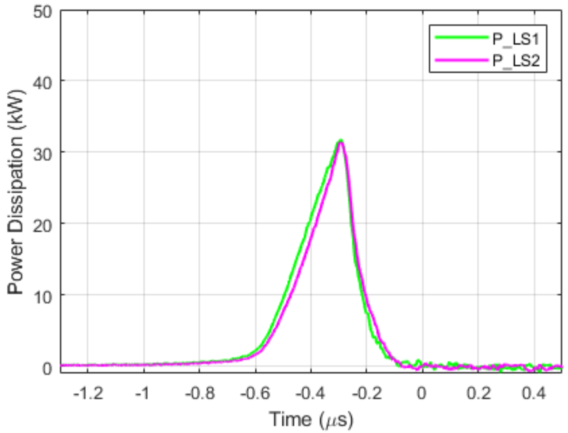


Turn-off w/o



Turn-off with balancing



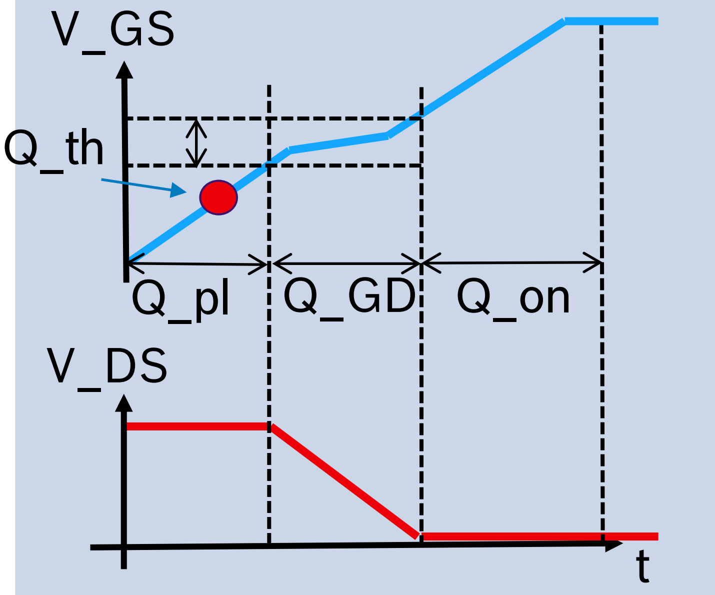


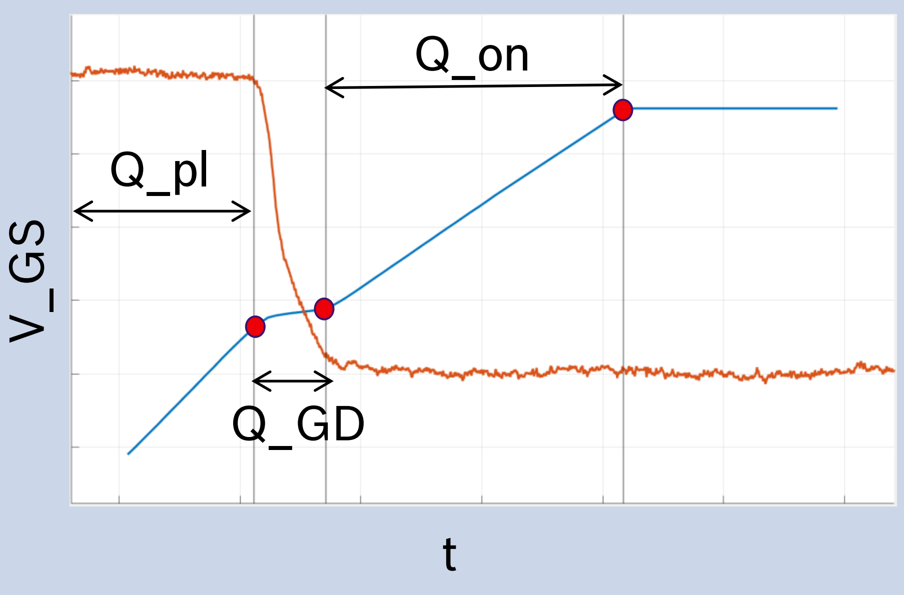
	Without balancing	With balancing
E_{LS1} (mJ)	14.02	7.22
E_{LS2} (mJ)	2.71	6.80
E_{total} (mJ)	16.73	14.02
E_{LS1}:E_{LS2}	84:16	51:49

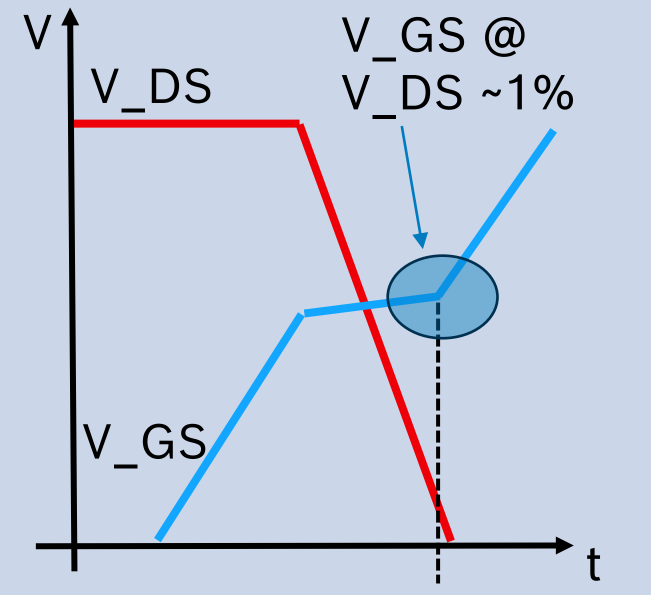
-16% total turn-off loss reduction & almost perfect balanced stress!

Alternative gate charge measurement
Embedded PI sensor - method

Gate-Charge-model suitable for own setup	V_GS Raw-data from sensor ADC	Miller-Plateau-end detection from sensor







Limitations: I_D signal not visible for sensor

=> Calibration of V_GS corridor for Q_pl, Q_GD calculation needed

=> Estimation of Q_th based on measured Q_pl needed

Sensor output characterization

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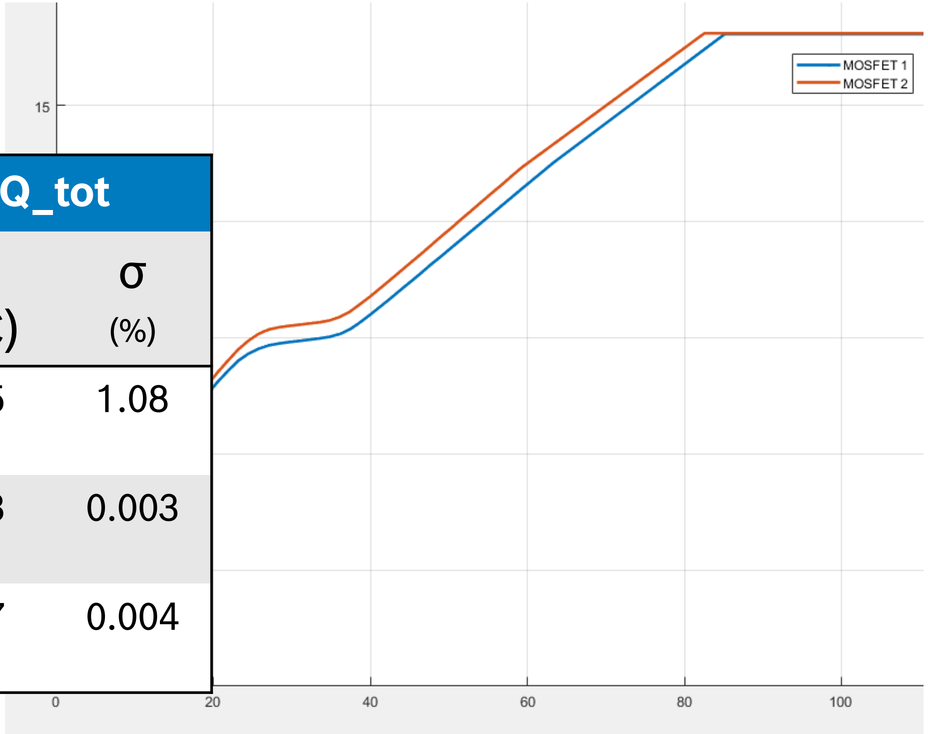
Condition: V_DS 60V; I_D ~0A

	Q_pl		Q_gd		Q_on		Q_tot	
	μ (nC)	σ (%)	μ (nC)	σ (%)	μ (nC)	σ (%)	μ (nC)	σ (%)
OSC (N = 25) on MOSFET 1	47.2	1.58	18.0	2.27	120	1.83	185	1.08
PI on MOSFET 1 (N = 50)	46.4	0.08	16.6	1.24	110	0.19	173	0.003
PI on MOSFET2 (N = 50)	47.6	0.06	13.0	0.97	106	0.13	167	0.004



++ Very good sensor repetition accuracy

\+ Sensor can identify μ differences between MOSFET 1 & 2

\- Remaining deviations between oscilloscope and embedded sensor measurement

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Conclusion & outlook

- We have used gate-shaping as an active gate driving technique to successfully reduce the stress in paralleled MOSFETs due to in-balancing
- The used function for in-balance reduction could be combined with algorithm to minimize also E_SW_tot in future
- An embedded gate charge measurement sensor has been characterized to replace the offline oscilloscope measurement in a future work once being better calibrated
- Want to have more insights now?

Please join us at PCIM exhibition
Hall 11, booth E40

Thanks for your attention!