

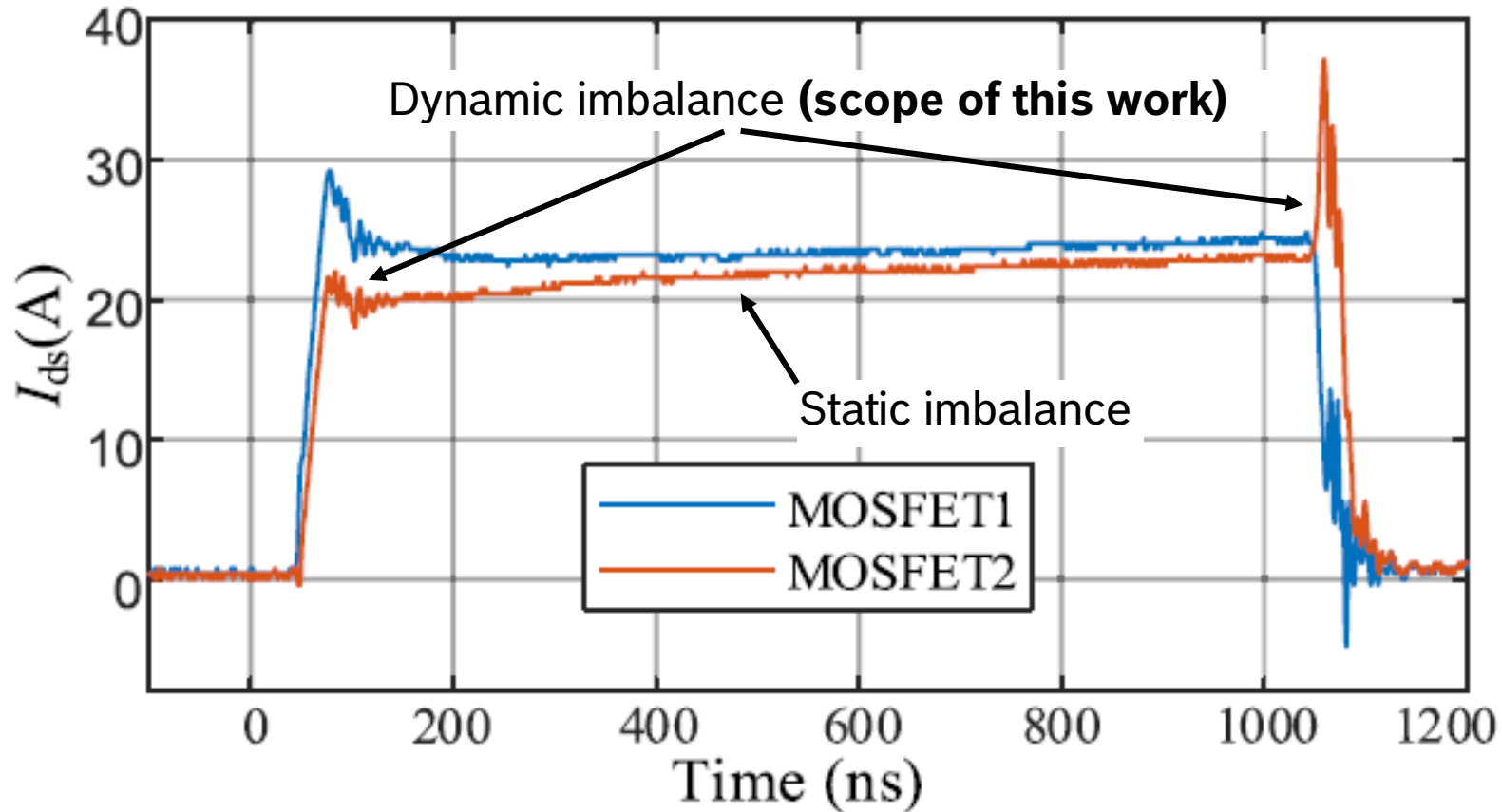
Optimize Switching Transient of Paralleled SiC-MOSFETs by Using Adaptive Gate Current Shaping

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Agenda

- Problem description & possible solutions
- Concept of this work: adaptive gate current shaping
- Measuring gate charge parameters (2 methods)
- Defining gate drive strength profiles
- Double pulse characterization test
- Alternative gate charge measurement characterization
- Conclusion & Outlook

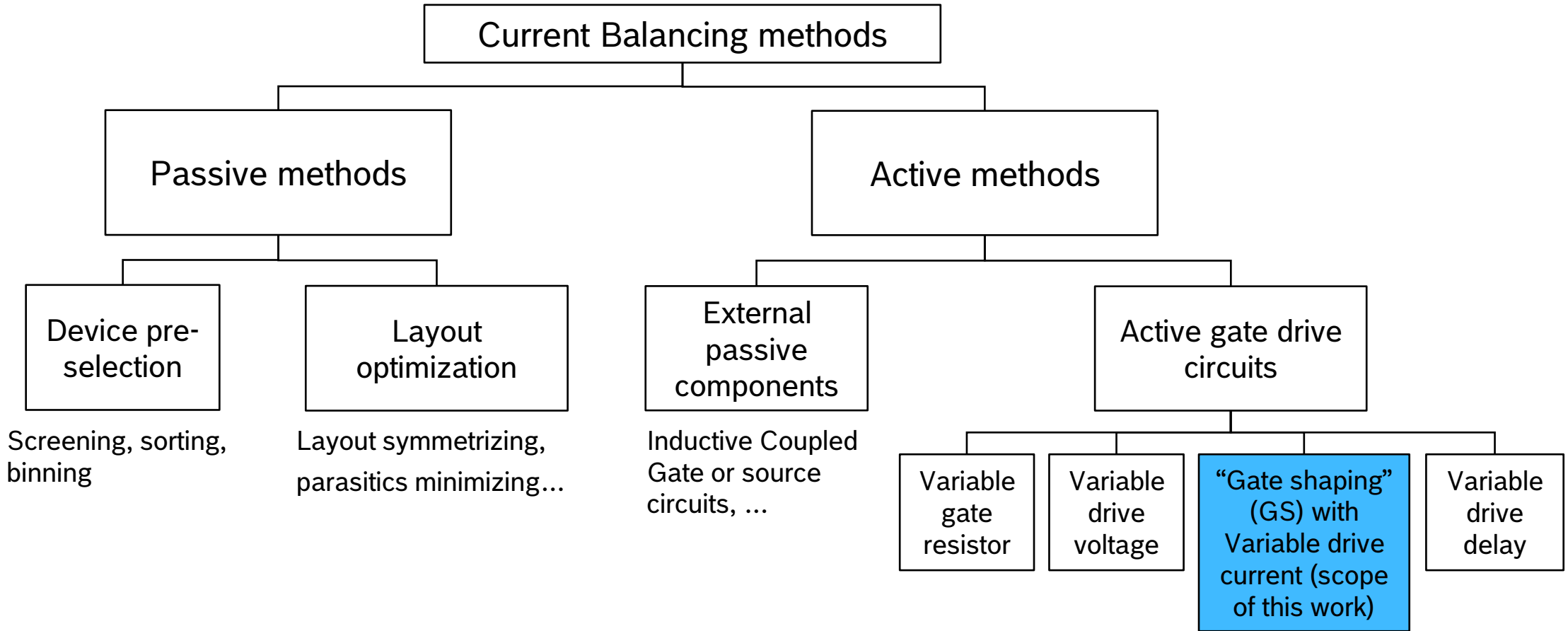
Problem description



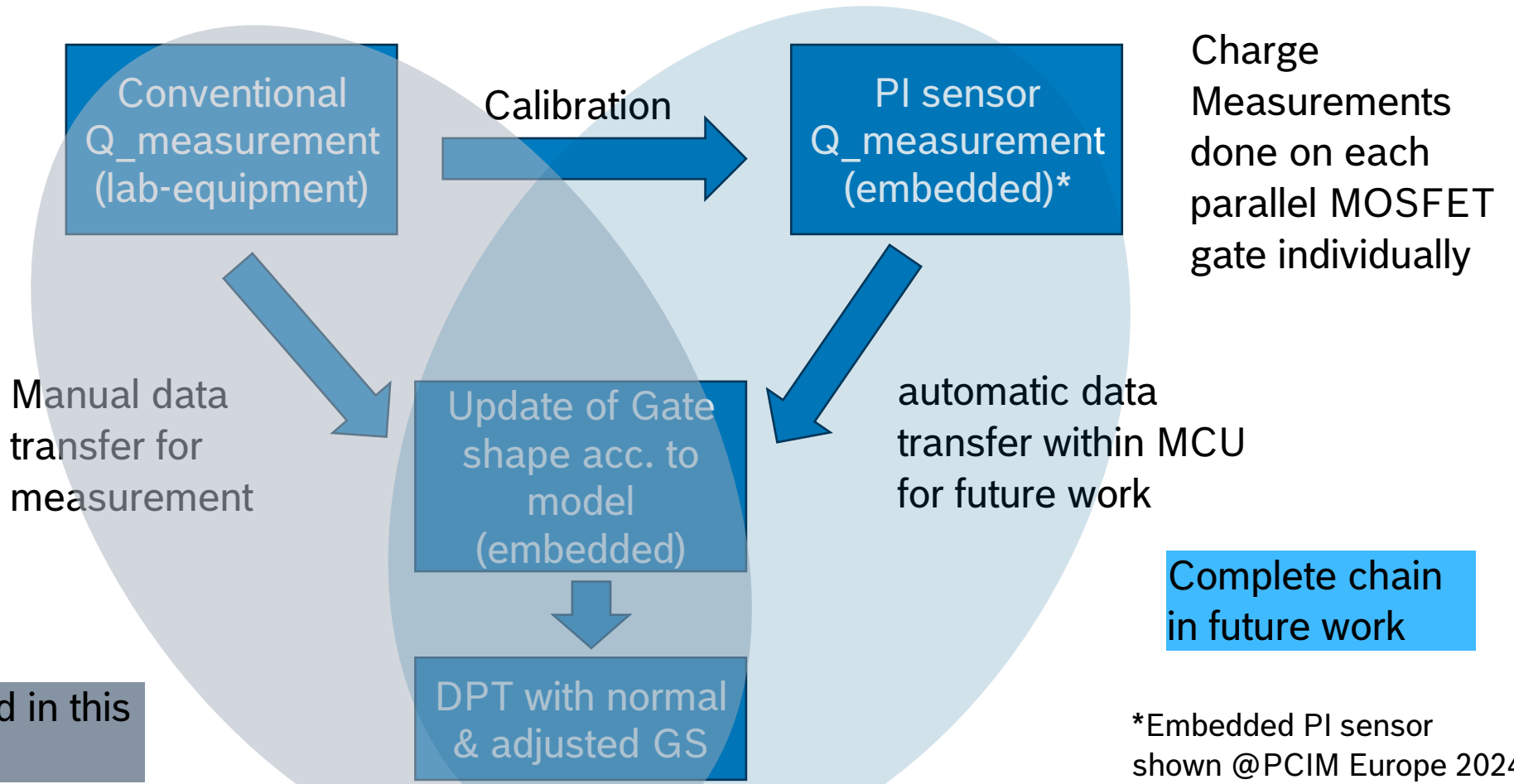
Resulting in huge variation of **switching losses (requires oversizing), overshoots and EME & increased component stress**

State of the art

Possible solutions



Adaptive gate current shaping Concept



Charge Measurements done on each parallel MOSFET gate individually

Fully used in this work

*Embedded PI sensor shown @PCIM Europe 2024 conference & exhibition

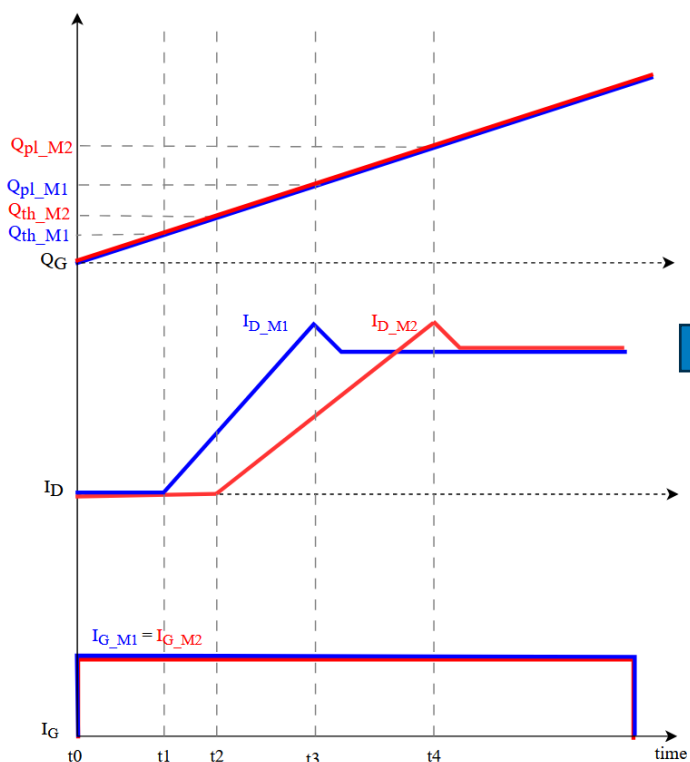
Measuring gate charge parameters

Conventional measurement

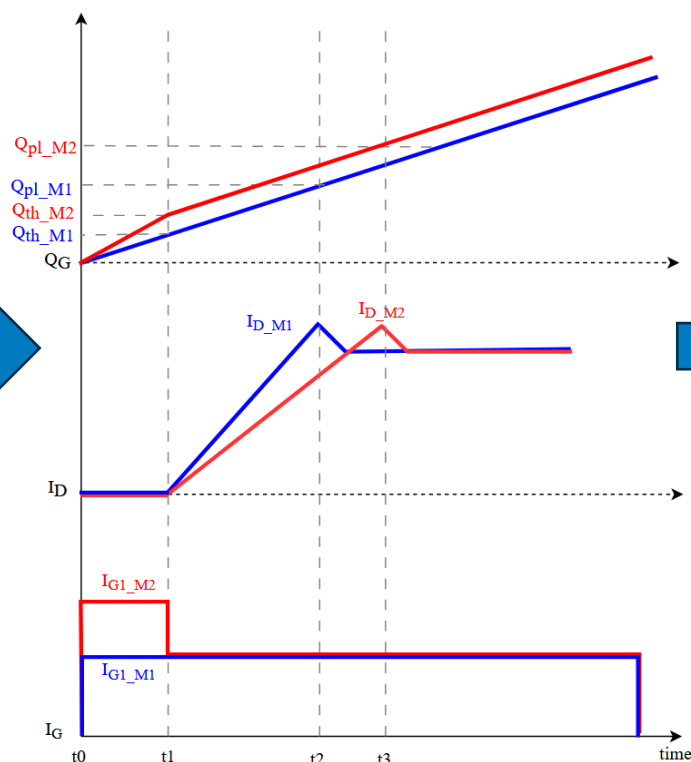
Gate-Charge-model	Oscilloscope measurement data	Parameters & criteria for charge integration
<p>The diagram shows two waveforms over time t. The top waveform is V_{GS} (blue), which starts at a low level, rises linearly through a region labeled Q_{pl} (Miller plateau), then continues to rise through a region labeled Q_{GD} (Miller plateau charge), and finally rises linearly through a region labeled Q_{on}. The bottom waveform is V_{DS} (red), which is constant at a high level during the Q_{pl} and Q_{GD} regions, then drops linearly to zero during the Q_{on} region. Vertical dashed lines mark the boundaries of these regions. Red dots on the V_{GS} waveform indicate the start of Q_{pl}, the end of Q_{GD}, and the end of Q_{on}. A horizontal double-headed arrow labeled Q_{th} indicates the time from the start of V_{GS} to the start of Q_{pl}.</p>	<p>The oscilloscope data shows three waveforms: V_{GS} (blue), V_{DS} (red), and I_D (yellow). The V_{GS} waveform shows a Miller plateau, a Miller plateau charge region, and a linear region. The V_{DS} waveform shows a high voltage during the Miller plateau and Q_{GD} regions, then drops to zero during the Q_{on} region. The I_D waveform shows a sharp peak during the Q_{on} region. Red dots on the V_{GS} waveform mark the start of Q_{pl}, the end of Q_{GD}, and the end of Q_{on}. Horizontal arrows labeled Q_{th}, Q_{pl}, Q_{GD}, and Q_{on} indicate the duration of these regions.</p>	<ul style="list-style-type: none"> - Charge till turn-on threshold Q_{th}: VEE \rightarrow $I_D \sim 10\%$ - Charge till Miller-plateau-begin: Q_{pl}: VEE \rightarrow $I_D \sim 100\%$ - Miller-plateau-charge Q_{GD}: till $V_{DS} \sim 10\%$ - Charge till full: Q_{on}: \rightarrow $V_{GS} \sim 99\%$

Method to define gate current profiles (GS): Turn-on

1. Define a constant charge current for MOSFET M1 as reference profile
2. Adapt current profile for MOSFET M2 to reach the turn on threshold at the same time t_1
3. Adapt current profile for MOSFET M2 to reach $I_D \sim 100\%$ at the same time t_2

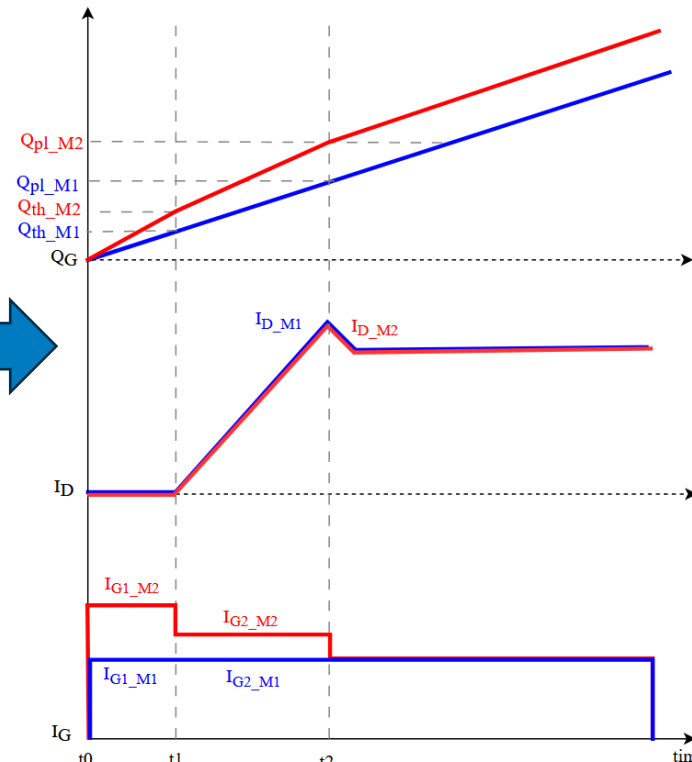


1. Before synchronization



2. Drain-Current edge synchronization

M1 and M2 reach their individual Q_{th} at the same time

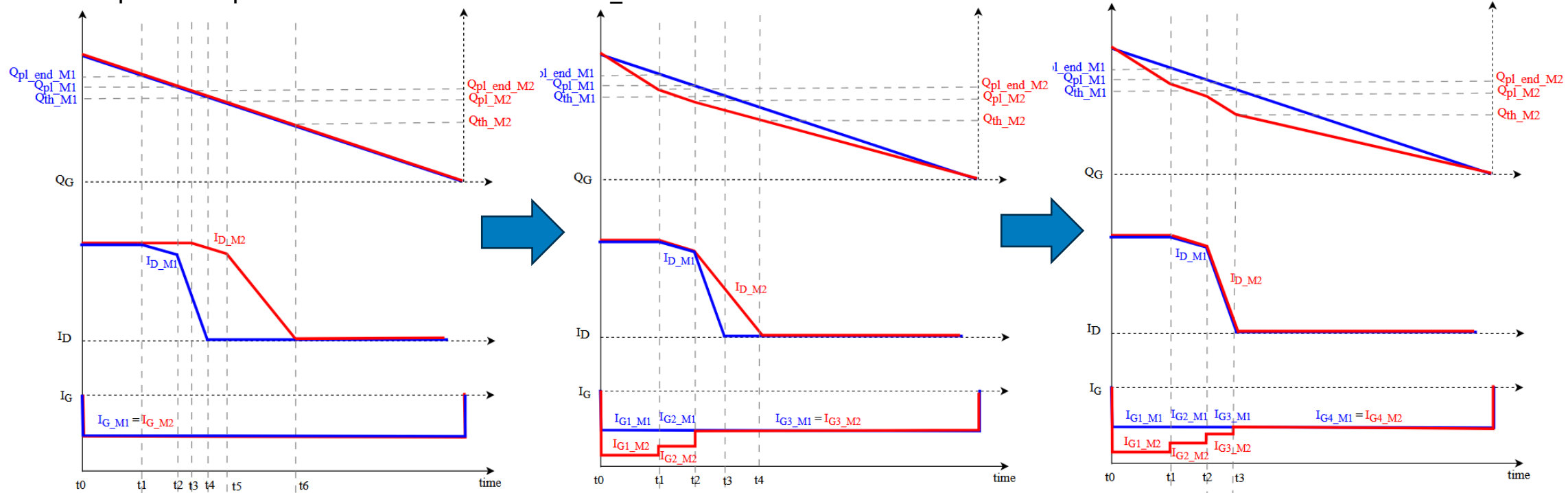


3. Drain-Current slope synchronization

M1 and M2 reach their individual Q_{pl} at the same time

Method to define gate current profiles (GS): Turn-off

1. Define a constant discharge current for MOSFET M1 as reference profile
2. Adapt current profile for MOSFET M2 to reach Miller-plateau-end at the same time t_1
3. Adapt current profile for MOSFET M2 to reach $V_{DS} \sim 1\%$ at the same time t_2
4. Adapt current profile for MOSFET M2 to reach $I_D \sim 1\%$ at the same time t_3



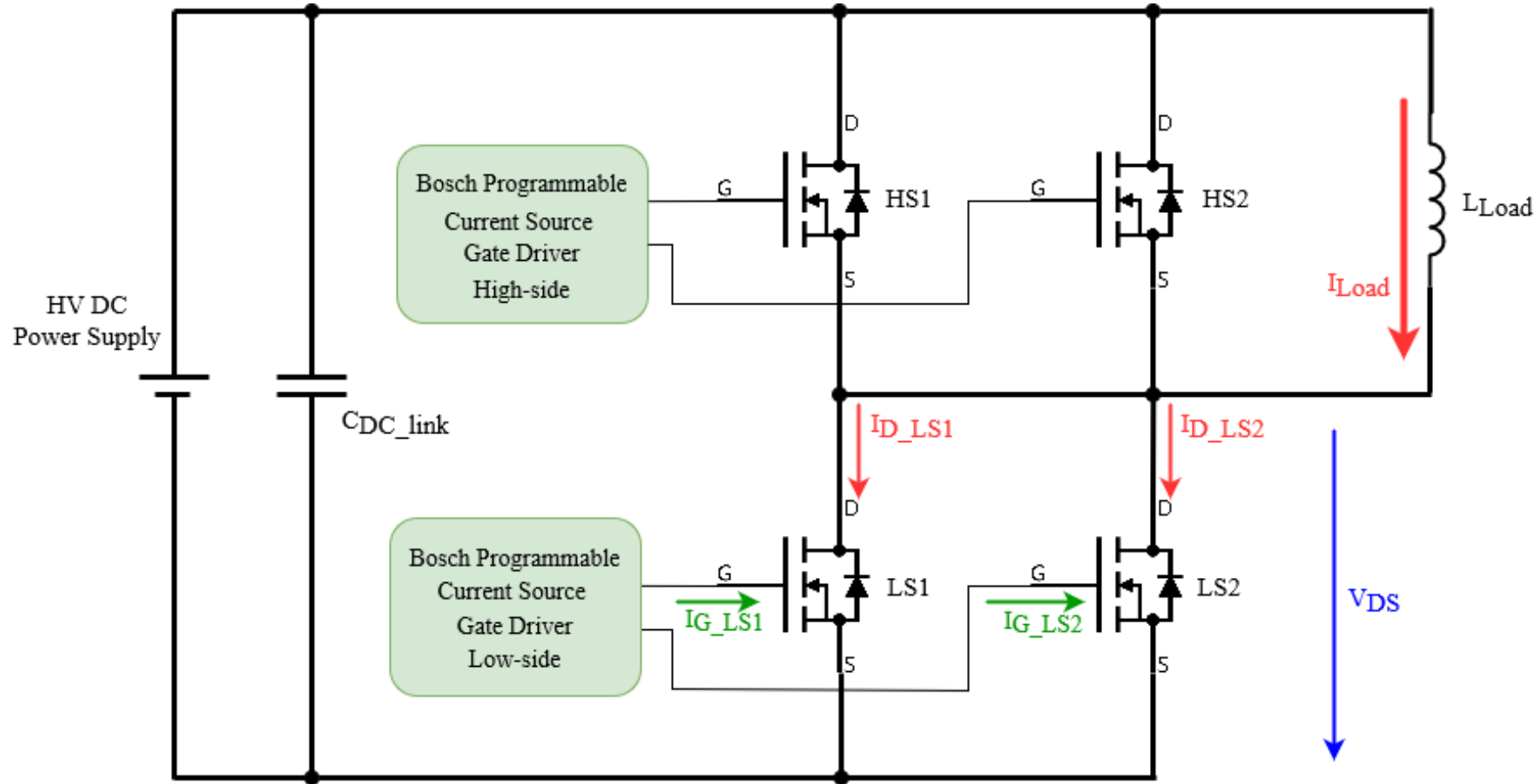
1. Before synchronization

2. & 3. Drain-Current edge synchronization
M1 and M2 reach their individual Q_{pl_end} and Q_{pl} at the same time

4. Drain-Current slope synchronization
M1 and M2 reach their individual Q_{th} at the same time

Hardware setup: schematic

Double-pulse test on two parallel LS switches

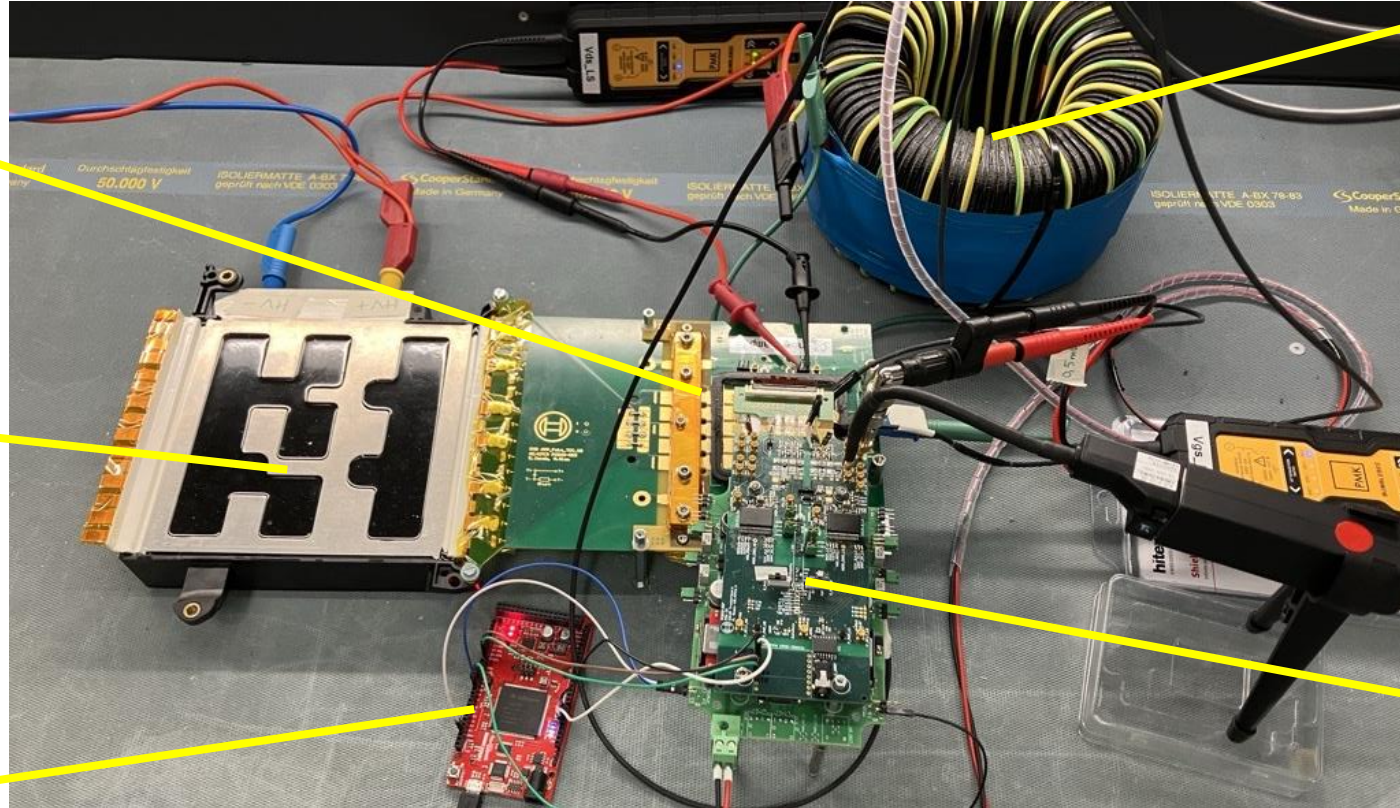


Hardware setup: HV-double-pulse-test-bench

Power Module
with paralleled
MOSFETs

DCLink Capacitor

Microcontroller
(Gatedriver IC
Control + DP
generator)

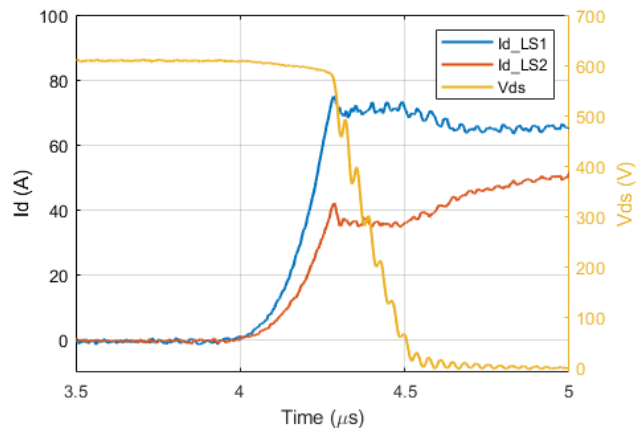


Load inductor

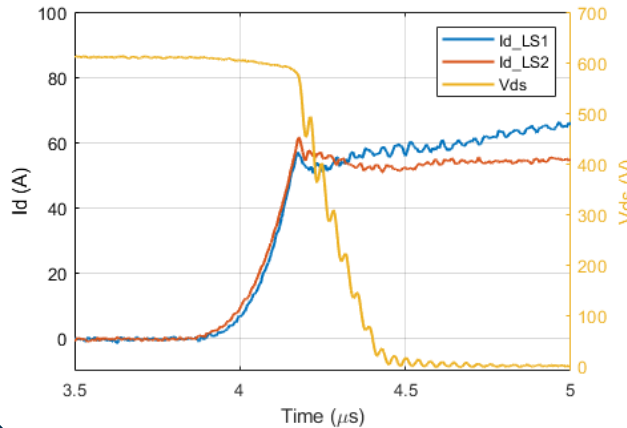
Gate Driver
PCB

Lab validation

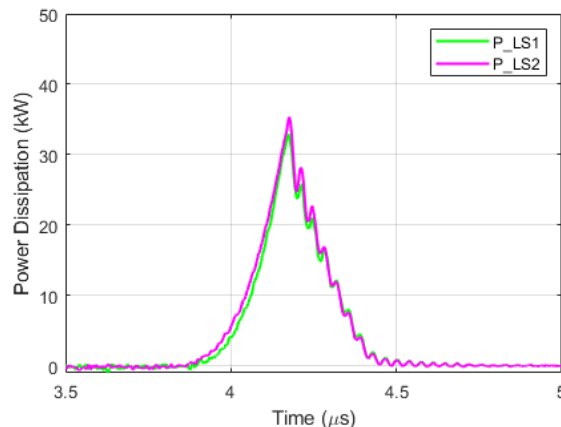
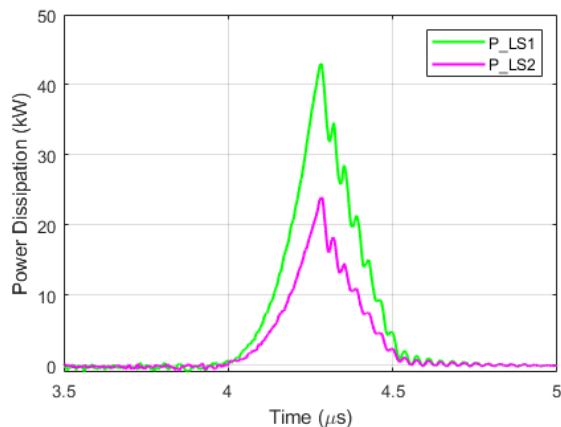
600V, 2*50A, turn-on



Turn-on w/o



Turn-on with balancing

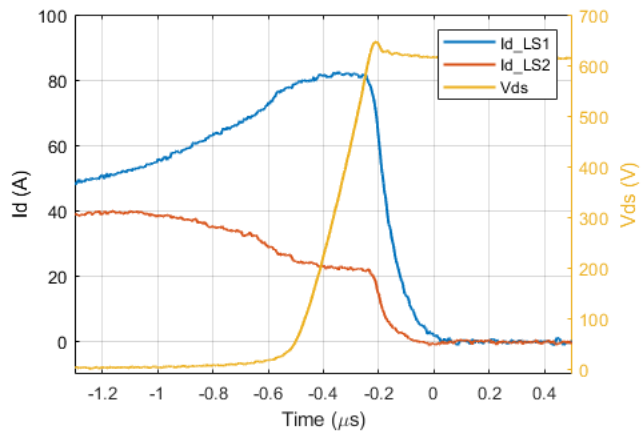


	Without balancing	With balancing
E_{LS1} (mJ)	8.83	6.45
E_{LS2} (mJ)	4.62	6.91
E_{total} (mJ)	13.45	13.36
$E_{LS1}:E_{LS2}$	66:34	48:52

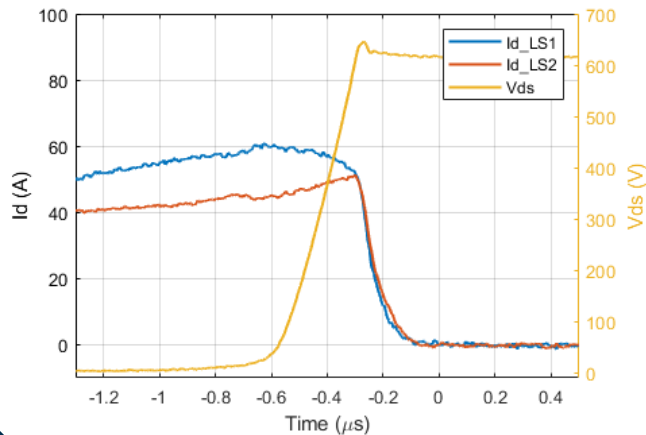
No total turn-on loss reduction
but almost perfect balanced
stress

Lab validation

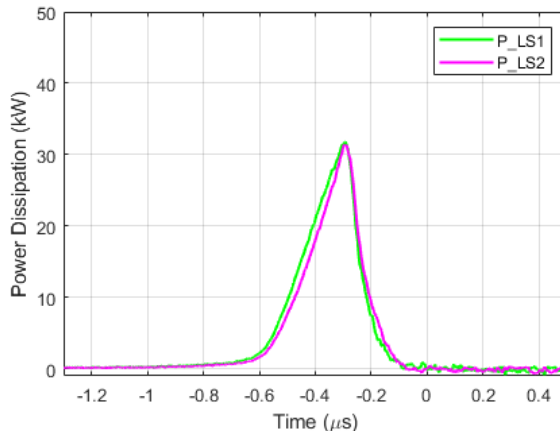
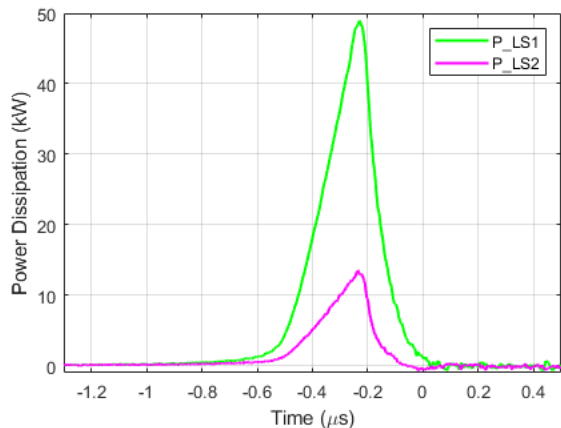
600V, 2*50A, turn-off



Turn-off w/o



Turn-off with balancing

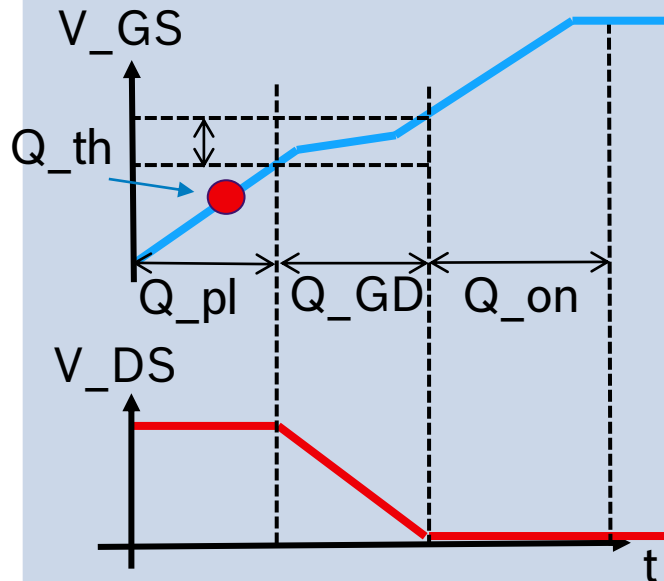


	Without balancing	With balancing
E_{LS1} (mJ)	14.02	7.22
E_{LS2} (mJ)	2.71	6.80
E_{total} (mJ)	16.73	14.02
$E_{LS1}:E_{LS2}$	84:16	51:49

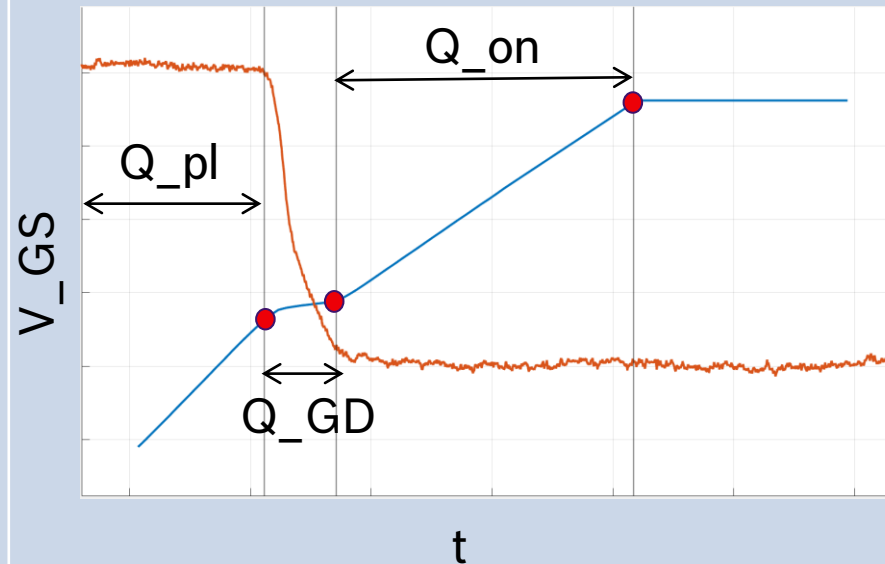
-16% total turn-off loss reduction & almost perfect balanced stress!

Alternative gate charge measurement Embedded PI sensor - method

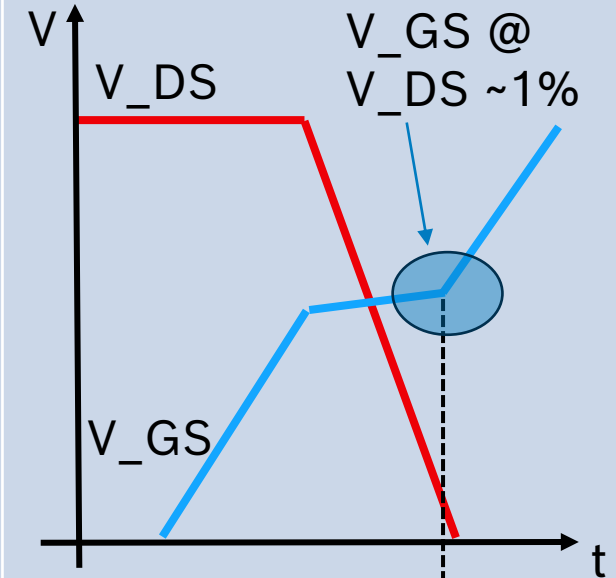
Gate-Charge-model suitable for own setup



V_{GS} Raw-data from sensor ADC



Miller-Plateau-end detection from sensor



Limitations: I_D signal not visible for sensor

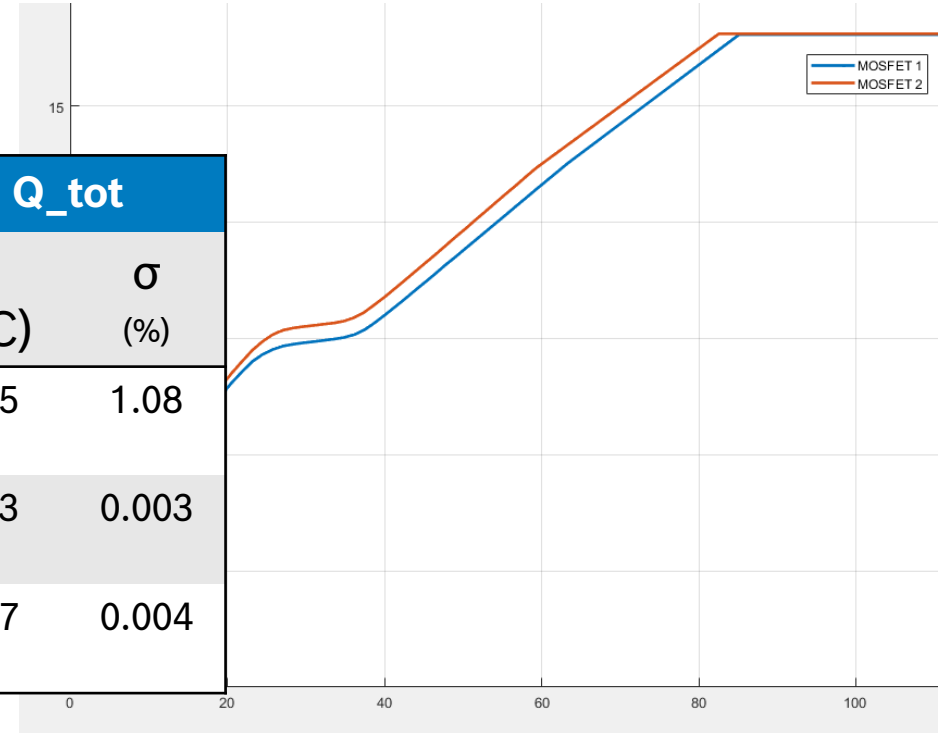
=> Calibration of V_{GS} corridor for Q_{pl} , Q_{GD} calculation needed

=> Estimation of Q_{th} based on measured Q_{pl} needed

Sensor output characterization

Condition: V_{DS} 60V; $I_D \sim 0A$

	Q _{pl}		Q _{gd}		Q _{on}		Q _{tot}	
	μ (nC)	σ (%)	μ (nC)	σ (%)	μ (nC)	σ (%)	μ (nC)	σ (%)
OSC (N = 25) on MOSFET 1	47.2	1.58	18.0	2.27	120	1.83	185	1.08
PI on MOSFET 1 (N = 50)	46.4	0.08	16.6	1.24	110	0.19	173	0.003
PI on MOSFET2 (N = 50)	47.6	0.06	13.0	0.97	106	0.13	167	0.004



- ++ Very good sensor repetition accuracy
- + Sensor can identify μ differences between MOSFET 1 & 2
- Remaining deviations between oscilloscope and embedded sensor measurement

Conclusion & outlook

- We have used gate-shaping as an active gate driving technique to successfully reduce the stress in paralleled MOSFETs due to in-balancing
- The used function for in-balance reduction could be combined with algorithm to minimize also E_{SW_tot} in future
- An embedded gate charge measurement sensor has been characterized to replace the offline oscilloscope measurement in a future work once being better calibrated
- Want to have more insights now?



Please join us at PCIM exhibition
Hall 11, booth E40

Thanks for your attention!