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New 400 V SiC MOSFET technology delivering highest efficiency in three-level industrial drive applications

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Presentation outline

1. Introduction of the 400 V CoolSiC™ Trench MOSFET technology
2. 400 V CoolSiC™ MOSFET properties and benefits
3. Device performance in 3-Level ANPC inverter
4. Outlook: device performance in 3-Level PFC
5. Summary and Conclusion

Introduction of the 400 V CoolSiC™ Trench MOSFET technology

Silicon-carbide is not Silicon

Device design addresses material-specific properties

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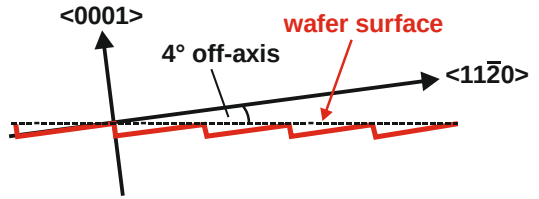
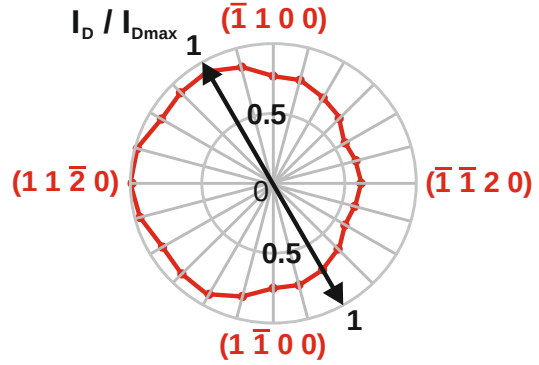
– epitaxial layers must be grown off-axis to gain sufficient control of the doping level
– this leads to a rough surface and a mix of different crystal faces with different properties

➡ **use a trench rather than a planar gate and align to an undisturbed crystal face**



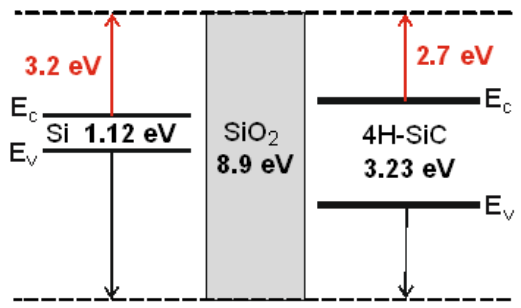
– hexagonal lattice leads to anisotropic crystal properties
– as consequence channel mobility, threshold voltage, interface charge density depend on the crystal plane

➡ **use asymmetric channel and align to a-plane for high channel mobility**



– SiC shows larger Fowler-Nordheim tunneling through gate oxide due to the larger bandgap of SiC
– breakdown in SiC occurs at much higher electric fields, causing also higher fields and consequently shorter oxide lifetime of the gate oxide

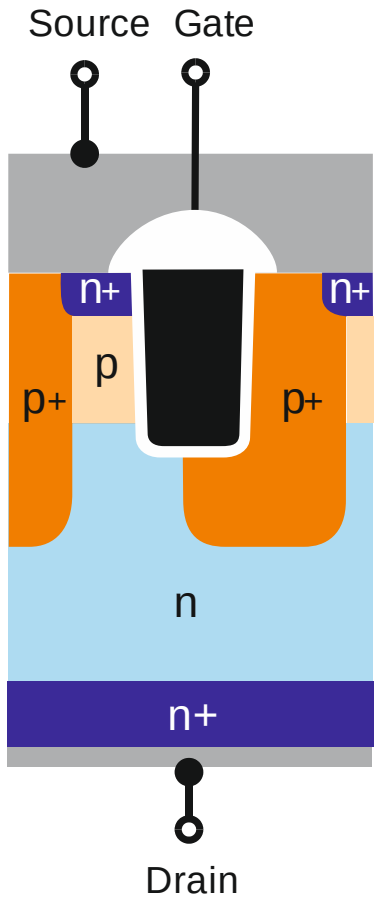
➡ **p+ type shielding regions below the trench limit electric field in the gate oxide**



400 V Cell design

Built on continouos technology advancements

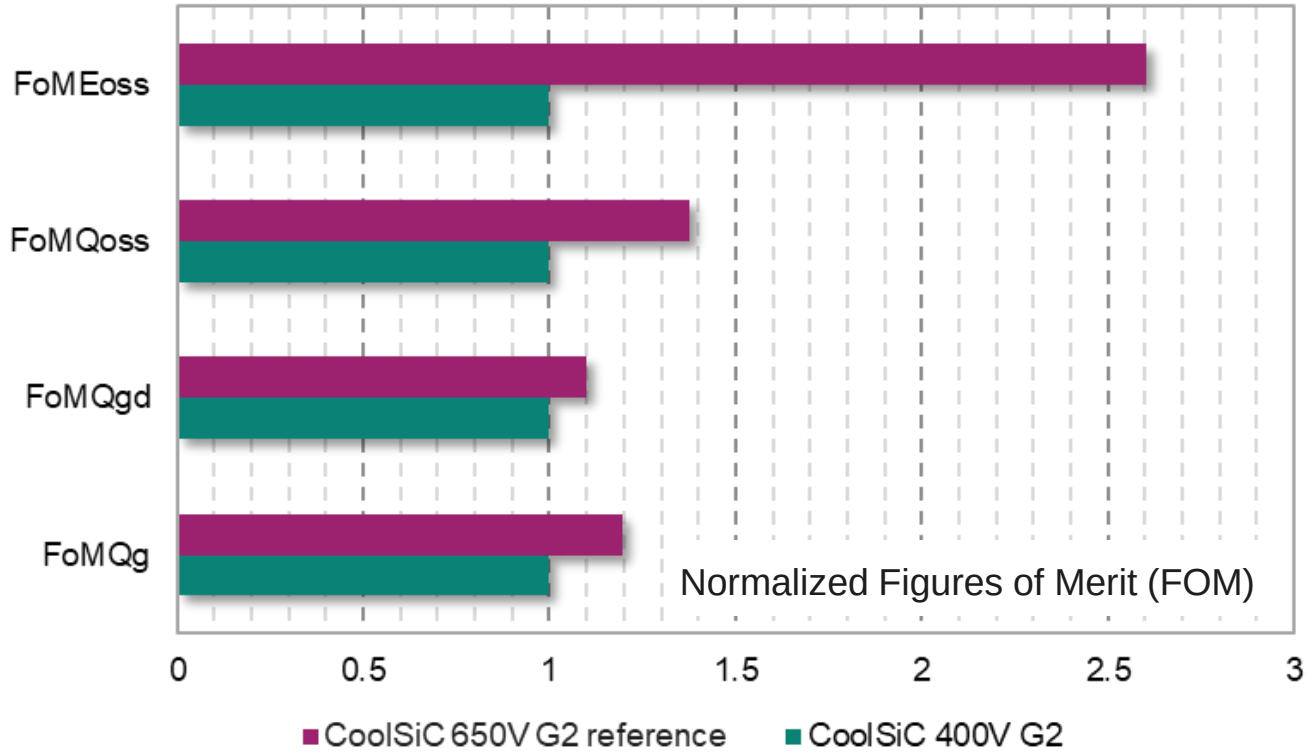
- the 400 V SiC MOSFET cell structure is based on the design of the already released higher voltage classes (as depicted exemplary)
- the significant performance improvements are gained by
  - further reduced cell pitch
  - refined channel properties
  - enhanced control over drift region properties
  - optimization of chip design to minimize losses of active area



400 V CoolSiC™ MOSFET properties and benefits

Excellent switching FOMs

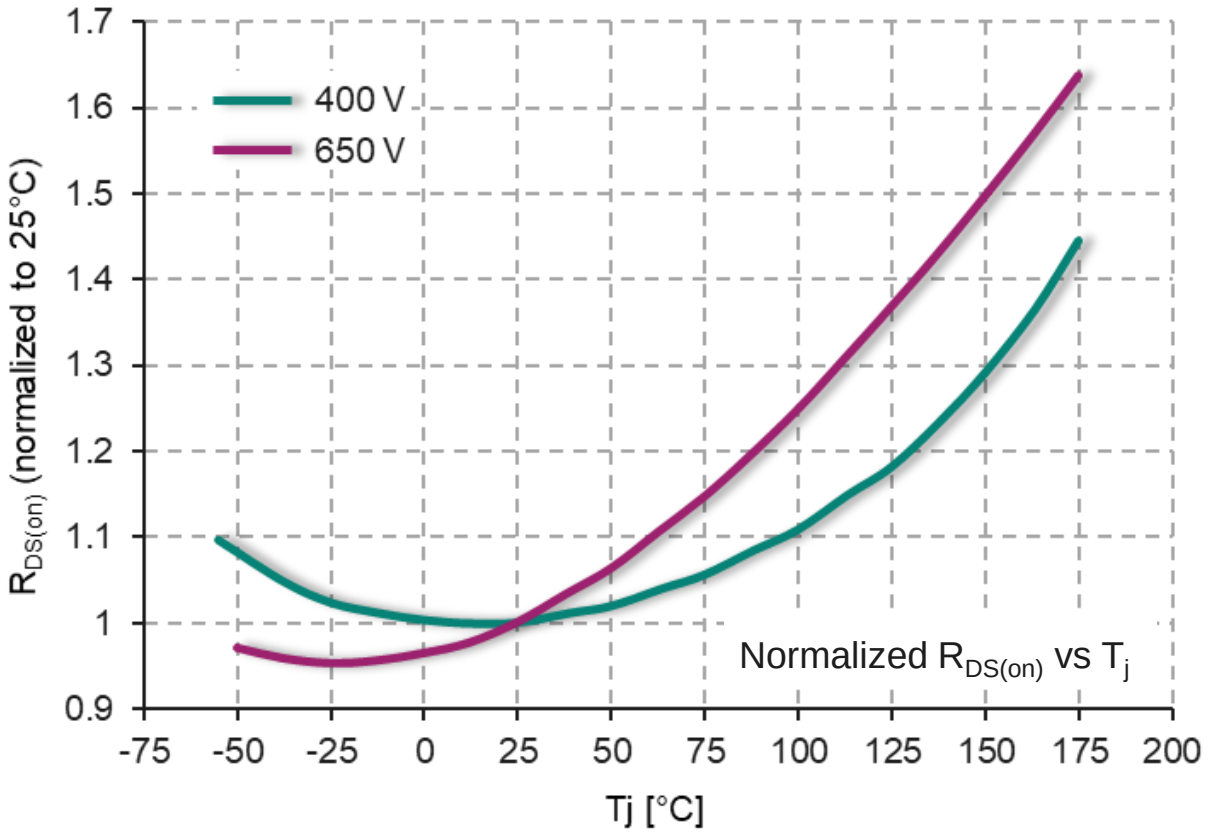
- optimization of CoolSiC G2 for a lower breakdown voltage of 400 V results in excellent FoM improvements compared to the 650 V reference
- CoolSiC 400V G2 is the best-fit for a wide range of applications, including 3L-ANPC inverters for drives and solar or AI Server PSUs, with bus voltages of ≤ 300 V in 2L topologies and ≤ 600 V in 3L topologies



FOMs defined at V_{DS} = 200 V for 400 V SiC and at V_{DS} = 400 V for 650 V SiC reference part

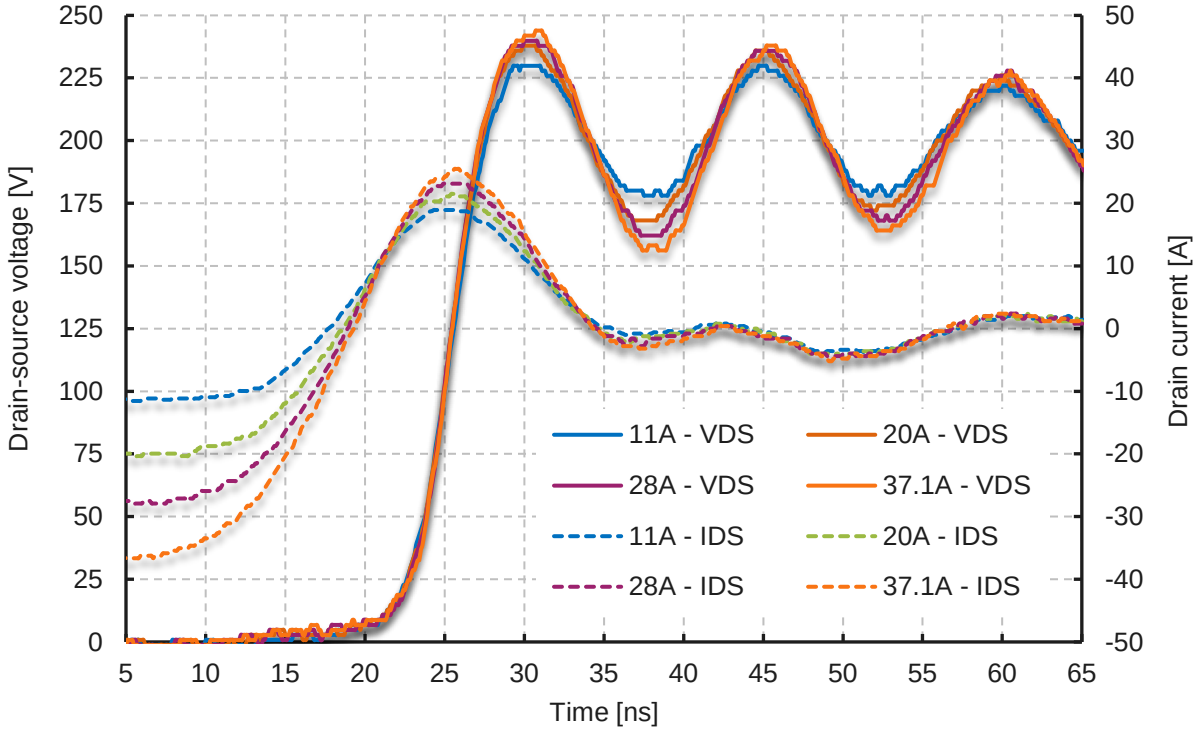
Flat temperature dependence of on-resistance

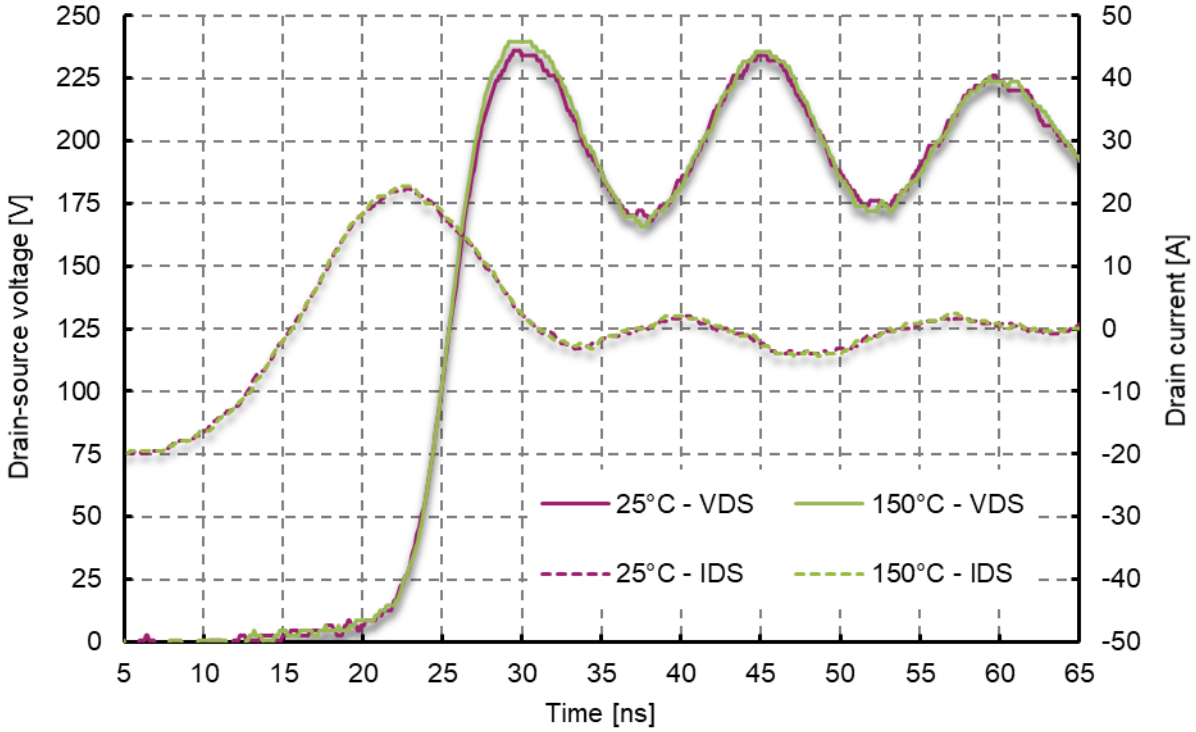
- the on-resistance of the 400 V device increases only by 11% with temperature rise from 25°C to 100°C
- flat $R_{DS(on)}$ vs T_j characteristics enables the use of MOSFETs with higher $R_{DS(on),typ}$, which is linked to lower costs and better switching performance



Commutation ruggedness of body diode

- double pulse characterization of 11 mΩ device (IMT40R011M2H)
- device shows stable switching waveforms with small overshoots and little ringing
- commutation behavior is almost independent of load current and operating temperature

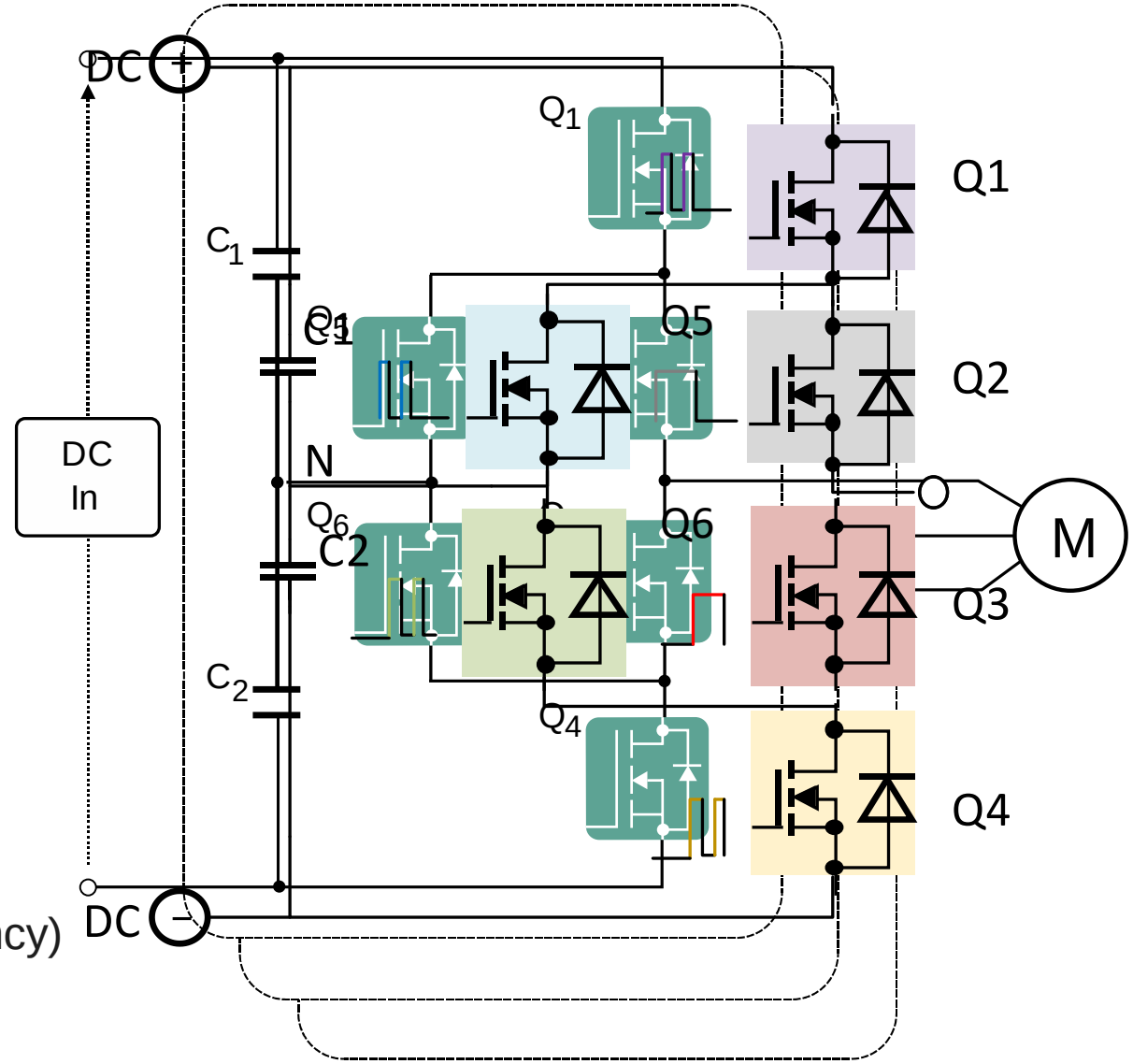




Device performance in 3-Level ANPC inverter

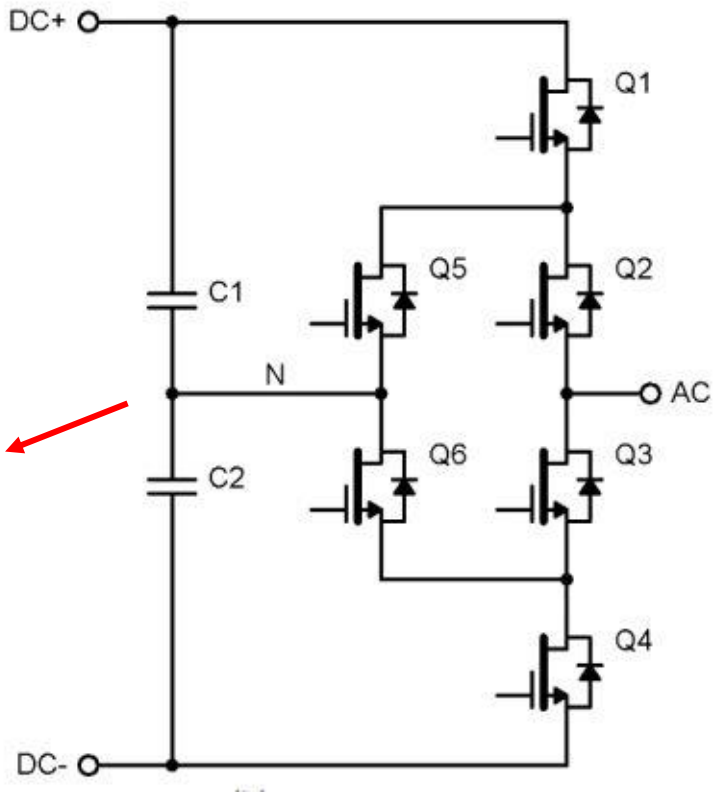
What is 3-Level ANPC topology

- 3L ANPC (Three Level Active Neutral Point Clamp) is a bidirectional topology
- it allows usage of half DC link voltage semiconductor devices since a DC Capacitor Bank divides the DC link voltage
- there are 3 different modulation schemes possible
- LF Modulation is selected because of the uniform temperature between MOSFETs and easier layout
- Q2 and Q3 are switching at low frequency while Q1, Q4, Q5, Q6 are modulated at carrier frequency (high frequency)



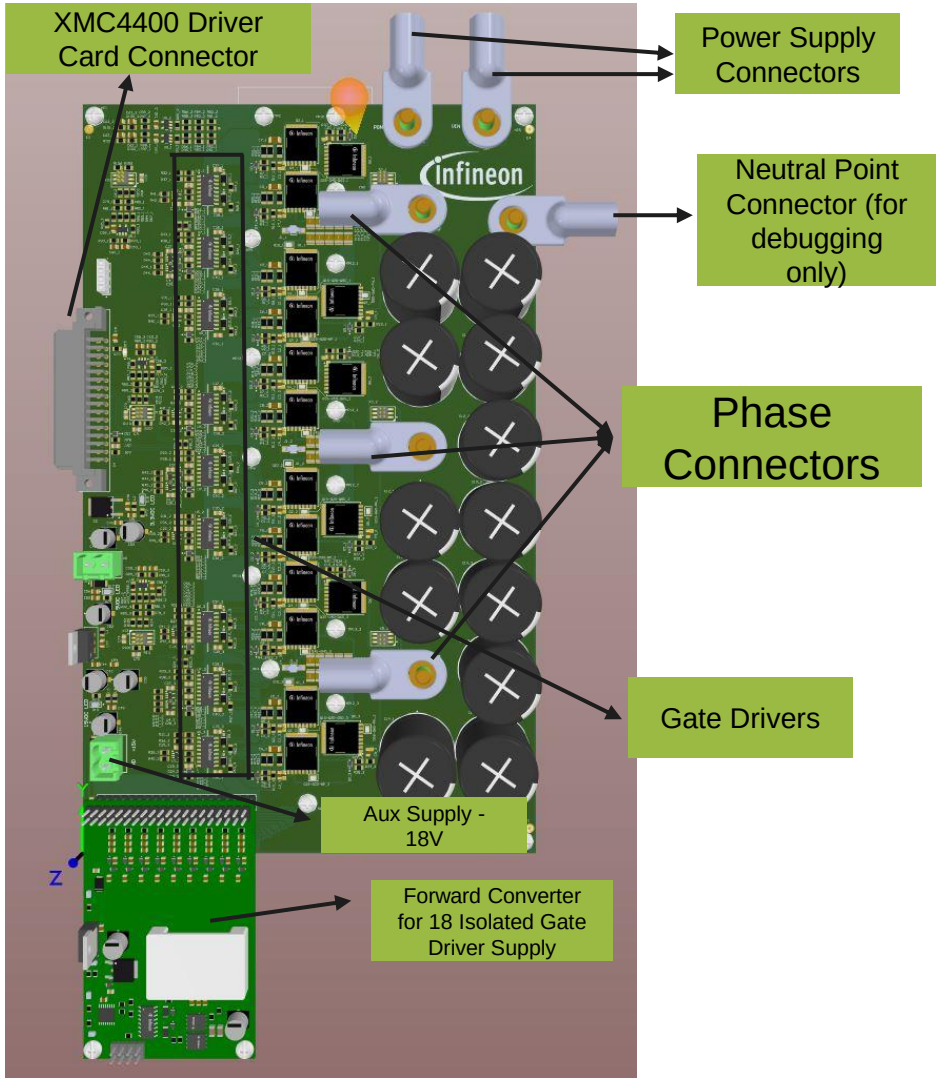
Benefits of 3-Level ANPC

- lower voltage rated semiconductors
- better switching performance due to lower voltages
- better EMI performance due to slower dv/dt and three different voltage levels
- better conduction performance due to lower voltages
- better efficiency
- higher output power



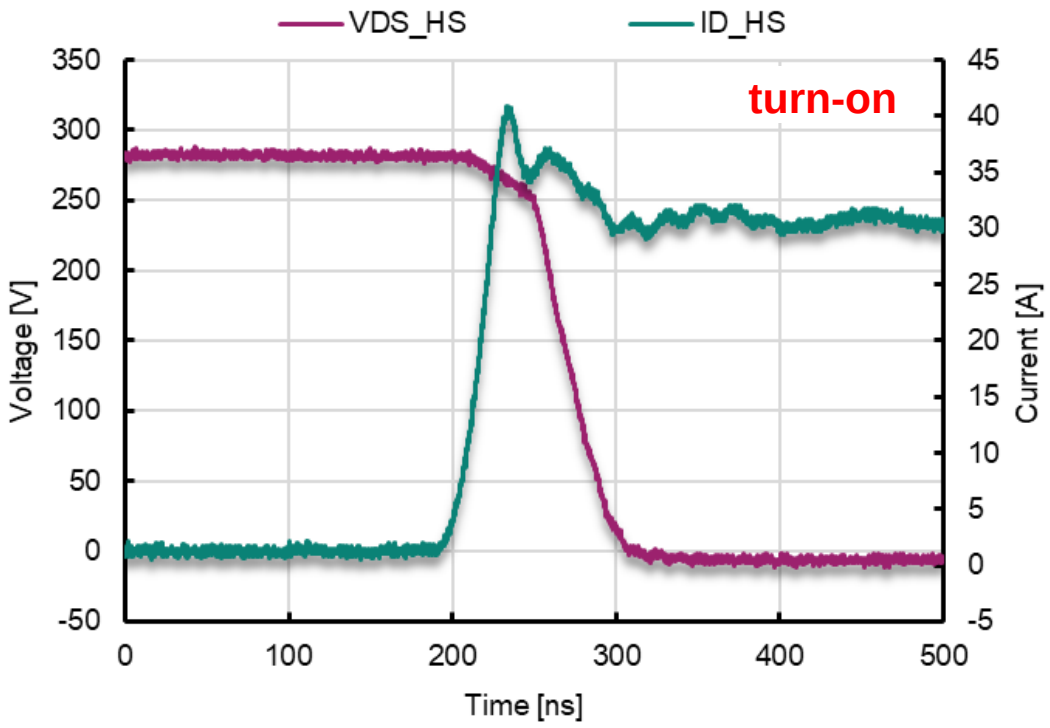
Introduction of the test board

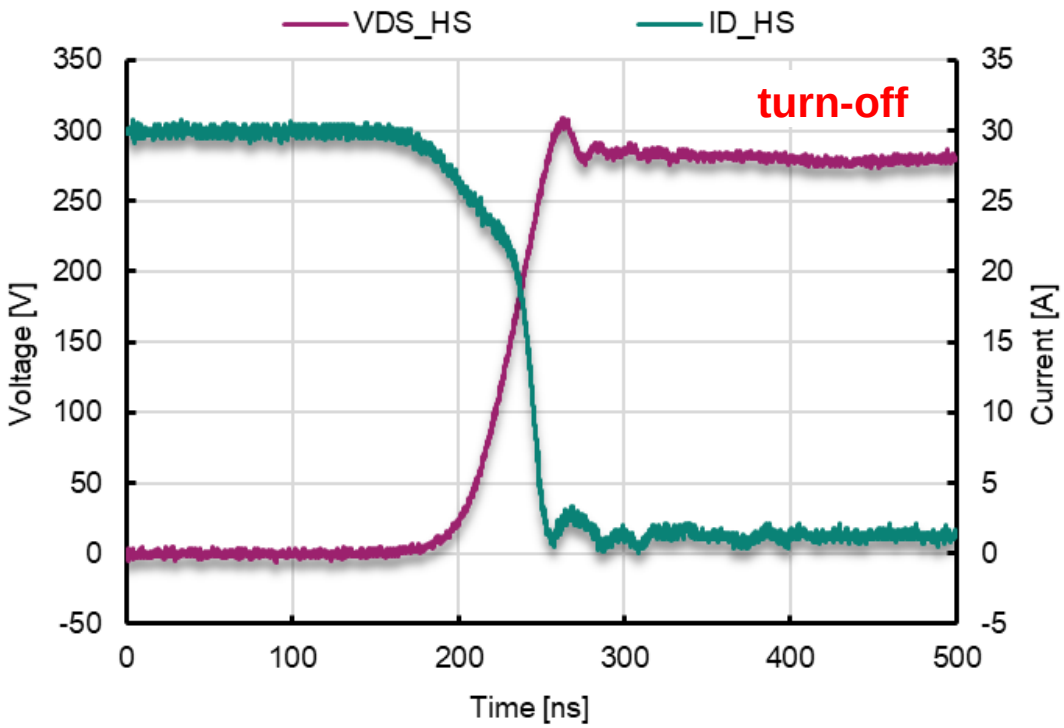
- 18 x SiC 400V IMT40R01XM2H in TOLL package
- 4 Layer - 2oz, 1.76mm thickness PCB
- 9x 2EDF7275 gate driver
- Forward Converter for gate driver supply
  - 1 Input – 18 Isolated Outputs with planar transformer
  - XMC1302-T028 for communication and controlling
  - OptiMOS BSZ099N06LS5 60 V in half bridge configuration
  - 2EDF7275 gate driver with bootstrap
- 3x TLI4971 current sensor to measure the output phase current



Switching waveforms

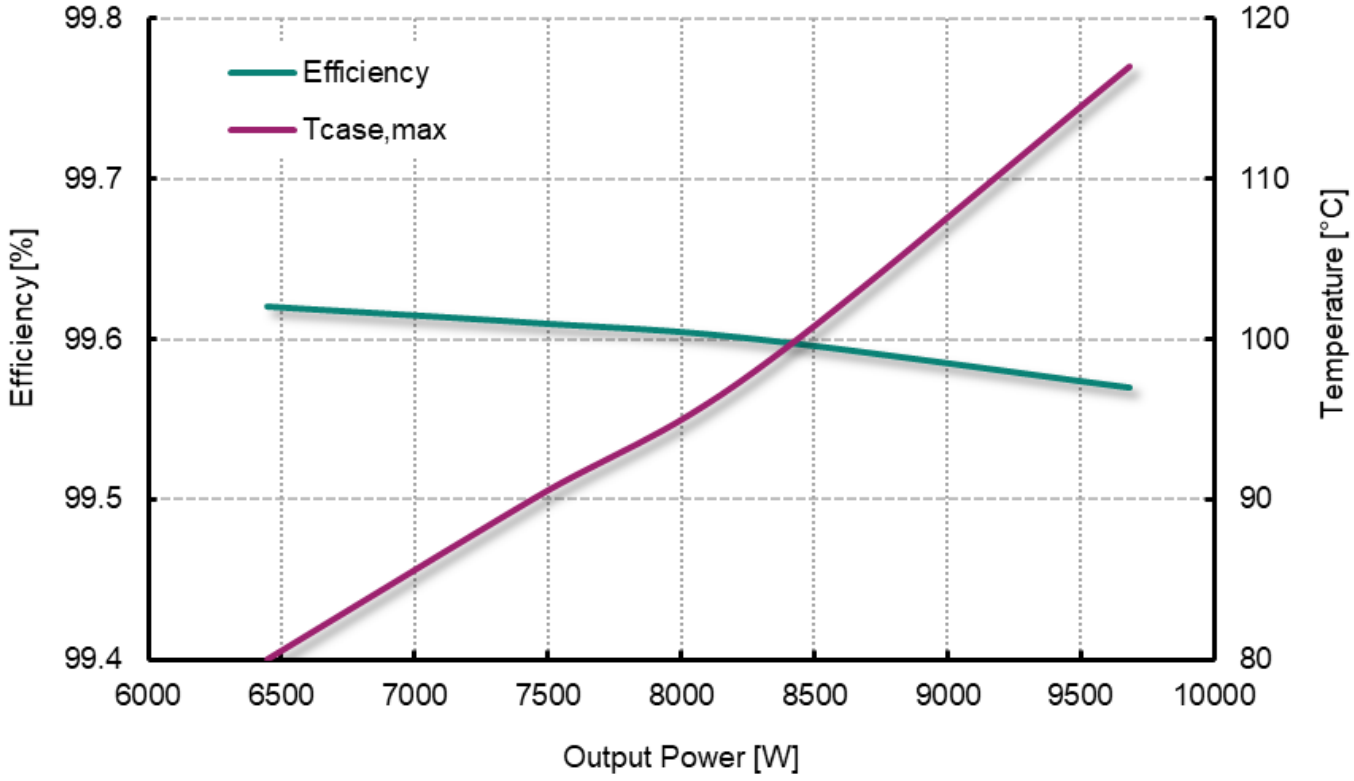
- switching waveforms were measured using a double-pulse configuration of the 3-Level ANPC board
- use of an inductive-resistive load of 1 mH + variable resistance
- the dv/dt per switch is limited to 5 V/ns
- measurements reveal a very smooth switching behavior of the 400 V device





Efficiency and case temperature

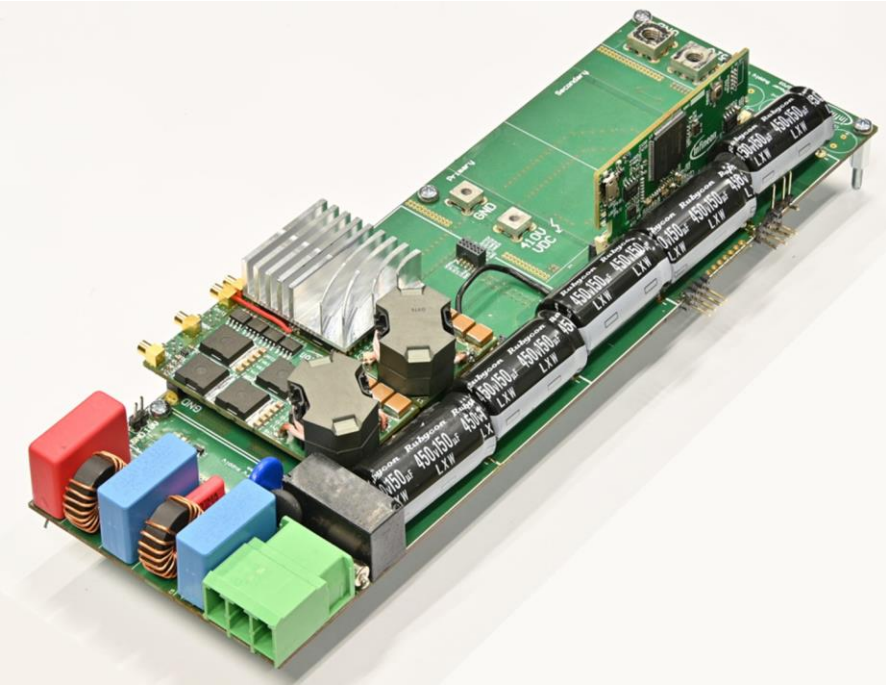
- inverter runs at a switching frequency of 10 kHz, dv/dt per switch limited to 5 V/ns, V_{DC} = 600 V
- no heatsink connected to enable temperature measurement by a thermal camera
- efficiency analysis excludes gate drivers and controller stage
- inverter delivers an efficiency of η = 99.57 % for 9.74 kVA load

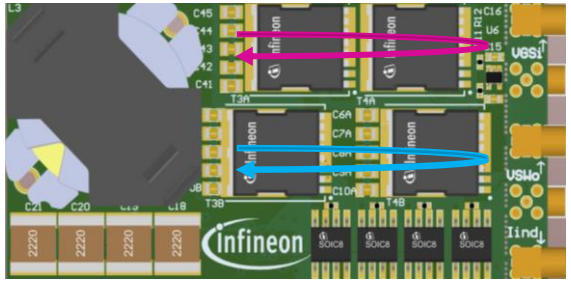


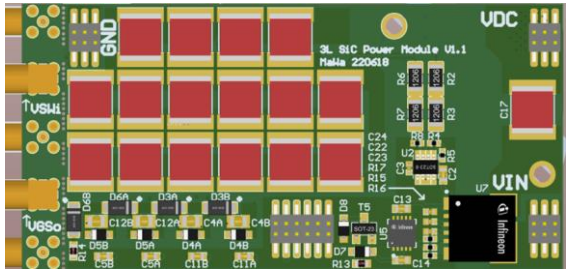
Outlook: device performance in 3-Level PFC

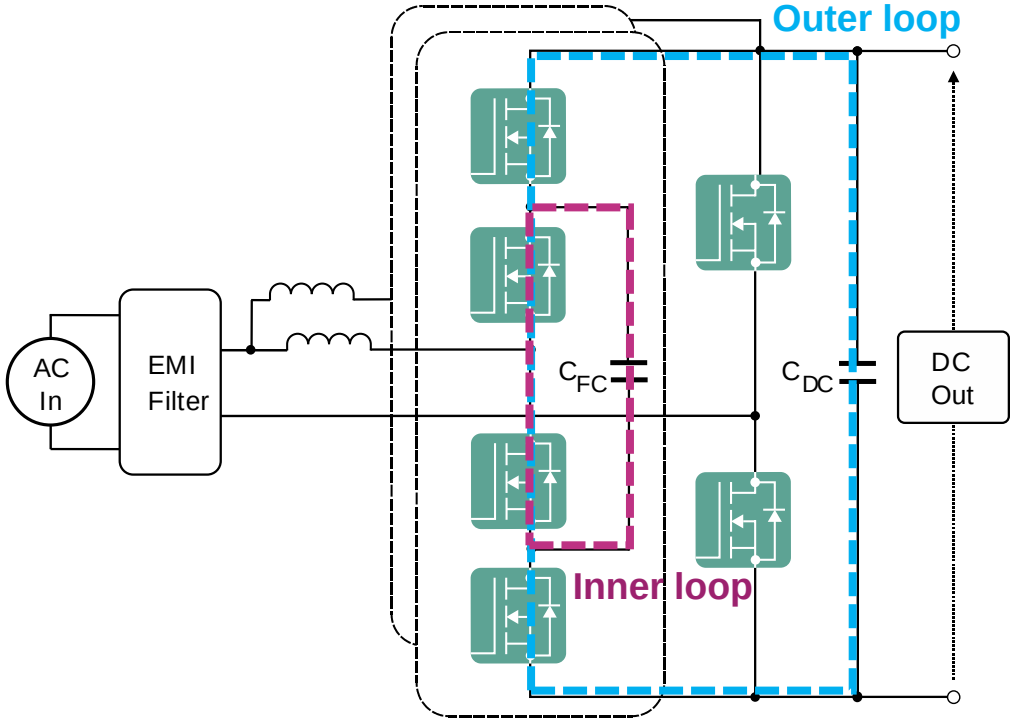
Technology demonstrator platform

- 2x interleaved 3-Level Flying-Cap (FC) PFC, each leg capable of 2.5 kW output power
- switching frequency of 80 kHz at device level results in 320 kHz effective for significant smaller EMI
- 230 VAC input and above, DC link voltage of 380 V or 420 V depending on input voltage



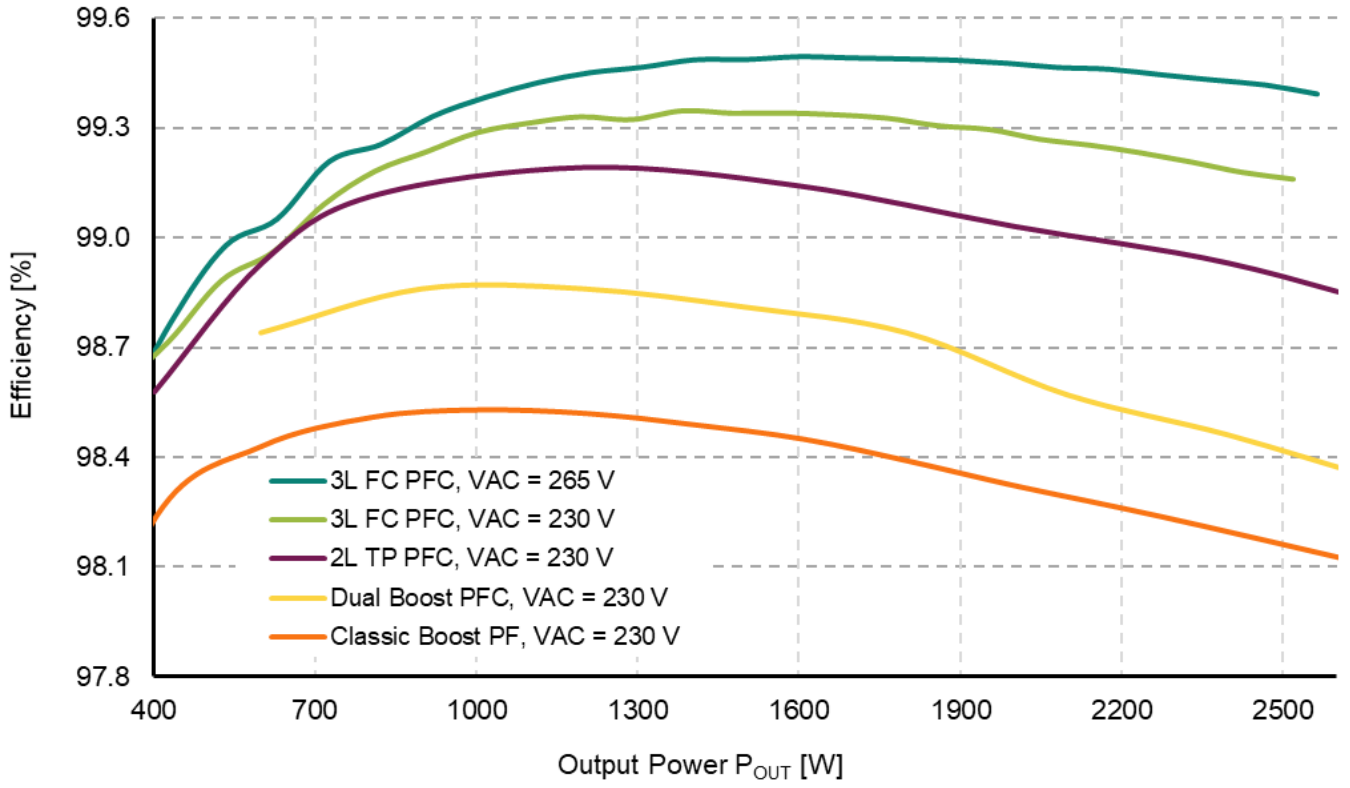






Efficiency comparison of 3-Level FC PFC with other solutions

– the 3-Level FC solution outperforms the 2-Level TP PFC at an AC input voltage of 230 V, resulting in 25% lower losses
– the series connection of 2x 400 V devices allows also higher input levels of 277 VAC or even 350 VAC, which helps to address the increasing power demand of AI in data centers



Summary

Summary

- the new 400 V CoolSiC™ G2 MOSFET technology is introduced, which offers a unique combination of performance, reliability and ease of use
- it offers Ron x A reduction and FOM improvement over existing solutions, with flat $R_{DS,on}$ vs T_J characteristics
- the low charges and the linearity of the output capacitance offer fast-switching capability, high slew rate control and low EMI
- the new devices allow highest efficiency and power density by enabling the adoption of innovative topologies, like 3-Level ANPC or 3-Level PFC
- the advantages of the new devices are demonstrated in a medium-power 3-phase 3-Level ANPC inverter
- the superior inverter efficiency beyond 99.5% (at dv/dt ≤ 5 V/ns) confirms the expected potential of the technology
- the high potential of the 400 V SiC MOSFET technology is also confirmed by the test results in a 3-Level Flying-Capacitor PFC

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Thank you for the attention!

I‘m pleased to answer your questions.

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