

Validating Duty Cycle-Based Repetitive Gate and Drain Transient Overvoltage Specifications for GaN HEMTs

Shengke Zhang, Ph.D. Efficient Power Conversion

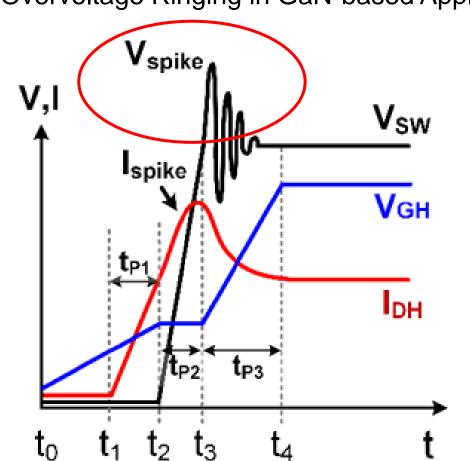


Introduction

- Motivation
- Definition of Duty Cycle-based Overvoltage Specifications
- Drain Repetitive Transient Overvoltage
- Gate Repetitive Transient Overvoltage
- Conclusions

Motivation





Transient Overvoltage Ringing in GaN-based Applications [1]

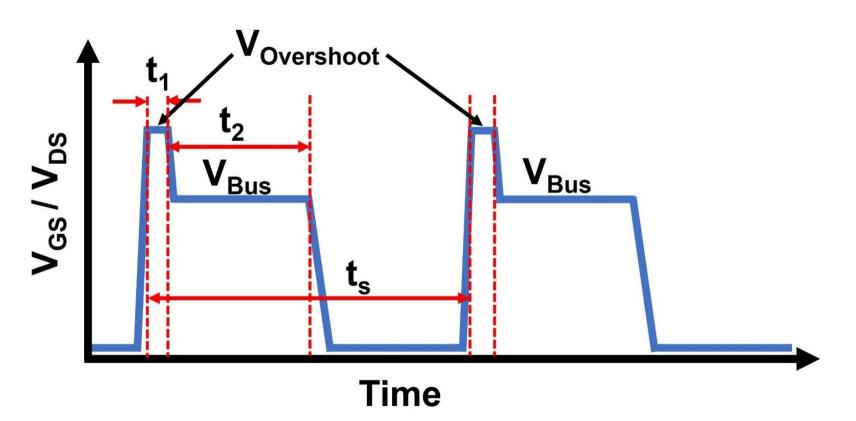
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[1] Ke et al, "A Tri-Slope Gate Driving GaN DC–DC Converter With Spurious Noise Compression and Ringing Suppression for Automotive Applications" in IEEE Journal of Solid-State Circuits, vol. 53, no. 1, pp. 247-260, Jan. 2018



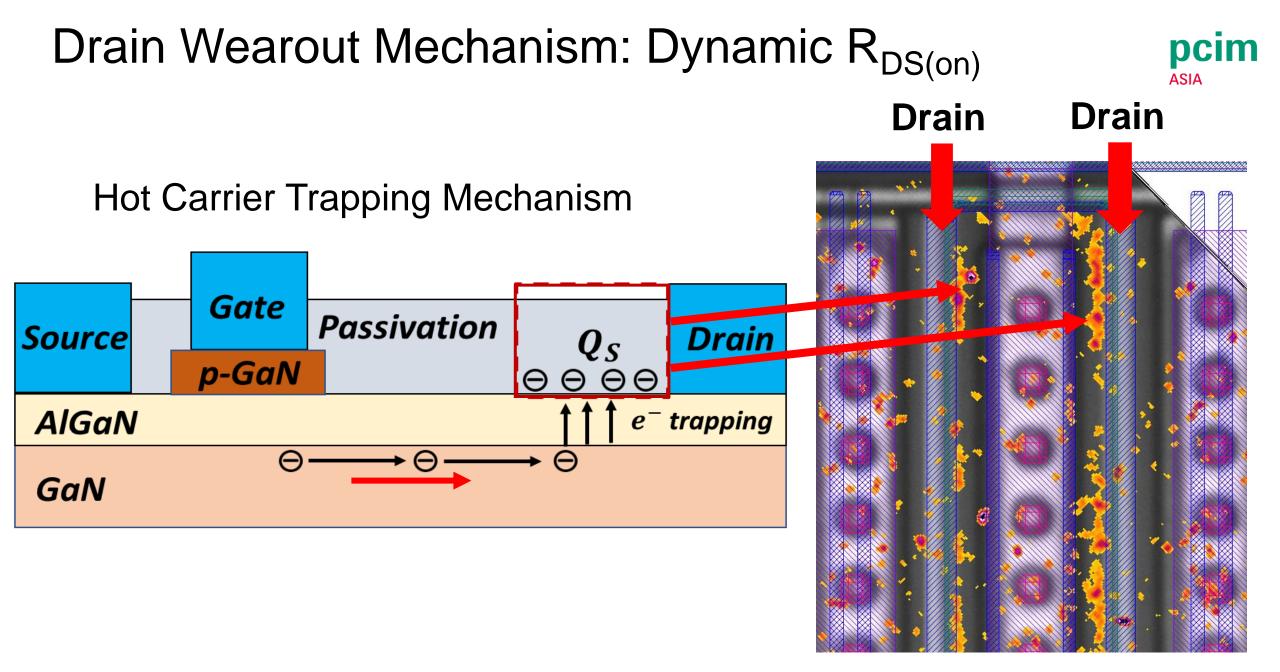
What is Duty Cycle-based Overvoltage Specification?







Drain Repetitive Transient Overvoltage Specification



Lifetime Model for Drain Wearout Mechanism $f(E)dE \propto Ee^{-E/qF\lambda}dE \quad \frac{dQ_s}{dt} = A \int_{\Phi_{bl}+\beta Q_s}^{\infty} f(E)dE = A \int_{\Phi_{bl}+\beta Q_s}^{\infty} Ee^{-E/qF\lambda}dE \quad \frac{dQ_s}{dt} = B \exp\left(-\frac{\beta Q_s}{qF\lambda}\right)$

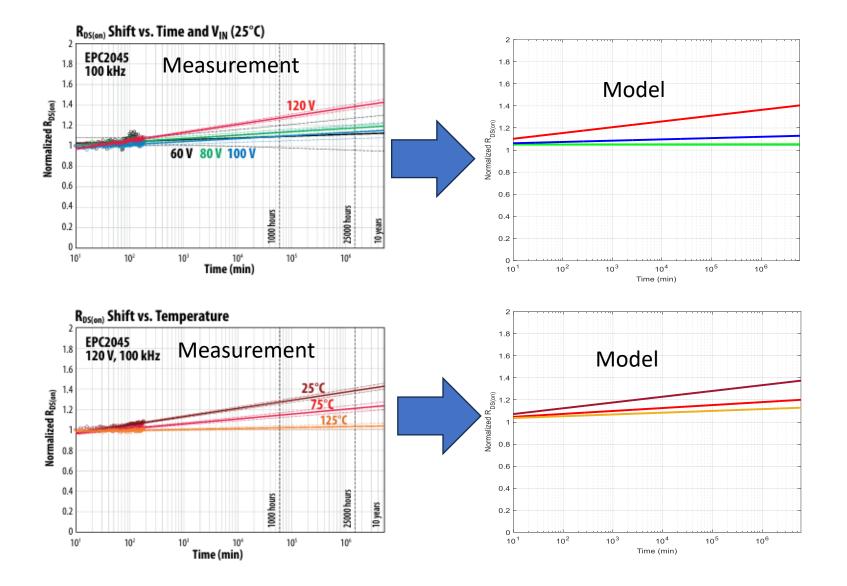
$$Q_{S}(t) = \frac{qF\lambda}{\beta} \log\left(1 + \frac{B\beta}{qF\lambda}t\right) \qquad R(t) = R_{0} + \frac{C}{Q_{P} - Q_{S}} = R_{0} + \frac{C}{Q_{P} - \frac{qF\lambda}{\beta} \log\left(1 + \frac{B\beta}{qF\lambda}t\right)}$$

$$R(t) \approx R_0 + \frac{C}{Q_P} \left[1 + \frac{qF\lambda}{Q_P\beta} \log\left(1 + \frac{B\beta}{qF\lambda}t\right) \right] \qquad \tau_{LO} \propto exp\left(\frac{\hbar\omega_{LO}}{kT}\right) \quad \lambda = v_{th}\tau_{LO} \propto A\sqrt{kT}exp\left(\frac{\hbar\omega_{LO}}{kT}\right)$$

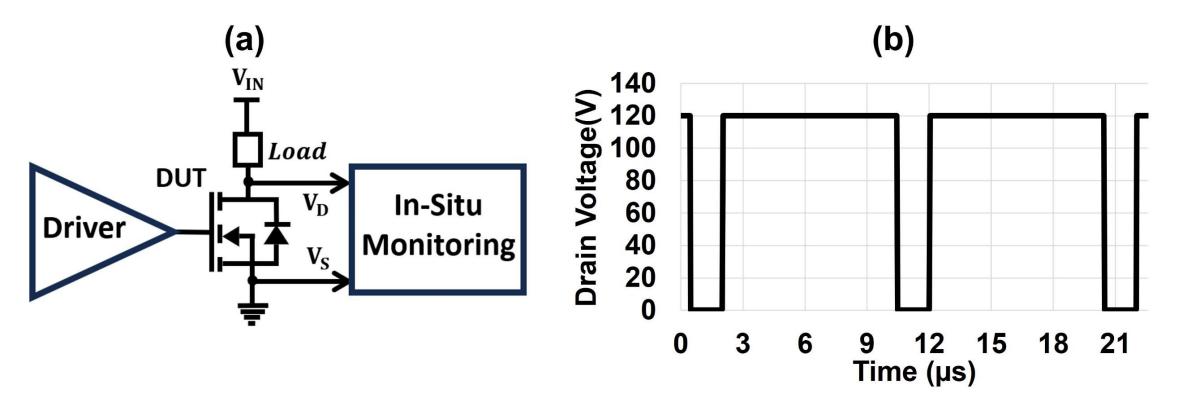
$$\frac{\Delta R}{R} = \frac{R(t) - R(0)}{R(0)} \approx a + bF \exp\left(\frac{\hbar\omega_{LO}}{kT}\right) \sqrt{T} \log(t)$$

Model vs Measurement





Resistive Hard Switching Circuit

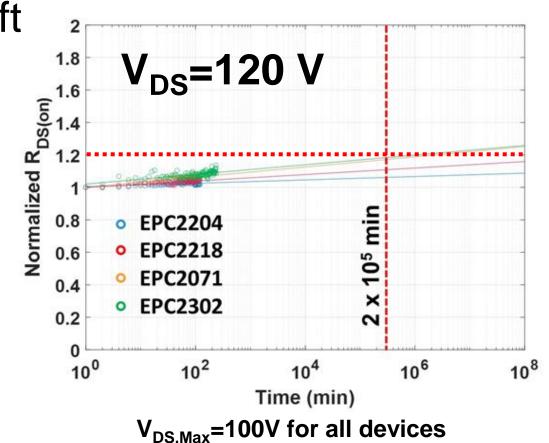


ASIA

- V_{DS} =120 V for 100 V maximum rated devices
- 85% of the time, the device is OFF with V_{DS} =120 V applied
- 15% of the time, the device is ON

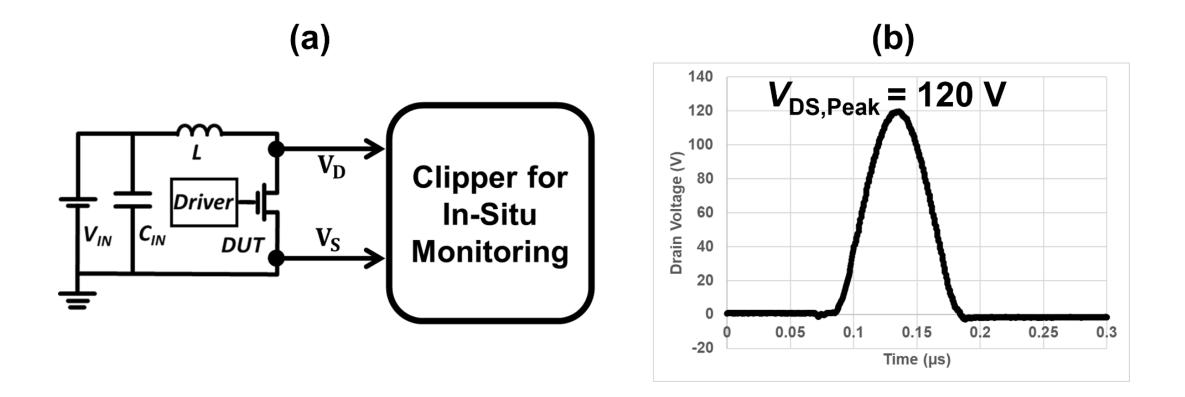
Developing Duty Cycle Factor for Drain Overvoltage

- Criteria: <20% Projected R_{DS(on)} Shift
- 2 x 10⁵ min x 85% (device off-time) = 1.7 x 10⁵ min
- 1.7 x 10⁵ mins / 25 years = ~1.3%
 25 years = 1.3 x 10⁷ mins



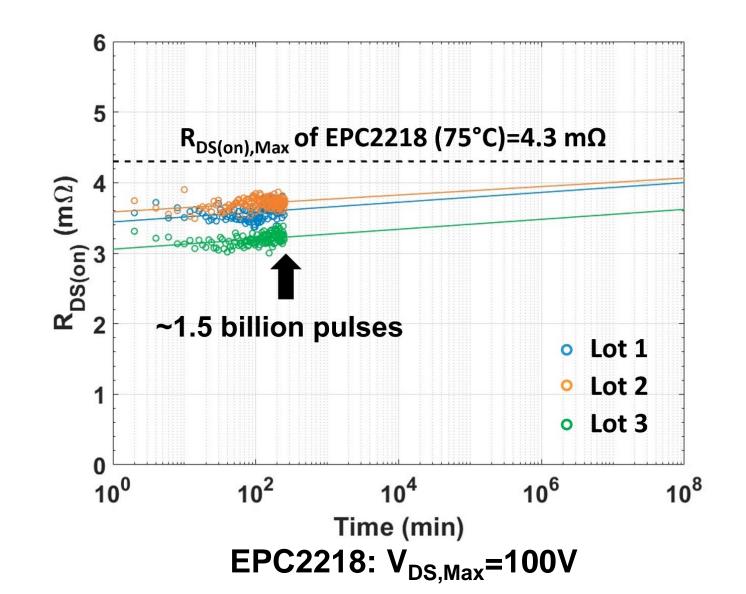
1% DC_{Factor} of the total lifetime when V_{DS} =120V

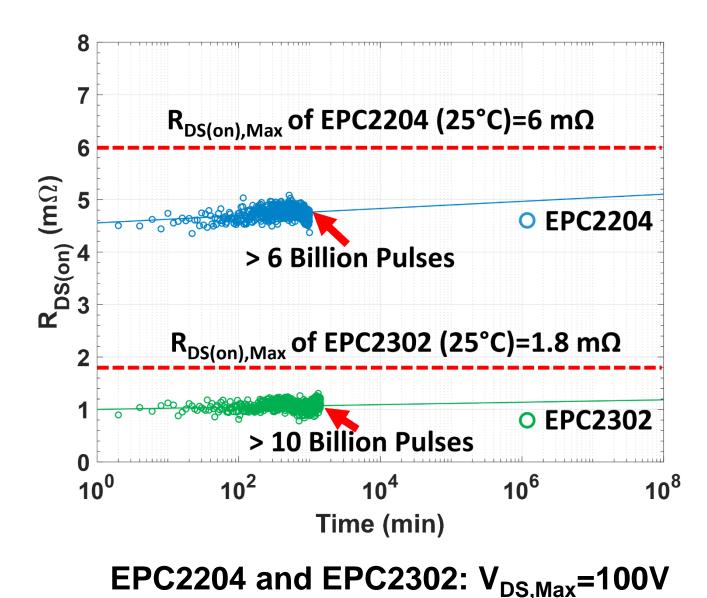




Validation of 120 V Repetitive Drain Transient Overvoltage









How to Use 1% DC_{Factor} in Applications

- A converter featuring 100 V max-rated GaN FETs operating at 1 MHz (period = 1 μ s)
- It shows a repetitive 120 V_{DS} spike measured with ~10 ns pulse width.
- 10 ns/1 μ s = 1% \leq 1% \rightarrow Low reliability risk

EPC's Repetitive Transient Overvoltage Specification

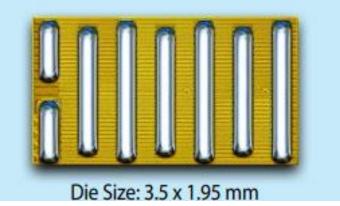


Maximum Ratings			
	PARAMETER	VALUE	UNIT
V _{DS}	Drain-to-Source Voltage (Continuous)	100	V
V _{DS(tr)}	Drain-to-Source Voltage (Repetitive Transient) ⁽¹⁾	120	
I _D	Continuous ($T_A = 25^{\circ}C$)	60	A
	Pulsed (25°C, $T_{PULSE} = 300 \ \mu s$)	231	
V_{GS}	Gate-to-Source Voltage	6	v
	Gate-to-Source Voltage	-4	
Tر	Operating Temperature	-40 to 150	°C
T _{STG}	Storage Temperature	-40 to 150	

EPC2218 – Enhancement Mode Power Transistor

 $V_{DS}, 100 V$ $R_{DS(on)}, 3.2 m\Omega max$ $I_{D}, 60 A$





⁽¹⁾ Pulsed repetitively, duty cycle factor (DC_{Factor}) $\leq 1\%$;

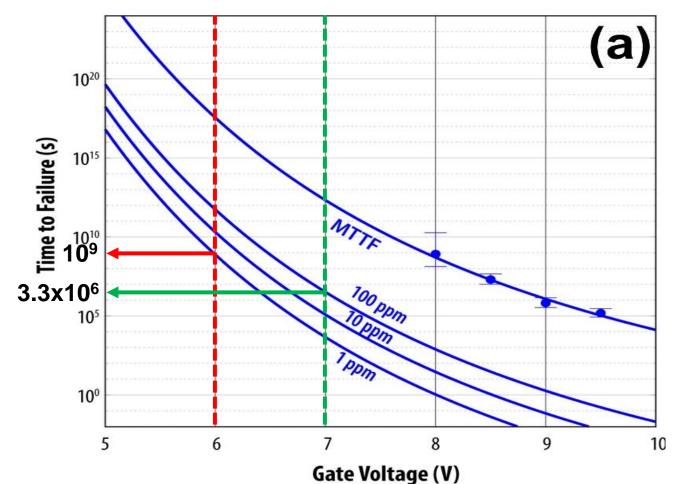


Gate Repetitive Transient Overvoltage Specification



Developing Duty Cycle Factor for Gate Overvoltage

- Project ~30 years $(1x10^9 \text{ seconds})$ lifetime with 1-ppm failure rate when $V_{GS} \le 6 \text{ V}$ (max-rated V_{GS})
- At V_{GS} =7 V, projected lifetime (100-ppm) = ~3.3 x 10⁶ seconds > 1% of 10 years lifetime

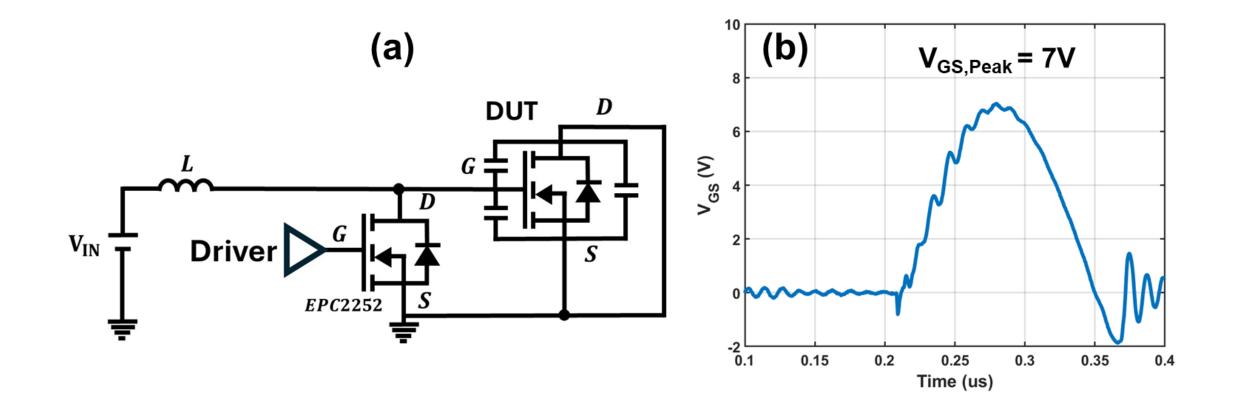


ppm: # failure of 1 million devices tested

1% DC_{Factor} of the total lifetime when $V_{GS}=7V$



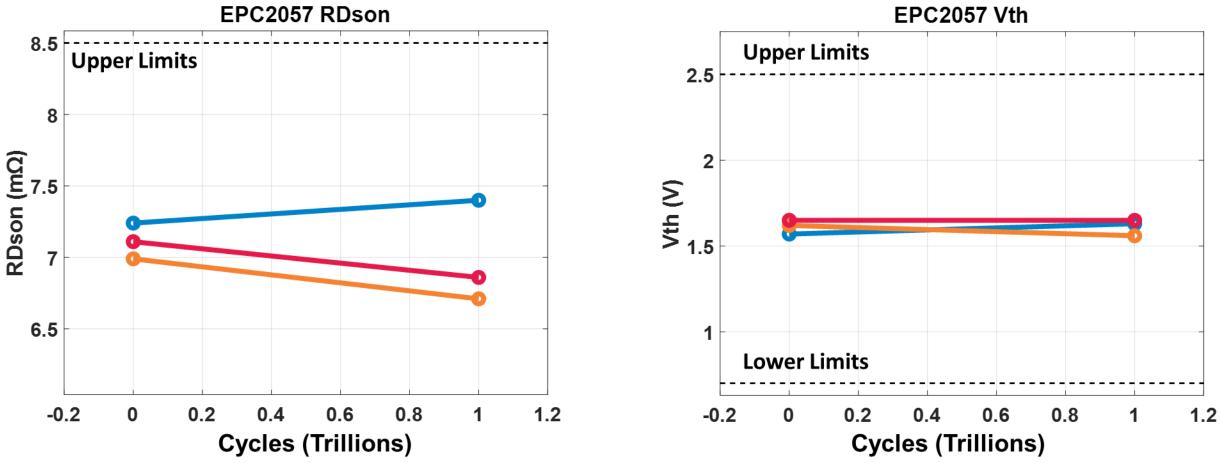
Validation: Gate Unclamped Inductive Switching



oltage ASIA

Validation of 7 V Repetitive Drain Transient Overvoltage

No issues found after 1 trillion pulses with V_{GS,Peak}=7V!



EPC's Repetitive Transient Overvoltage Specification



Maximum Ratings UNIT PARAMETER VALUE Drain-to-Source Voltage (Continuous) 150 v V_{DS} Drain-to-Source Voltage (Repetitive Transient)⁽¹⁾ 180 Continuous ($T_1 \le 125^{\circ}C$) 63 I_D А Pulsed (25 °C, $T_{PULSE} = 300 \ \mu s$) 157 Gate-to-Source Voltage 6 VGS Gate-to-Source Voltage v -4 Gate-to-Source Voltage (Repetitive Transient) (1) 7 T Operating Temperature -40 to 150 °C TSTG Storage Temperature -40 to 150 ⁽¹⁾ Pulsed repetitively, duty cycle factor (DC_{Factor}) ≤ 1%; Figure 13;

EPC2308 – Enhancement Mode Power Transistor

 V_{DS} , 150 V $R_{DS(on)}$, 6 m Ω max







How to Use 1% DC_{Factor} in Applications

- A converter featuring 100 V max-rated GaN FETs operating at 1 MHz (period = 1 μ s)
- It shows a repetitive 6.8 V_{GS} spike measured with 10 ns pulse width.
- 10 ns/1 µs= 1% ≤ 1% and V_{GS}=6.8 V < 7 V \rightarrow Low reliability risk



Conclusions

- Repetitive transient overvoltage ringing is commonly observed in GaNbased applications.
- The wearout mechanisms responsible for gate and drain stress are identified and the corresponding lifetime models are derived.
- A 1% duty cycle-based repetitive overvoltage specification is developed for both gate turn-on transients and drain turn-off transients.
- Different switching circuits are developed to validate the proposed overvoltage specifications for gate and drain.

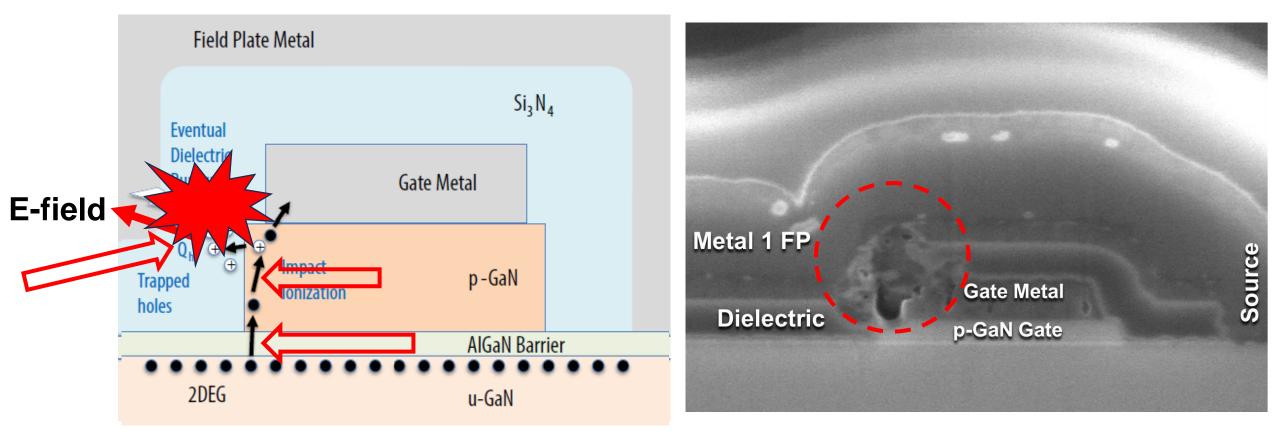


Thank You!

Backup

Gate Wearout Mechanism: Impact Ionization





Lifetime Model for Gate Wearout Mechanism



MTTF: Mean Time to Failure

 $MTTF = \frac{Q_c}{G}$

 Q_C is the critical charge density of SiN layer

Q is the electron-hole pair generation rate from impact ionization

$$G = \alpha_n \frac{|J_n|}{q} + \alpha_p \frac{|J_p|}{q}$$
$$G \approx \alpha_n \frac{|J_n|}{q} \qquad J_n >> J_p$$

Impact Ionization coefficient

$$\alpha_n = a_n e^{-\left(\frac{b_n}{E}\right)^m}$$

Temperature dependence of impact ionization coefficient

$$a_n = a_{n.0}(1 + c\Delta T)$$
$$b_n = b_{n.0}(1 + d\Delta T)$$

$$MTTF = \frac{qQ_c}{J_n a_{n.0} (1 + c\Delta T)} e^{\left(\frac{b_{n.0} (1 + d\Delta T)}{E}\right)^m}$$