

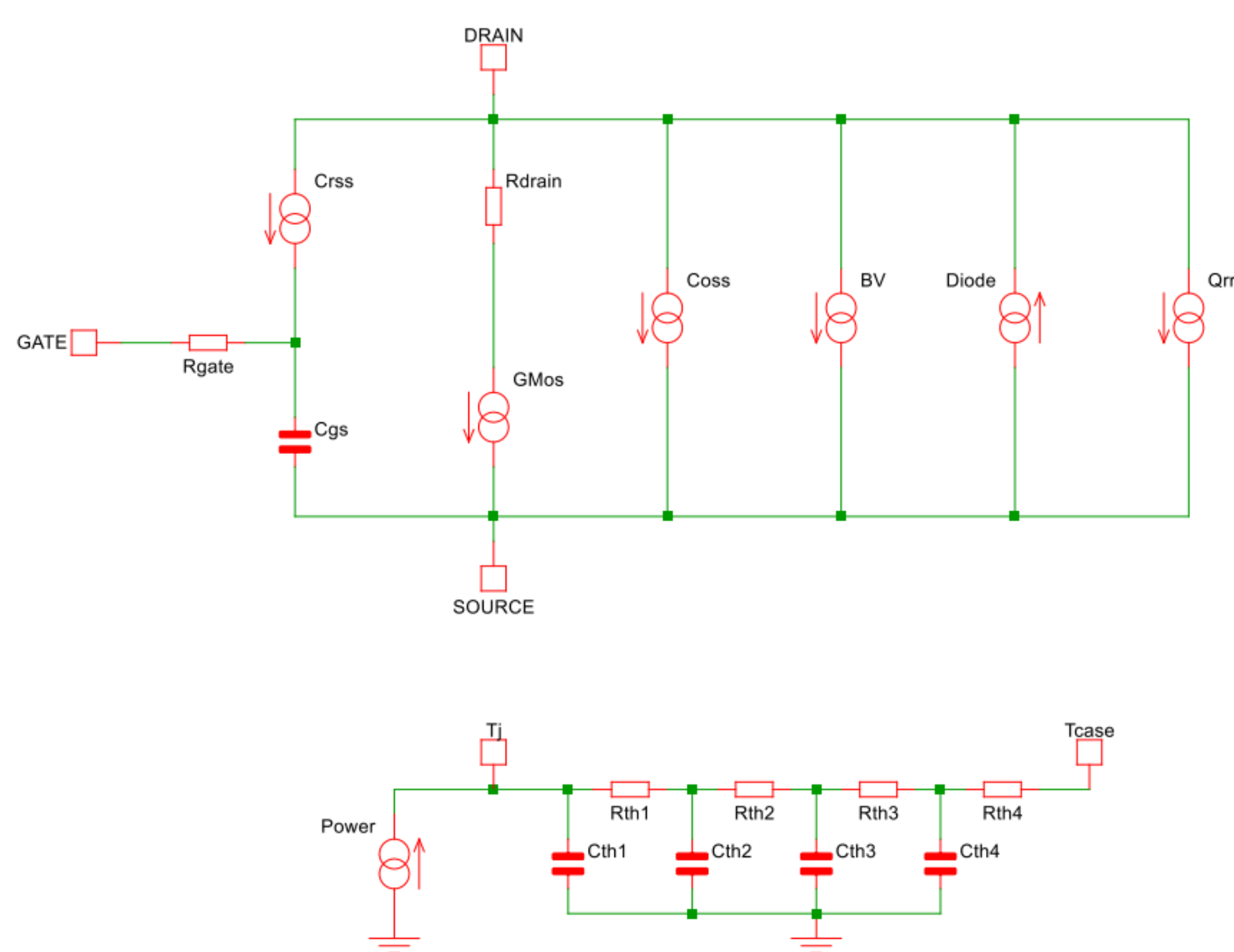
SPICE Modeling and Experimental Validation of the Active Short Circuit (ASC) Test with Silicon Carbide Power MOSFETs

By Alessandra RAFFA, Pier Paolo VENEZIANO, Benedetto AMATA, Carlo BRUGALETTA, Paolo MESSINA, Marco PAPASERIO, Antonia LANZAFAME

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Introduction

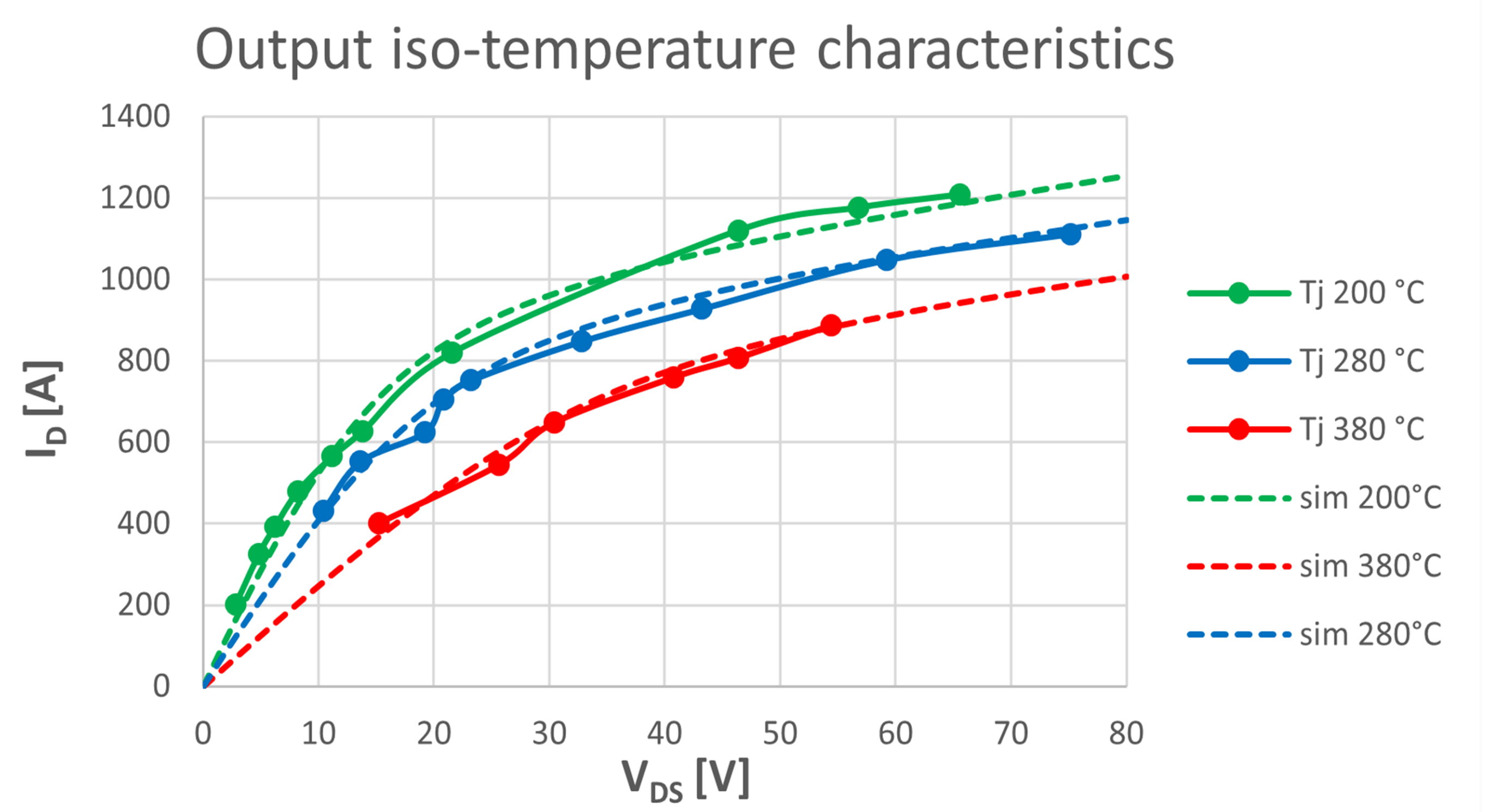
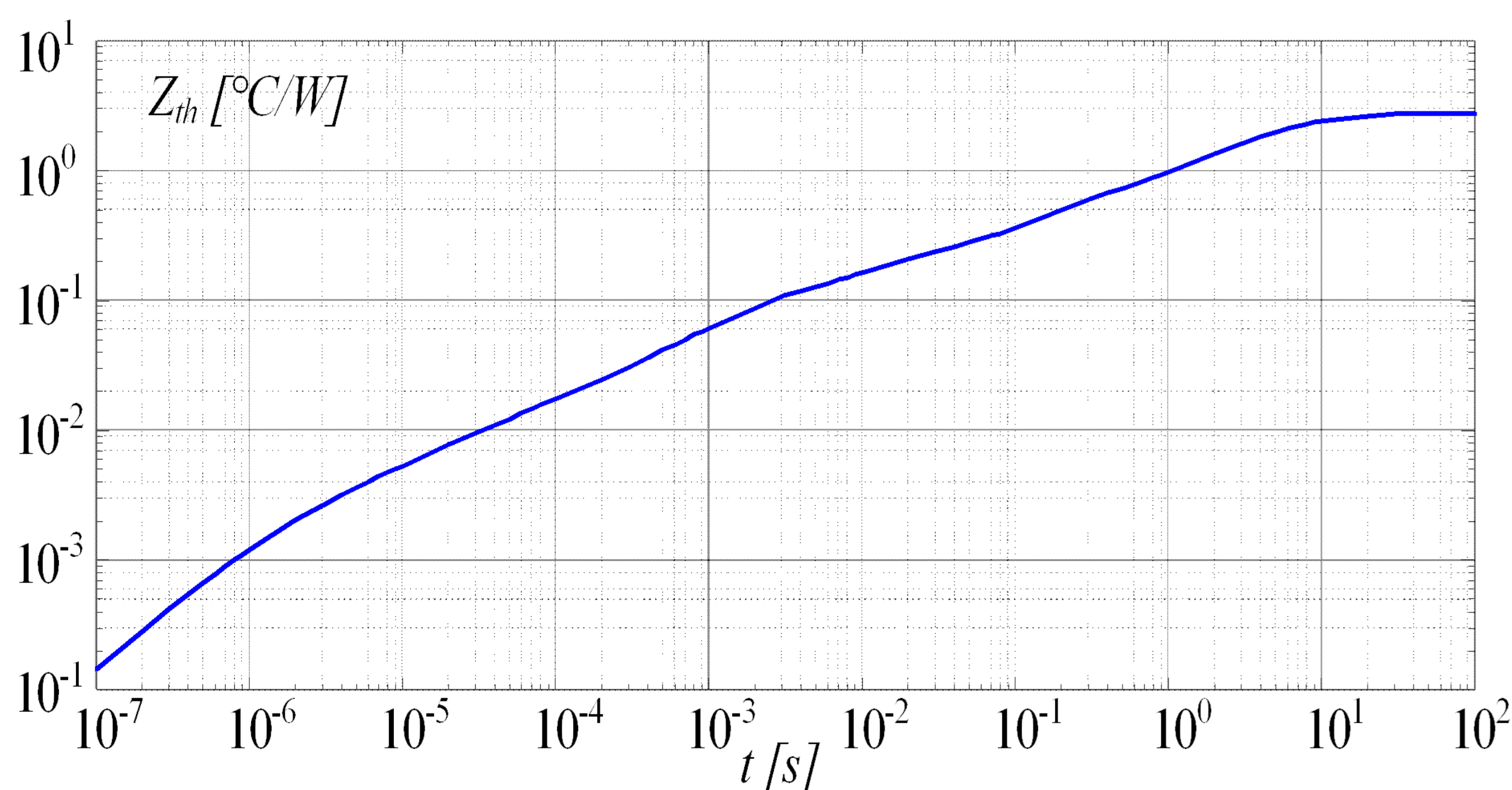
A new SPICE model for SiC MOSFETs to be used in ASC test simulations has been developed. This model accurately reproduces the behavior of the device at extreme conditions, such as high temperature, high current, and high drain-source voltage, typical for this kind of test. The ASC test has been simulated and the results have been compared with experimental measurements to validate the methodology.



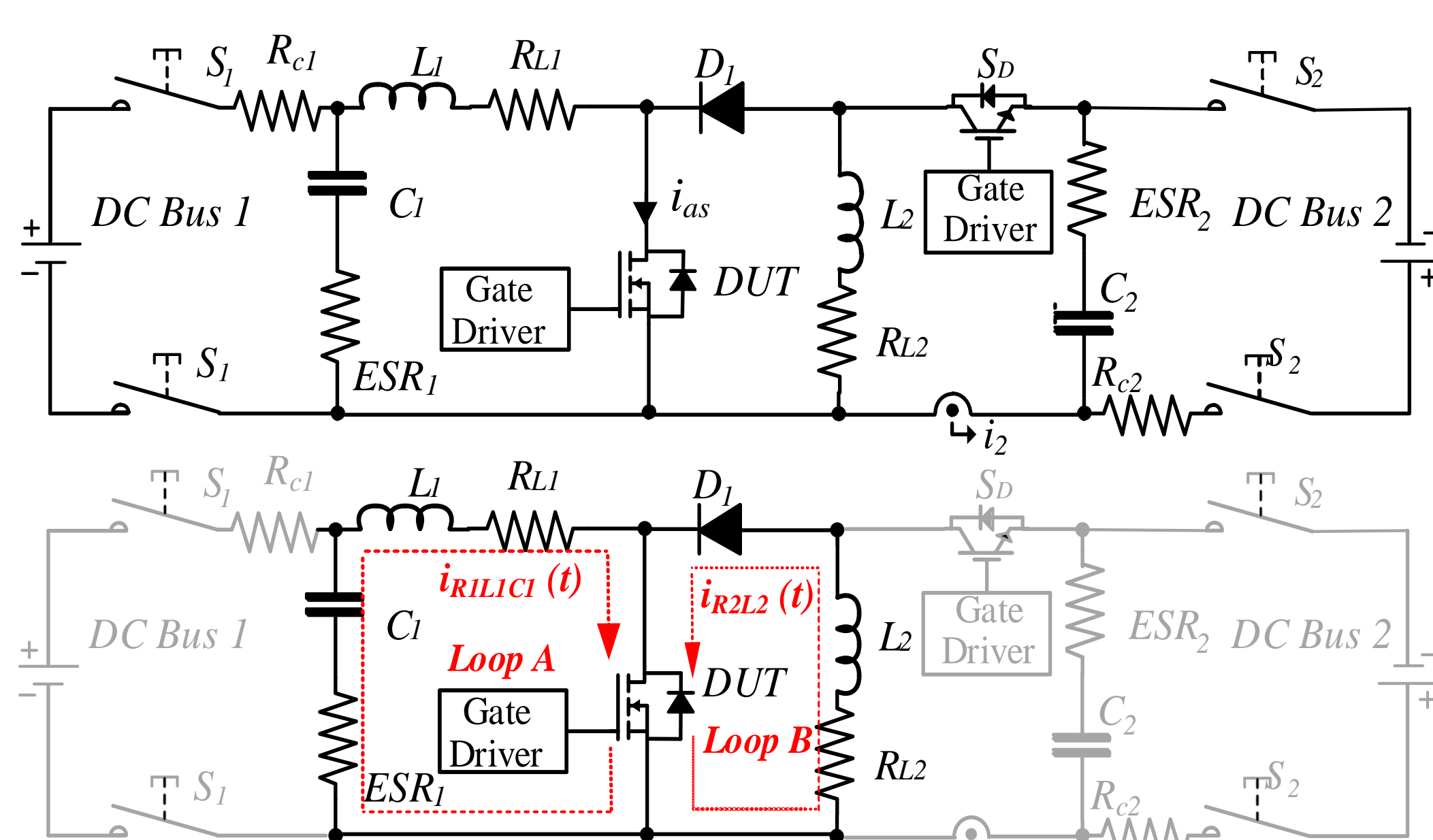
Device modeling for ASC test Simulation

- Self-heating capabilities through RC network (Cauer) SiC power MOSFET
- Two functions to model the output behavior in linear and non linear region, able to reproduce the effect of the temperature on the output current

$$f(V_{ds}, V_{gs}, T_j) = x_0 \left\{ V_{ds} \left[1 + x_1 \left(1 + \alpha_1 (T_j - T_0) + \alpha_2 (T_j - T_0)^2 + \alpha_3 (T_j - T_0)^3 \right) + \frac{V_{ds}}{k_0} \right] \frac{V_{gs}}{|V_{gs}| + 1 + \frac{V_{ds}}{k_1}} \right\} (1 + x_2 V_{gs})$$



Experimental setup



Specification of the DUT	
$V_{BDSS} (V_{GS} = 0 V)$	750 V
$R_{DS(on)} @ (V_{GS} = 18 V, I_{DS} = 150 A)$	15.7435 mΩ (Typ) @ 200 °C
$I_{DS} @ 200 °C$	150 A

Main circuit parameters	
C_1	260 μF
ESR_1	5.44 mΩ
L_1	1.2 mH
R_{L1}	1.85 mΩ
C_2	3.1 mF
ESR_2	16 mΩ
L_2	3.62 mH
R_{L2}	190 mΩ
$R_{D1} @ 125 °C$	2.45 mΩ
ω	1790 rad/s
ω_{02}	298 rad/s

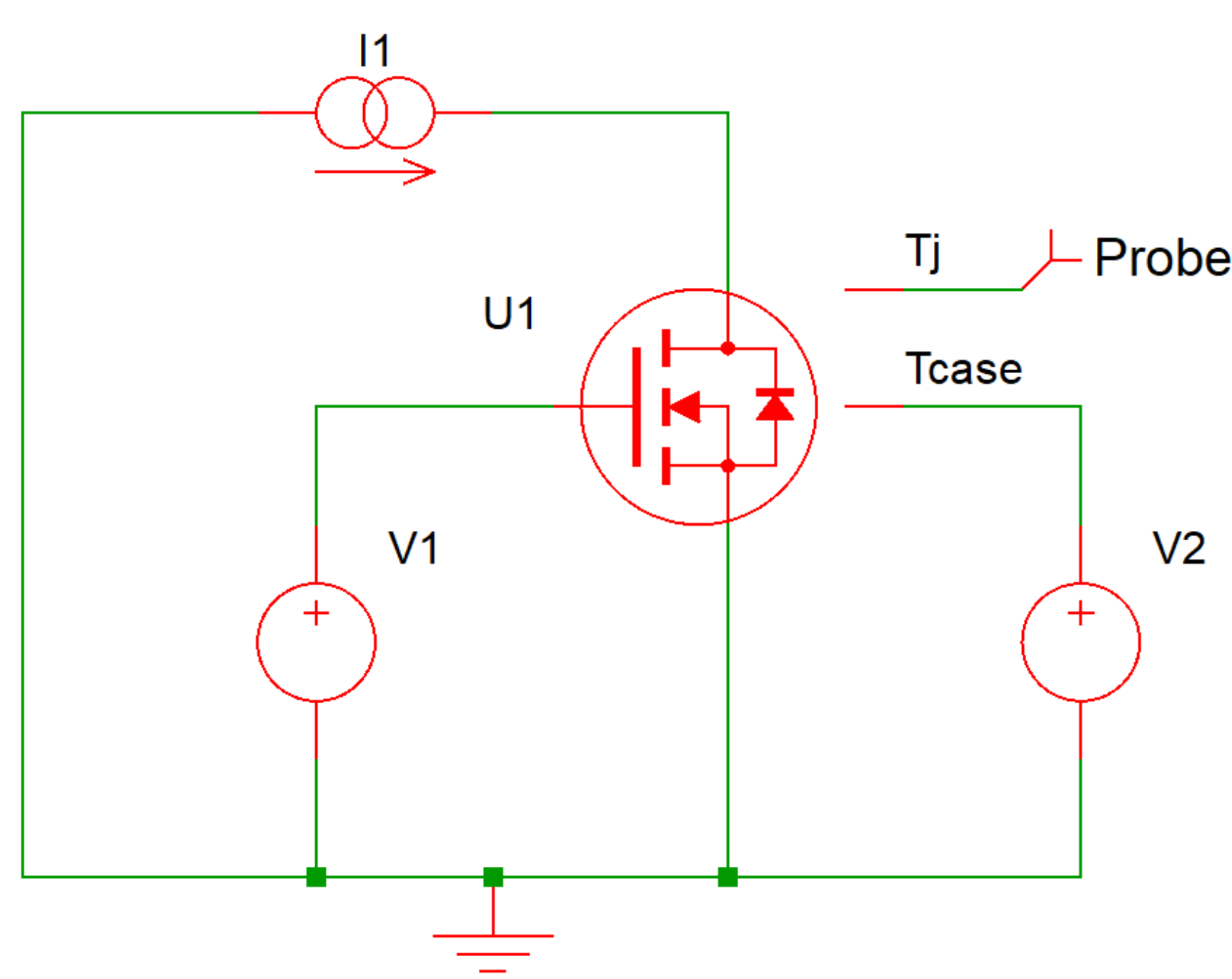
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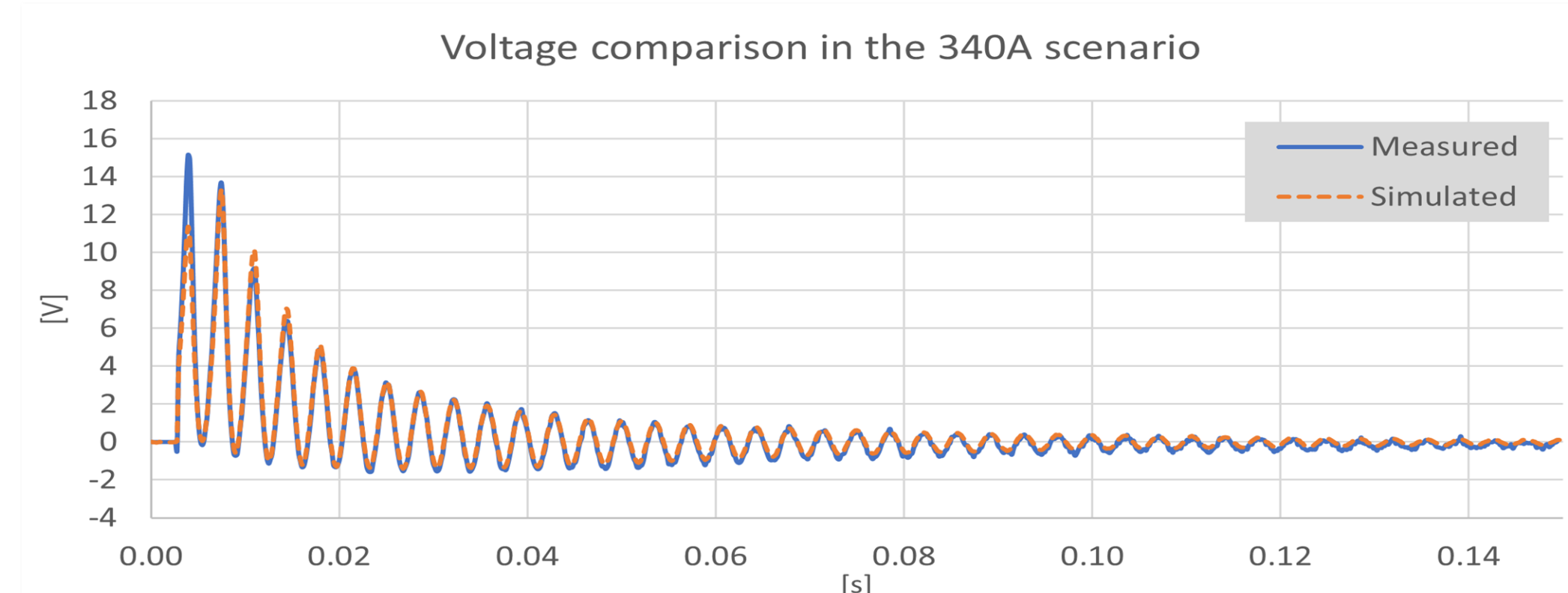
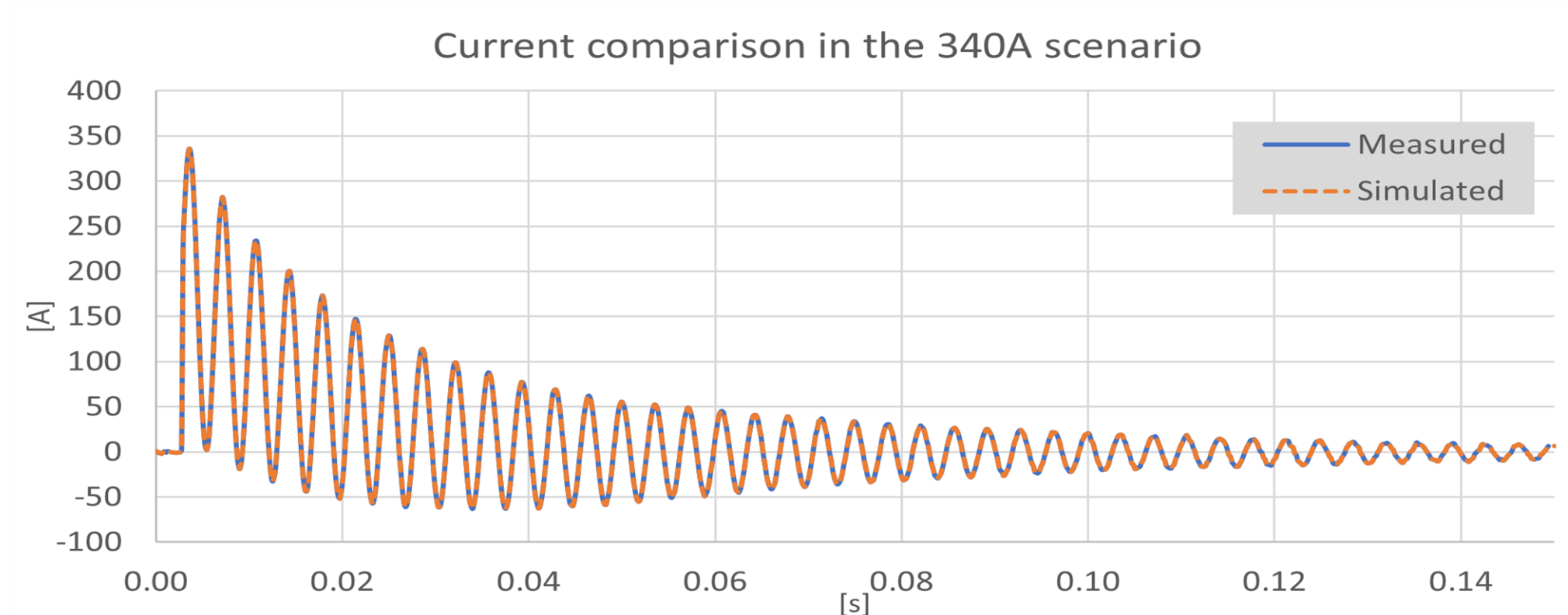
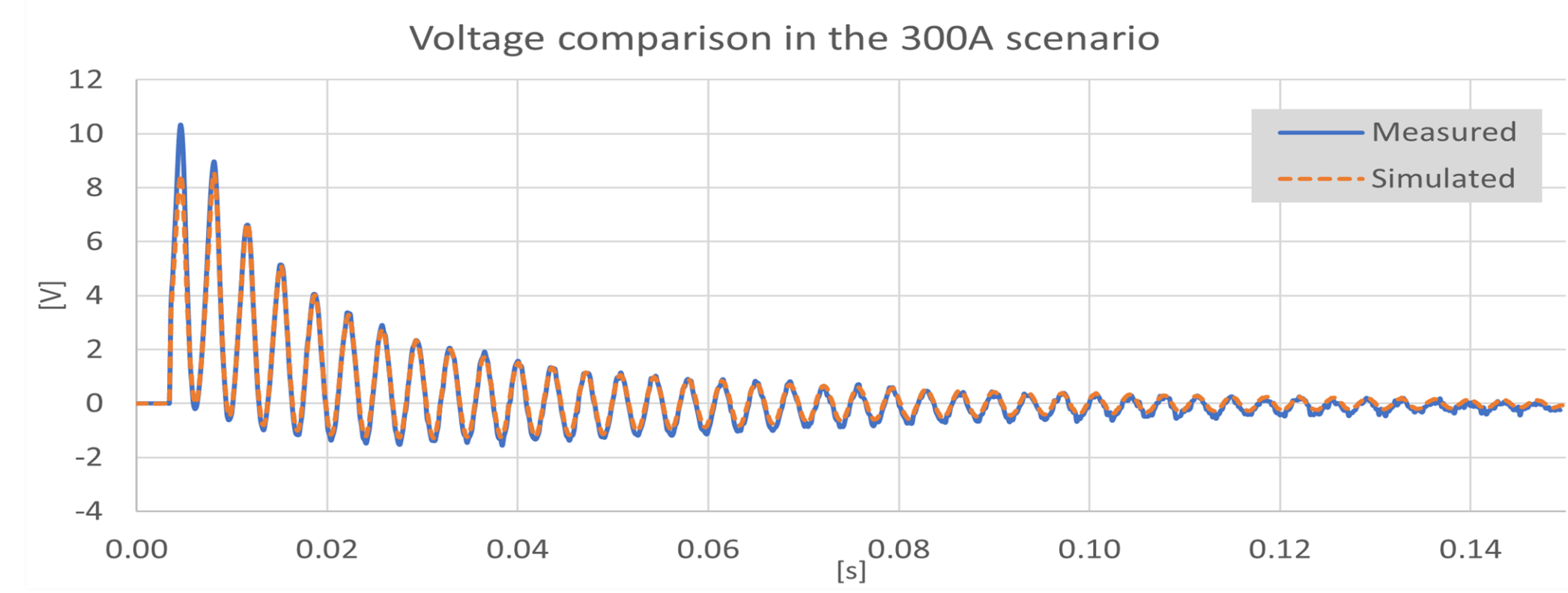
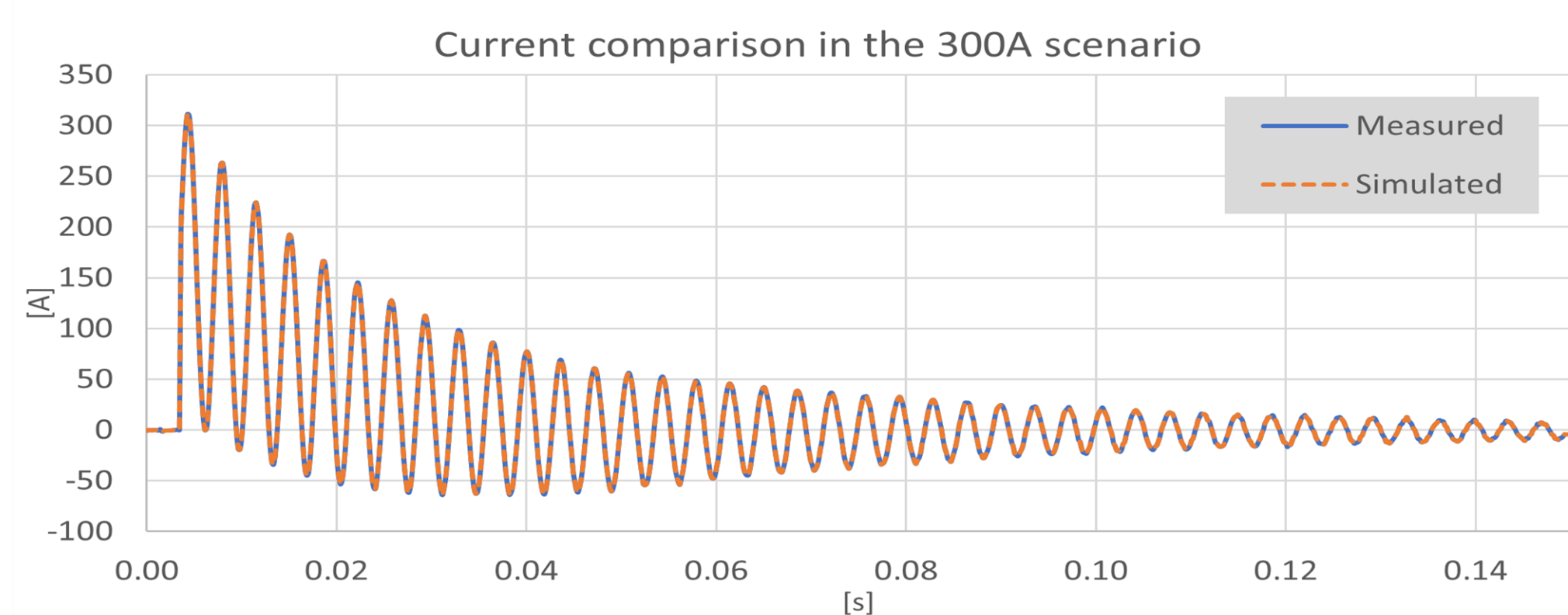
Simulation Results

In a SPICE environment, the simulation of the ASC test is performed using the reported schematic, in which the pseudo-damped sinusoidal currents with 300 A and 340 A peak, coming from the measurements, are forced in the drain of the MOSFET, U1, by the current generator, I1. The device is in the on-state set by the V1 generator, while V2 defines the external temperature.

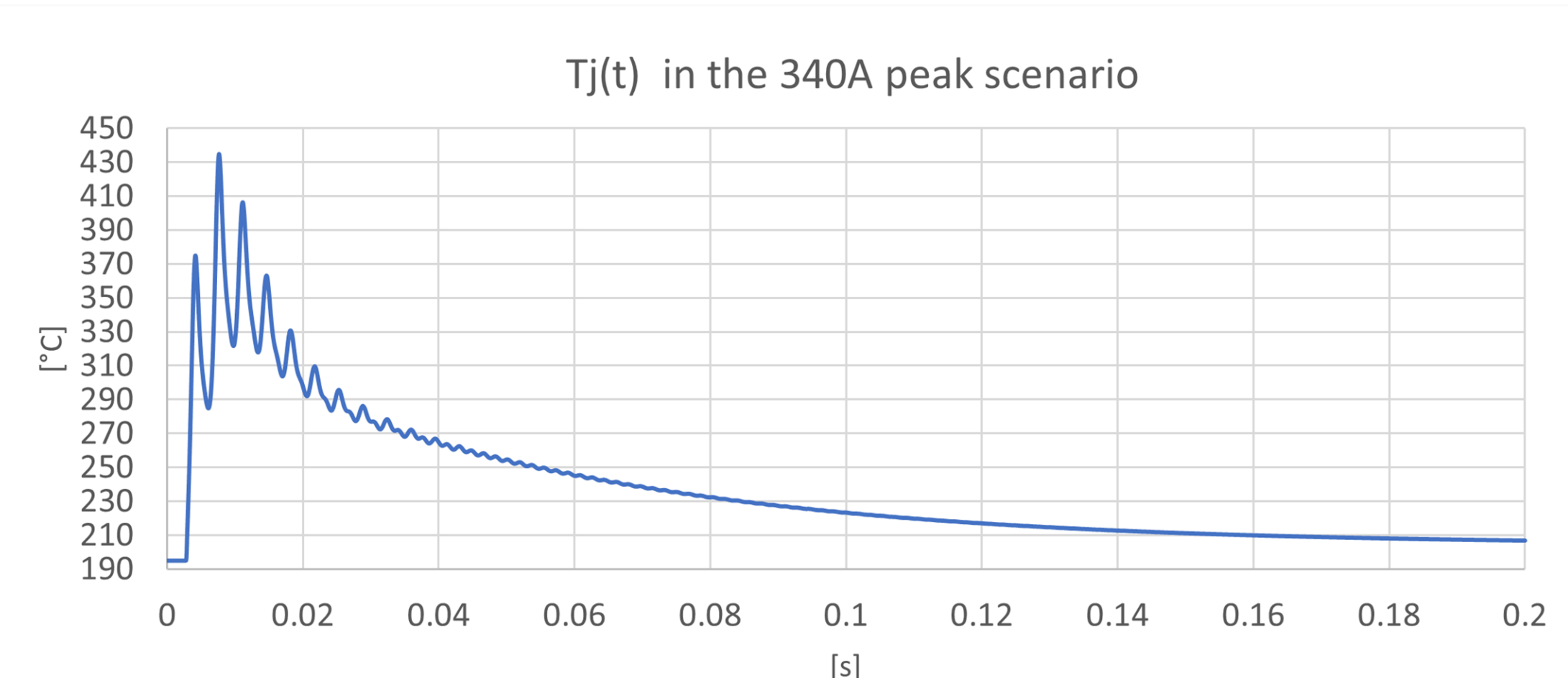
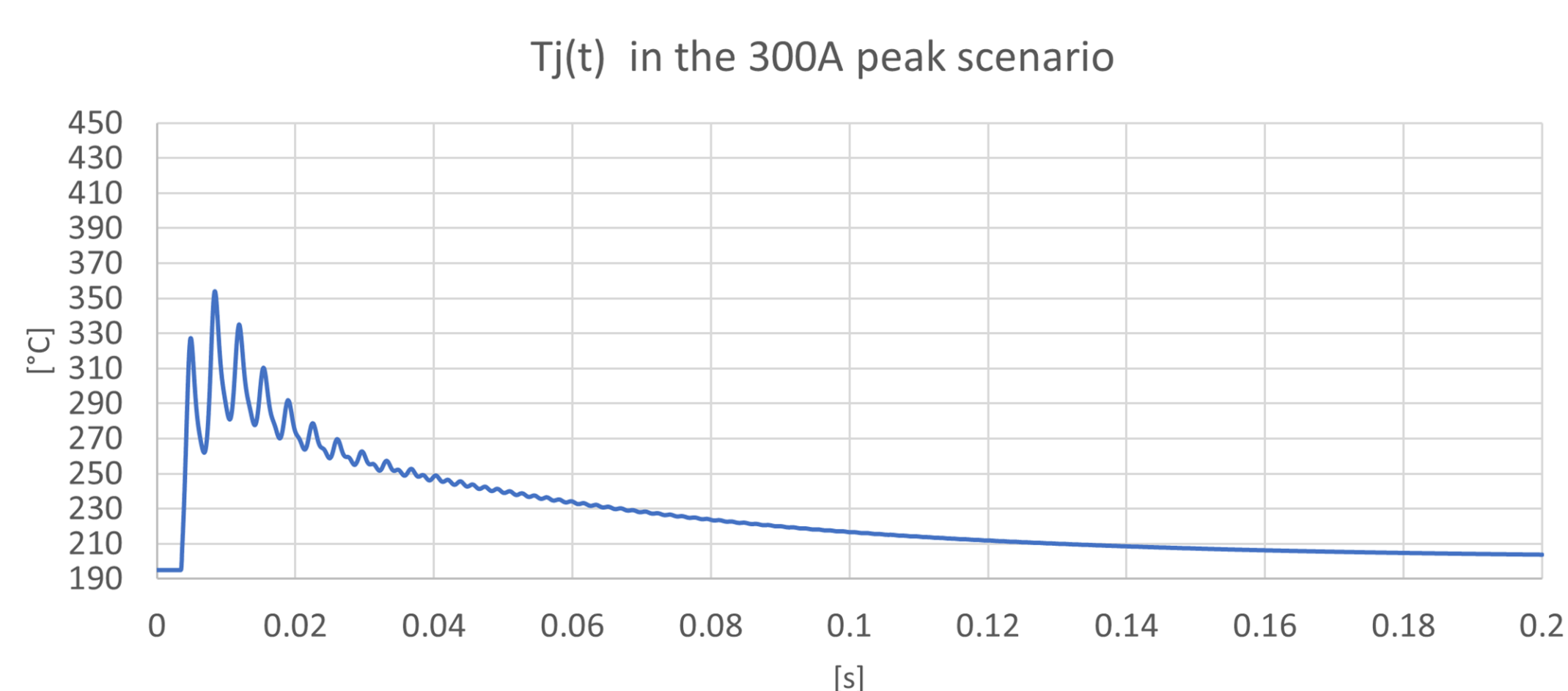


The simulated V_{ds} is compared with the measured one for each case as reported in the figures below. As the tested and simulated V_{ds} match very closely, we can conclude that the methodology is effective and it is therefore possible to evaluate the internal temperature using a voltage probe on the pin Tj, where 1 V represents 1 °C.

Measured data vs Simulation results



Simulated temperature profiles



Conclusion

Starting from the measured output iso-temperature characteristics and the thermal impedance of the device, a new SPICE model has been developed to allow the simulation of various tests at extreme conditions in terms of temperature, current, and drain-source voltage, estimating the internal temperature and thereby evaluating whether or not the power device is able to withstand specific conditions, as well as its overall reliability. The effectiveness of the methodology has been verified experimentally with a specific ASC current transient on a 750 V 150 A SiC MOSFET.