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Comprehensive Board Level Temperature Cycling Lifetime Projection of WLCSP GaN Power Devices

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Abstract

Wafer level chip scale packaged (WLCSP) gallium nitride (GaN) power devices have been deployed in increasingly advanced applications that demand high board-level temperature cycling (TC) reliability. In this study, a comprehensive TC lifetime model is developed, accounting for different device sizes and varying land grid array (LGA) solder bump dimensions. COMSOL finite element analysis (FEA) simulations were conducted to model the characteristic TC lifetime based on solder fatigue wear-out mechanism. The simulated results agree with the experimental data, validating the proposed TC lifetime model.

TC Experiment

Five WLCSP GaN transistors with various dimensions are evaluated for TC reliability

- EPC2206, EPC2071, EPC2069, EPC2218 and EPC2204.

TC experiment parameters are kept consistent:

- PCB boards – 2-layer Cu, 1.6 mm thick Cu board
- SAC305 solder stand off height consistent after assembly
- Temperature cycle conditions T_{max} = 125°C, T_{min} = -40°C with dwell time of 10 mins

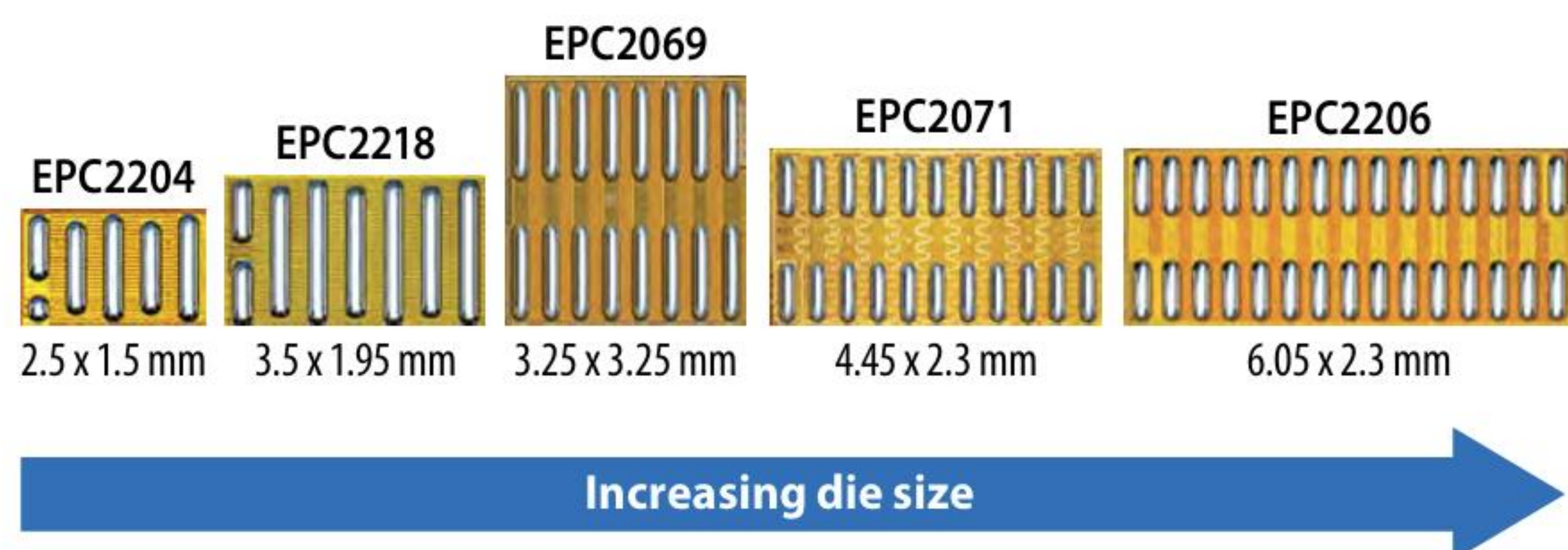


Fig. 2. Five GaN devices scaled to size tested including EPC2206, EPC2071, EPC2069, EPC2218 and EPC2204.

TC Wear-out Mechanism

The CTE mismatch between the device, solder and PCB is the fundamental wear-out mechanism.

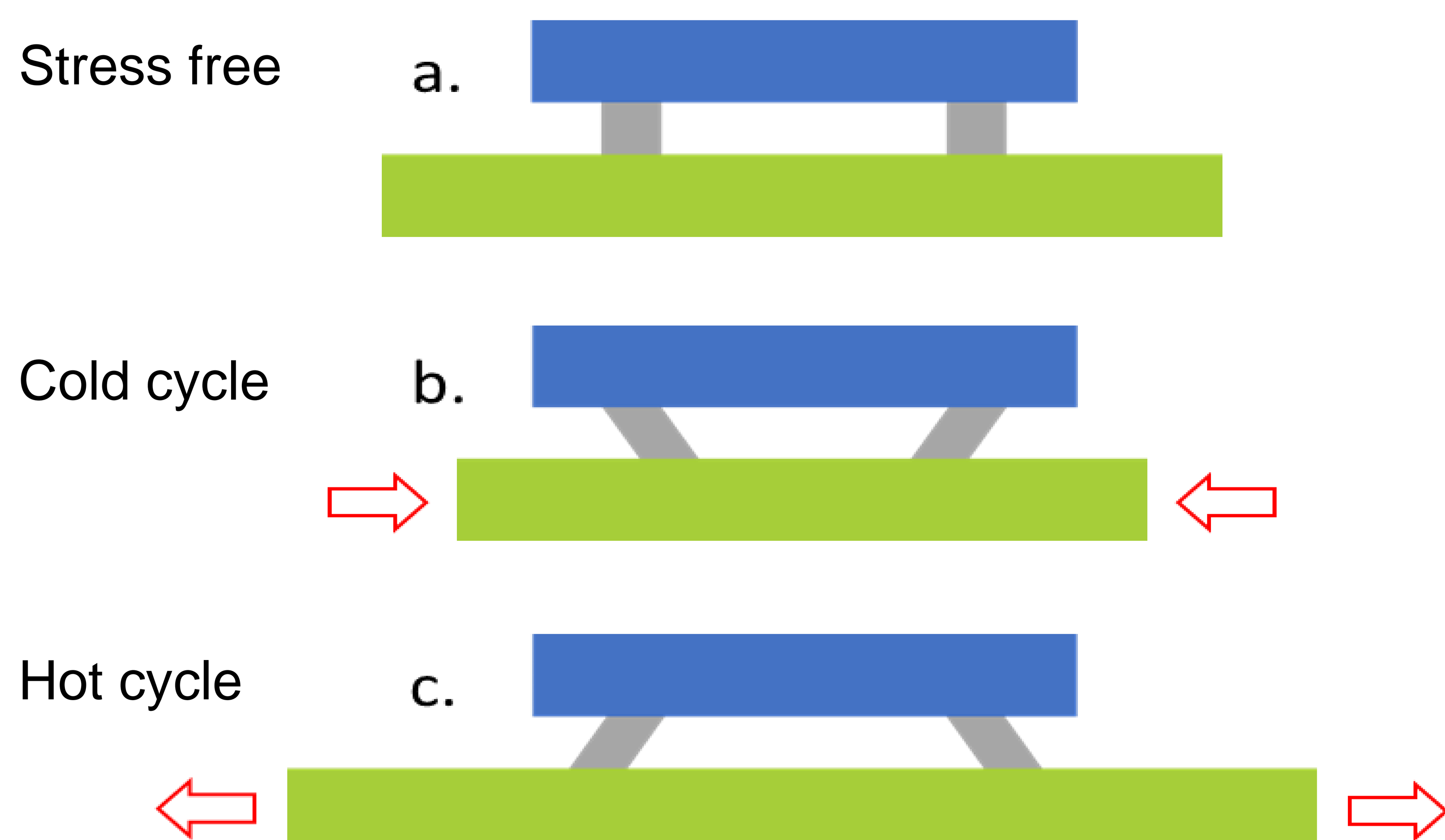
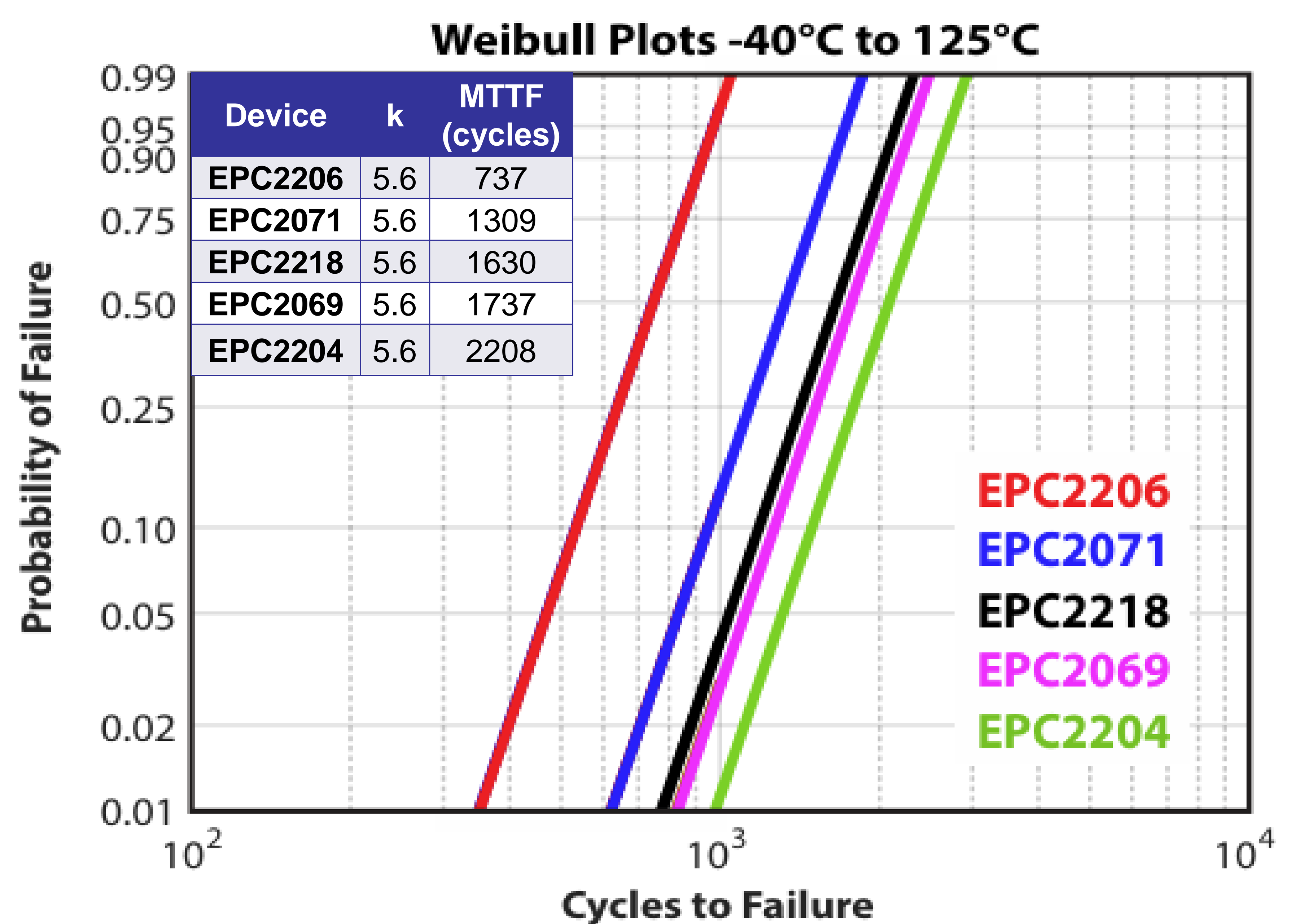


Fig. 1. (a) Neutral stress-free condition; (b) Contraction during a cold cycle; (c) Expansion during a hot cycle.

Weibull Distribution Analysis



Device	k	MTTF (cycles)
EPC2206	5.6	737
EPC2071	5.6	1309
EPC2218	5.6	1630
EPC2069	5.6	1737
EPC2204	5.6	2208

Fig. 3. Mean-time-to-fail (MTTF) calculated by Weibull distribution analysis for experimental TC data of five GaN devices.

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Failure Analysis

Solder joint cracking of the corner gate bump responsible for the TC failures, as shown in physical cross-section SEM Image.

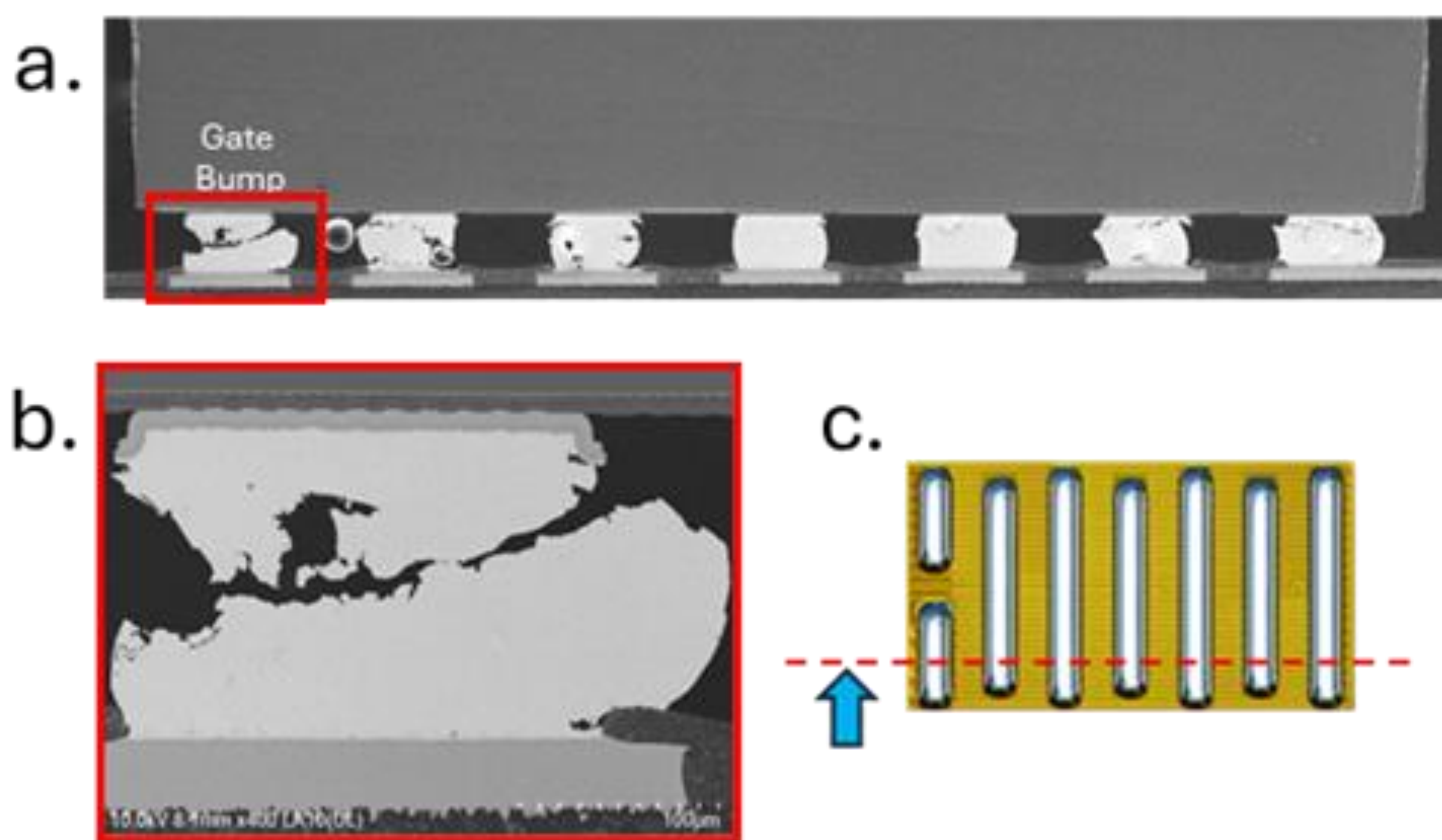

Fig. 4. (a) Cross-section of an EPC2218 TC failure; (b) worst solder joint cracking observed in the corner gate bump; (c) direction of the cross-section view.

Analysis

- TC MTTF is usually modeled by the Coffin-Mansion relation in literature

$$\mathrm{MTTF} \propto (\mathrm{DNP}^{\mathrm{Max}})^{-n} \text{ or Die Area}^{-n} \qquad \text{Eq. (1)}$$

- Neither Die Area or $\mathrm{DNP}^{\mathrm{Max}}$ provided a good fit

EPC2069, 10.56 mm²

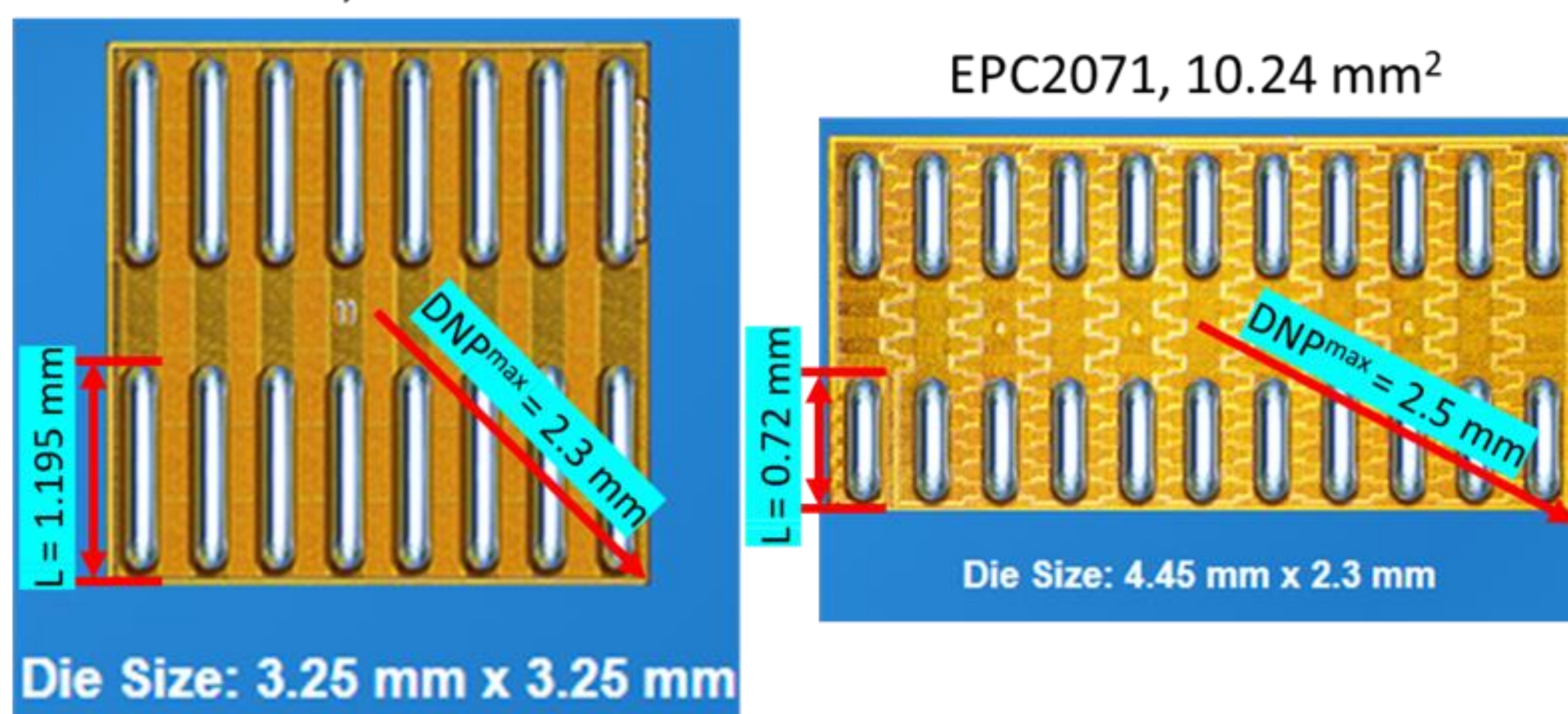

Fig. 5. Example of gate bump length (L) and $\mathrm{DNP}^{\mathrm{max}}$.

Device	MTTF (cycles)	Die Area (mm²)	L (mm)	$\mathrm{DNP}^{\mathrm{Max}}$ (mm)
EPC2071	1309	10.24	0.72	2.5
EPC2069	1737	10.56	1.195	2.3

Effective distance from neutral point ($\mathrm{DNP}^{\mathrm{eff}}$)

$$\mathrm{DNP}^{\mathrm{eff}} = \mathrm{DNP}^{\mathrm{Max}} + a \times L \qquad \text{Eq. (2)}$$

- $\mathrm{DNP}^{\mathrm{max}}$ = Distance from the neutral point (die center) to the farthest solder bump corner
- L = corner gate bump length

Incorporated in classic Coffin-Manson power law relation

$$\mathrm{MTTF} = A\left(\mathrm{DNP}^{\mathrm{eff}}\right)^{-n} = A\left(\mathrm{DNP}^{\mathrm{Max}} + a \times L\right)^{-n} \qquad \text{Eq. (3)}$$

- The coefficient, a is determined to be -0.65 based on the best fit.
- The power exponent, n is found to be -1.4, which is consistent with literature reported values in the range $-2 \leq n \leq -1$.

COMSOL Finite Element Analysis (FEA) Simulation

- Deveraux's energy-based fatigue model was used in FEA simulation, shown in Eq. (4)

$$\mathrm{MTTF} = K_1 \Delta W^{K_2} + \frac{L}{K_3/\Delta W^{K_4}} \qquad \text{Eq. (4)}$$

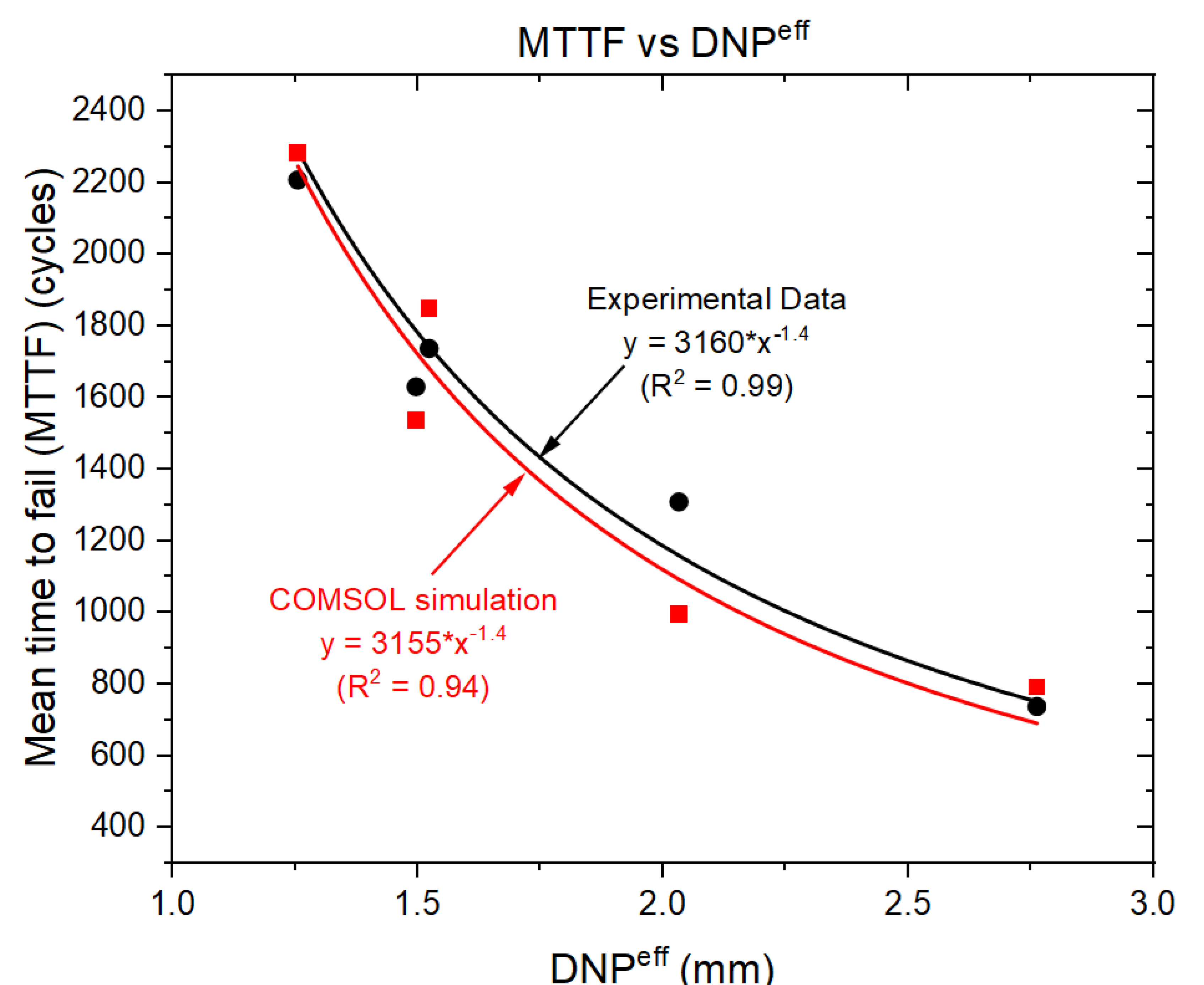

Fig. 6. Good agreement found between the COMSOL FEA simulation and TC experiment.