A Harmonic Current Suppression Method for PMSM Based on Model Predictive Current Control

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ABSTRACT

This paper introduces a harmonic current suppression (HCS) strategy utilizing dual-vector model predictive current control (DV-MPCC) to mitigate the issue of elevated harmonic currents resulting from a reduced switching frequency in Permanent Magnet Synchronous Motors (PMSMs). First, the number of switching actions of the inverter at future moments is evaluated and limited to reduce the switching frequency of the inverter. Second, by employing a simple calculation method, the harmonic components induced by the reduced switching frequency are separated from the predicted current. These components are then embedded as one of the performance indicators in the cost function so that high-performance predictive control can be achieved even with reduced switching frequency. Finally, the effectiveness of the proposed method is validated through simulation experiments.

The Theory of Proposed HCS-SFL-MPCC Method

A. Switching Frequency Limitation

To reduce the switching frequency between neighboring VVs in a dual-vector, the following function is designed

$$f_1 = \left| S_{abc}^2(k-1) - S_{abc}^1(k) \right| \tag{1}$$

$$f_2 = \left| S_{abc}^1(k) - S_{abc}^2(k) \right| \tag{2}$$

where f_1 denotes count of switching operations between the second VV at the $(k-1)^{th}$ instant and the first VV at the kth instant. f_2 denotes the count of switching operations between the two adjacent VVs during the sampling period at k^{th} instant.

According to the T-DV-MPCC method, the selection of the first and second VVs is still based on minimizing the cost function. Additionally, the switching states between adjacent VVs need to be considered as a constraint. Therefore, the cost function for selecting the first and second optimal VVs can be designed as

$$J_1 = \left[i_d^* - i_{d1}^p(k+1) \right]^2 + \left[i_q^* - i_{q1}^p(k+1) \right]^2 + H_1 f_1 \tag{3}$$

$$J_2 = \left[i_d^* - i_{d2}^p(k+1) \right]^2 + \left[i_q^* - i_{q2}^p(k+1) \right]^2 + H_2 f_2 \tag{4}$$

where H_1 and H_2 denotes the weighting factor between current difference and number of switches. Since both H_1 and H_2 in J_1 and J_2 are designed to balance the order-of-magnitude relationship between the current and the quantity of switching actions, it can be assumed that $H_1=H_2=H$.

B. Harmonic Current Suppression

It should be noted that when the switching frequency constraint is applied to reduce the inverter's switching frequency, errors occur between the synthesized VV and the exact synthesized VV, leading to degraded system control performance and a significant increase in harmonic current components. To address this issue, this paper first uses a low-pass filter to separate harmonic currents from the predicted currents. Then, the harmonic components are directly embedded as one of the performance indicators in the cost function for constraint. The specific steps are as follows.

a) Harmonic Extraction

Using a low-pass filter to isolate the fundamental component from the predicted currents under the action of the eight synthesized VVs, denoted as

$$i_{sf}^p(k+1) = \gamma \cdot i_{sf}^p(k) + (1-\gamma) \cdot i_{s2}^p(k+1) \tag{5}$$

where γ denotes the fundamental wave current component of the predicted current at $(k+1)^{th}$ instant and k^{th} instant, respectively. And the coefficients of the filter are set to 0.9.

Then, the harmonic current in the predicted current is determined by the discrepancy between the predicted current and the fundamental current , denoted as

$$i_{sh}^p(k+1) = i_{s2}^p(k+1) - i_{sf}^p(k+1) \tag{6}$$

a) Harmonic Suppression

The obtained harmonic current components are introduced into equation (4) to reduce the harmonic currents generated when the switching frequency is reduced. Therefore, equation (4) is extended to

$$J_2 = \left[i_d^* - i_{d2}^p(k+1) \right]^2 + \left[i_q^* - i_{q2}^p(k+1) \right]^2 + H_2 f_2 \tag{7}$$

$$+ M \left[\left(i_{dh}^p(k+1) - 0 \right)^2 + \left(i_{qh}^p(k+1) - 0 \right)^2 \right] \tag{8}$$

where M denotes the value of the weighting factor among the current derivative and the harmonic currents, and M is set to 1. The core idea control graph of the proposed HCS-SFL-MPCC methodology is shown in Fig. 1.
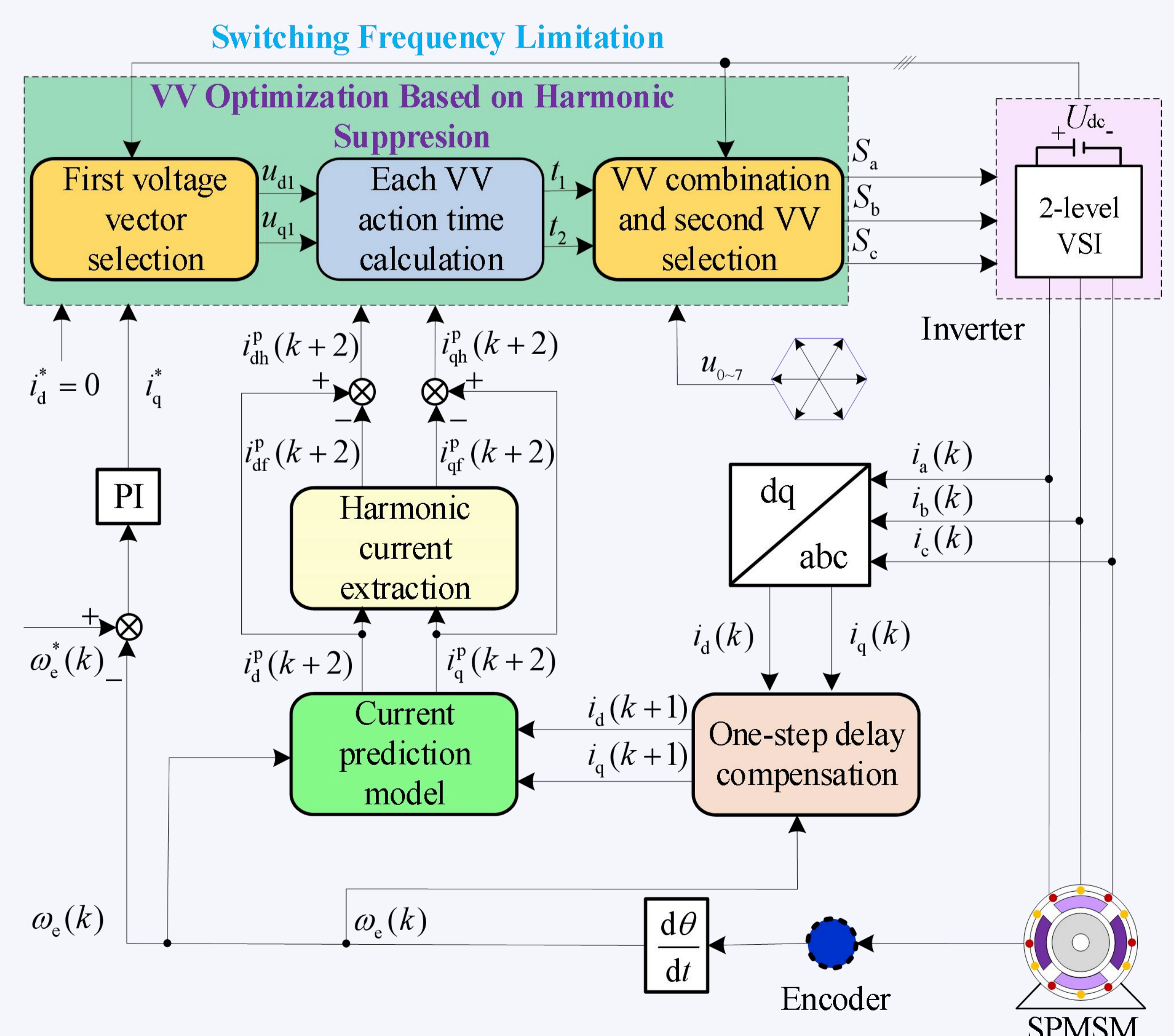

Fig. 1. Control schematic diagram of the proposed HCS-SFL-MPCC method.

Experimental Results

To verify the effectiveness of the proposed HCS-SFL-MPCC method in this paper, this section designs relevant simulation experiments. For clarity in subsequent discussions, this paper will refer to the method of restricting switching frequency using T-DV-MPCC alone as Method-I. Method-II, which incorporates harmonic suppression (i.e., the proposed HCS-SFL-MPCC method), builds upon Method-I. It should be noted that the coefficients for the switching frequency constraint is the identical for either method, with $H_1 = H_2 = H = 1.5$.

Firstly, the steady-state performances of the two methods are evaluated and compared at rated torque and different speed conditions, as depicted in Figs. 2-3.
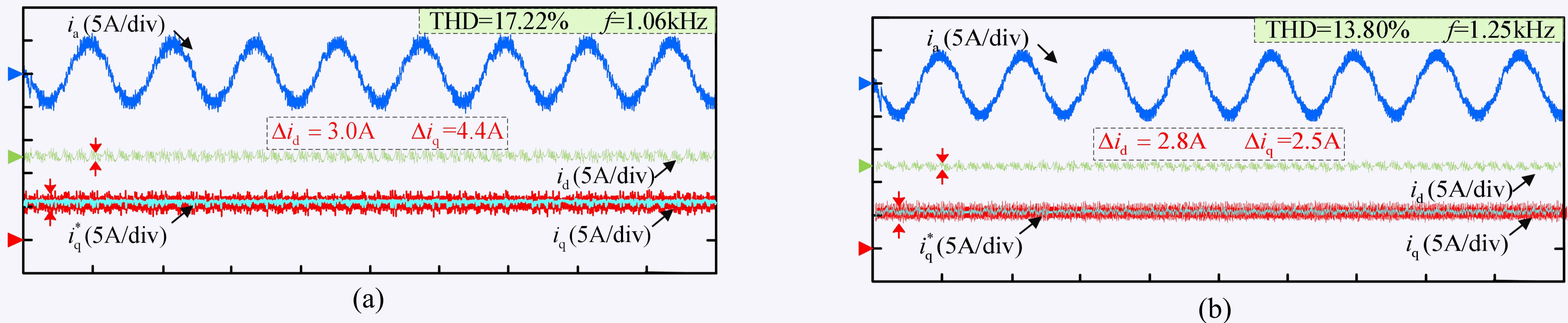

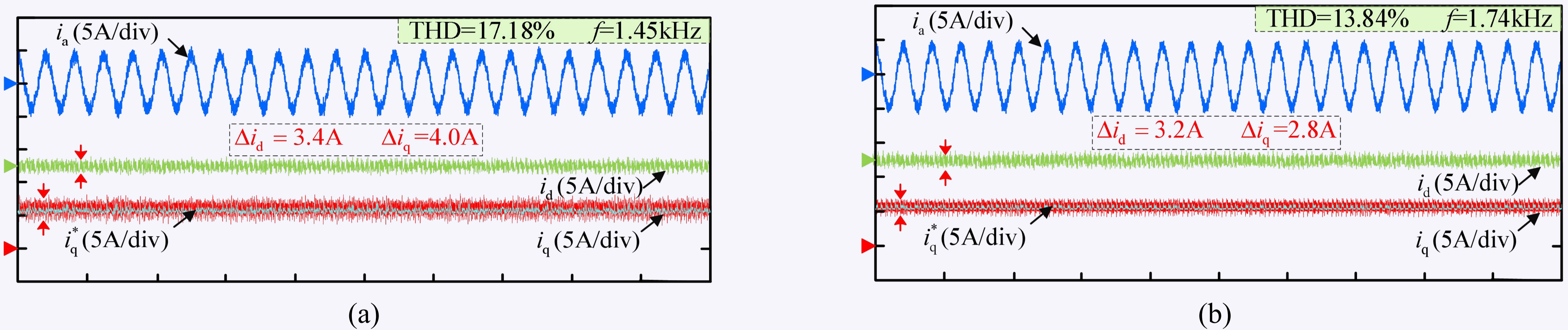**Fig. 2.** Simulation results at rated load and speed of 500 rpm, (a) Method-I, (b) Method-II.

Fig. 3. Simulation results at rated load and speed of 1500 rpm, (a) Method-I, (b) Method-II.

When the switching frequency is reduced, the total harmonic distortion (THD) of the currents in Method-I is 17.22% at 500 r/min and 17.18% at 1500 r/min, accompanied by significant dq-axes current ripple. However, Method-II effectively mitigates the negative impact of reduced switching frequency on the system. It reduces the THD of Method-I to 13.80% and 13.84% at 500 r/min and 1500 r/min, respectively. Similarly, the dq-axes current ripple is also reduced.

To prove more about the advantages of the proposed method in harmonic suppression, this paper also compares the dq-axes current ripple of the two methods across the full speed range under rated torque, as shown in Fig. 4.
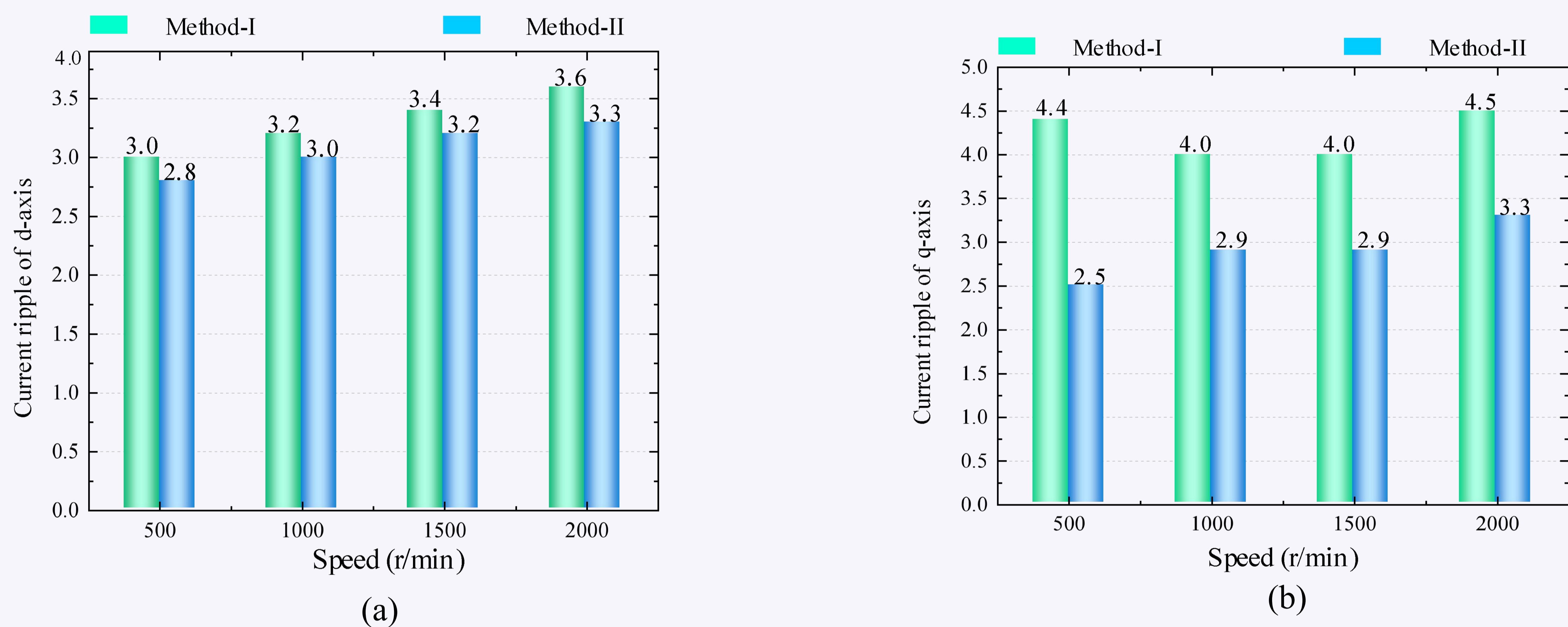

Fig. 4. Comparison plot of current ripple between Method-I and Method-II across full speed range. (a) d-axis. (b) q-axis.

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CONCLUSION

To mitigate the harmonic current components caused by reduced switching frequency in the MPCC, this paper proposes a harmonic current suppression MPCC method applied to switching frequency limitations. This method achieves reduced switching frequency by restricting the conduction states of the inverter at different instances. Simultaneously, it predicts and extracts the harmonic current components corresponding to each inverter switching state. These harmonic currents are then introduced into the cost function as one of the performance indicators for the entire system, facilitating rolling optimization. This method equalizes the relationship among switching frequency and harmonic currents. Finally, simulation results validate the effectiveness of the proposed method.