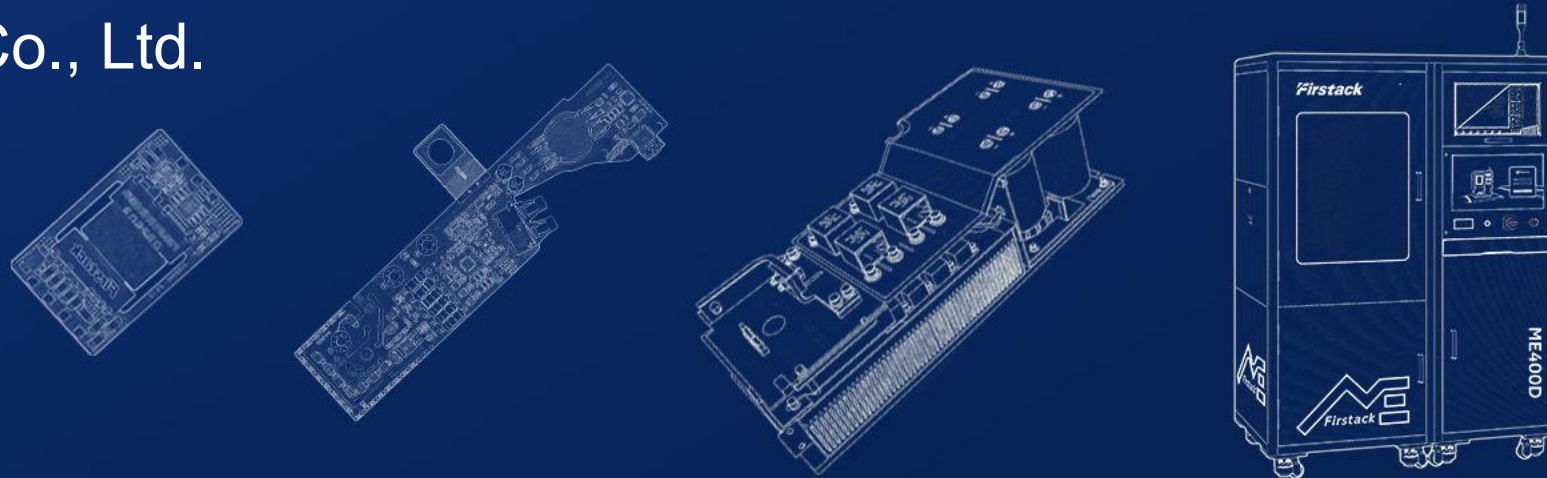


Ultra-Low Static Loss Achieved by IGBT Gate Voltage Enhancement

Firstack Technology Co., Ltd.

Zhe Chen 25/8/2026



目录

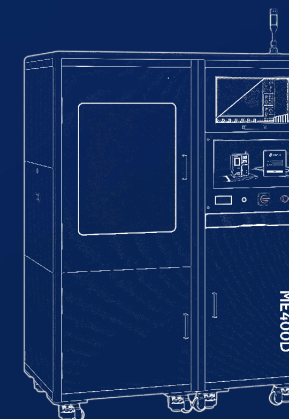
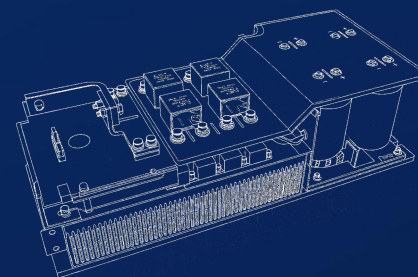
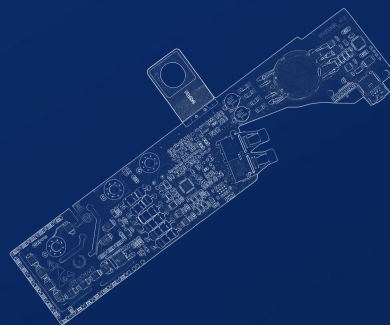
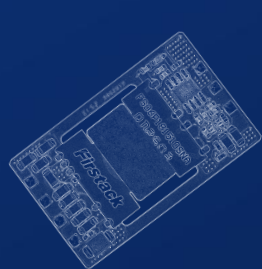
CONTENTS

01 Company Introduction

02 Enhanced Efficiency and Reliability

01

Company Introduction



Firststack at a glance

FIRSTSTACK

2011

Founded

~6M+

Shipment

No.1

China

~500+

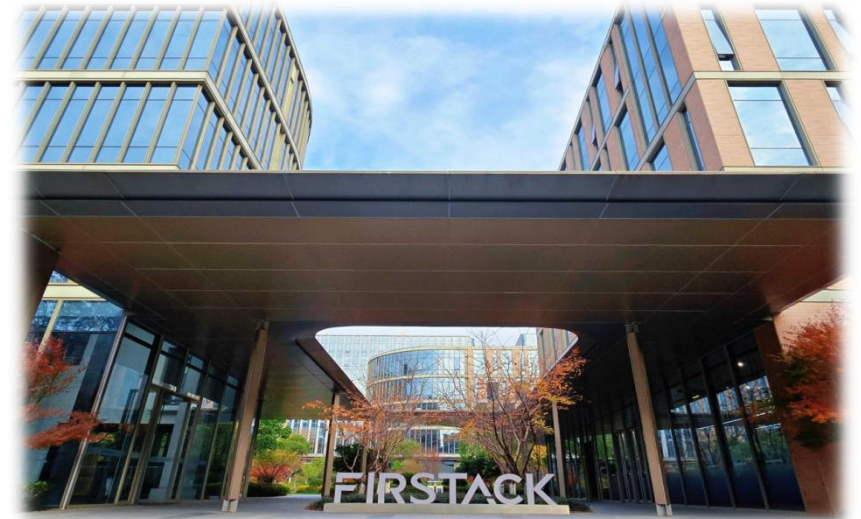
Employees

150+

IPs

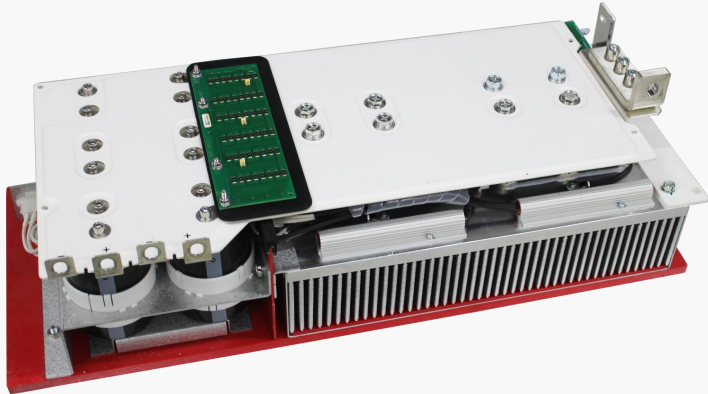


HQ & Mfg. Site: Linping, Hangzhou

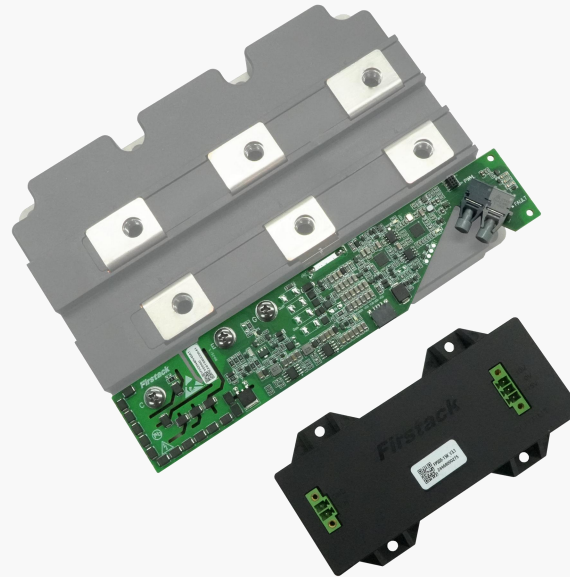


Office: Shangcheng, Hangzhou

Power Stack



Driver



Test Equip.



Bridging devices to system

End-to-End Manufacturing: From PCBA to System Integration

PCBA Production



System Assembly

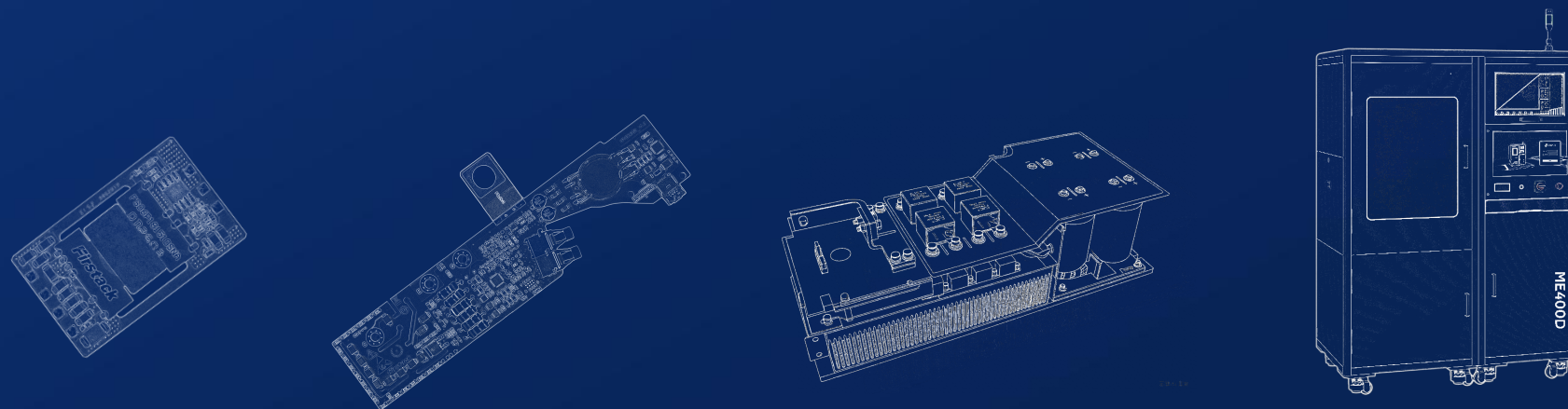


System Testing & Ageing



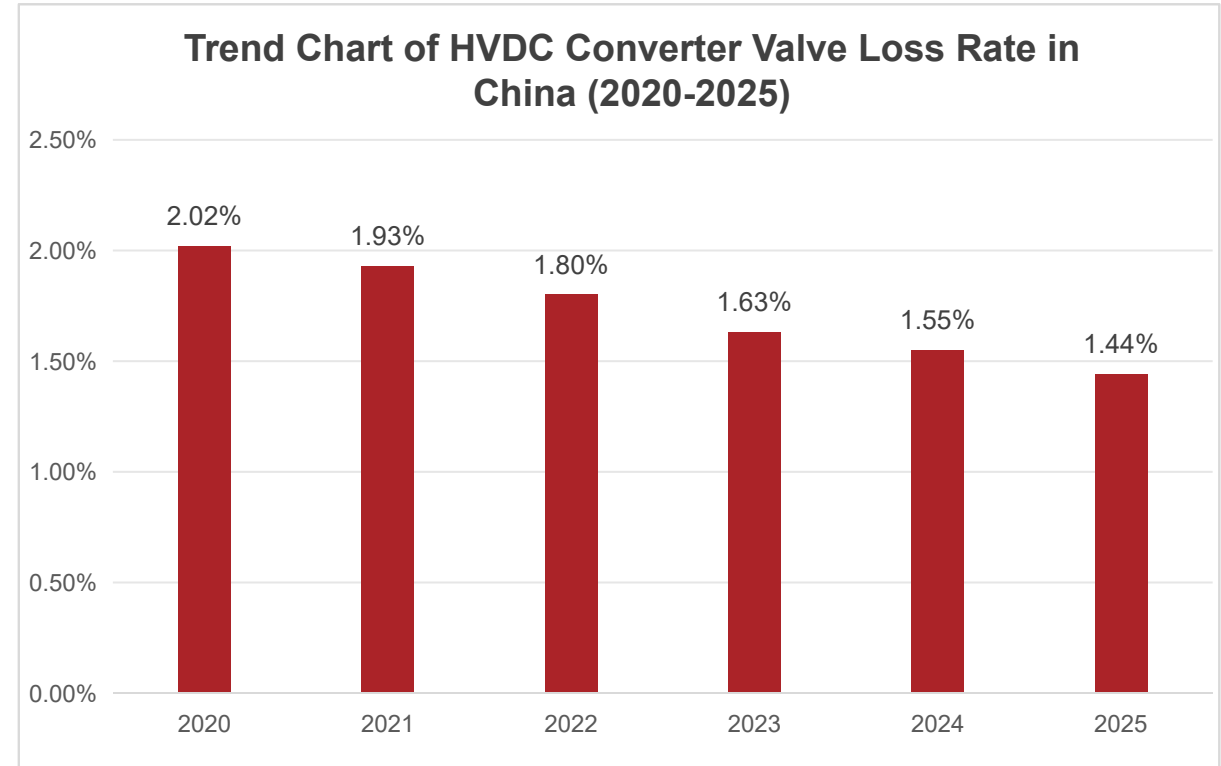
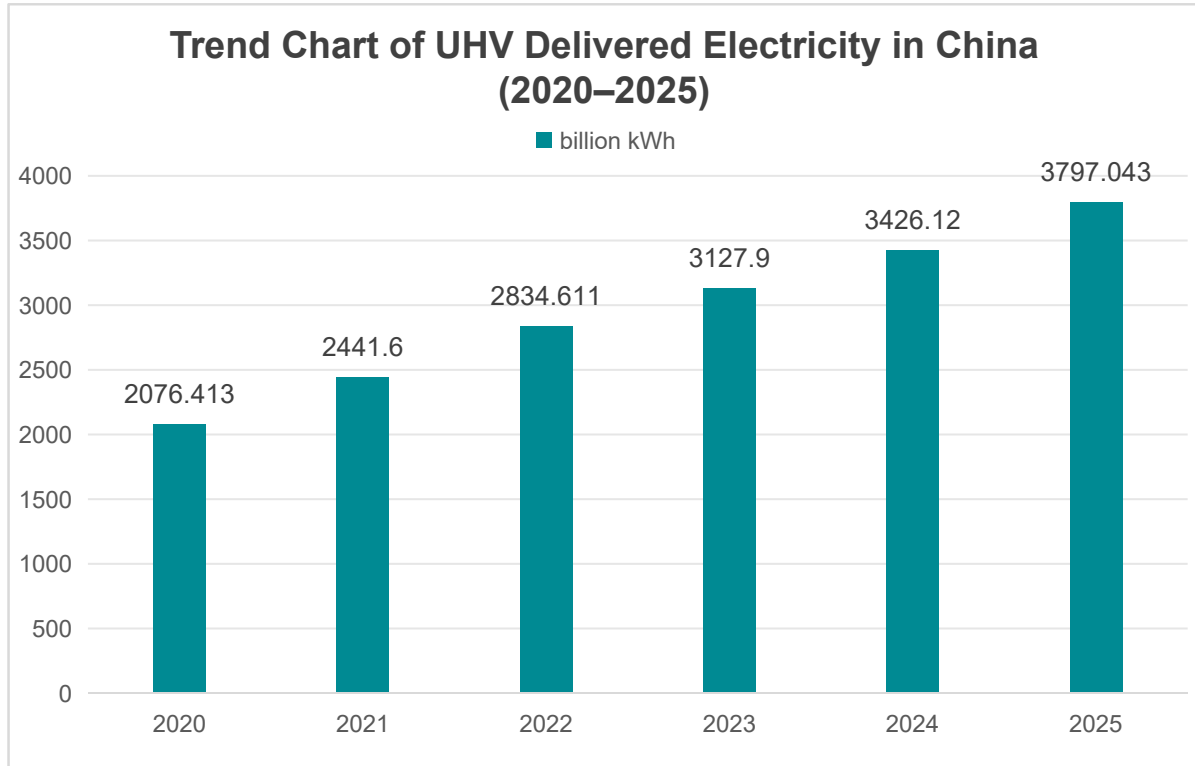
02

Enhanced Efficiency and Reliability





Energy Loss of HVDC

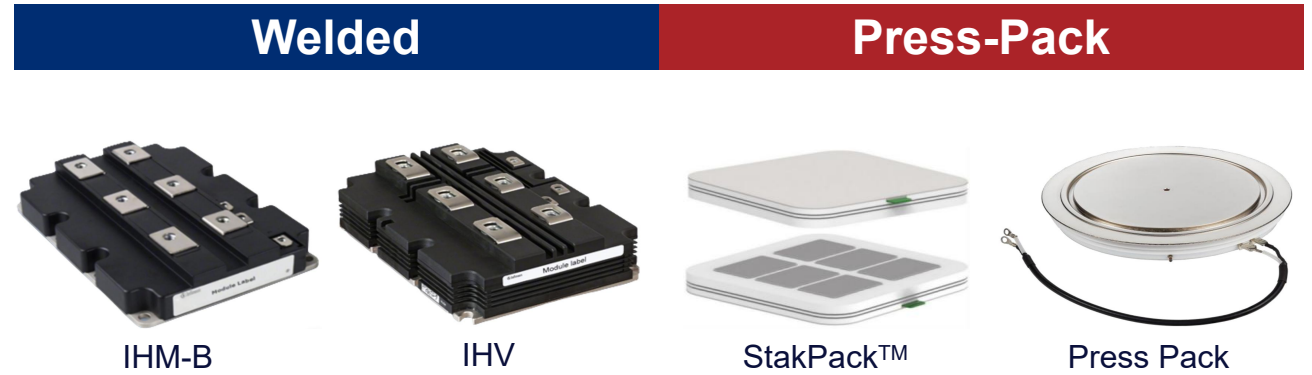
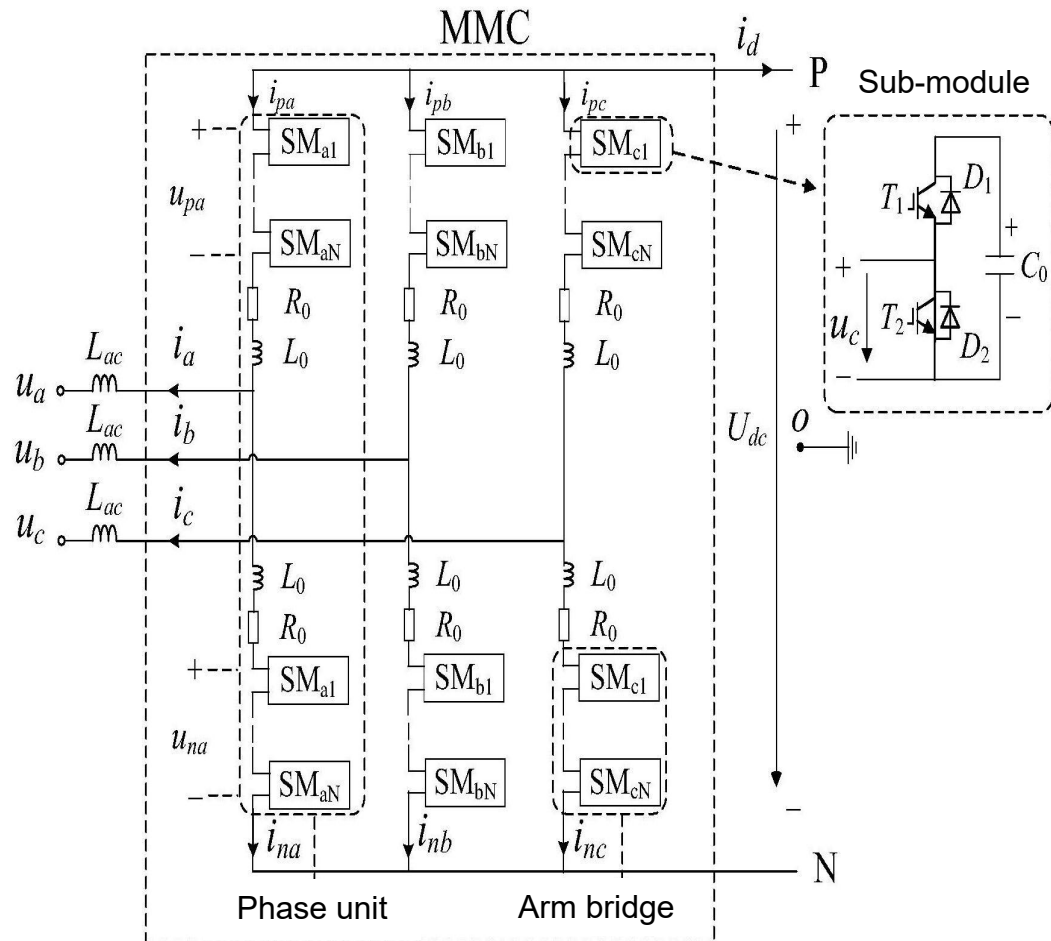


Resource: 中商产业研究院发布的《[2024-2030年中国特高压设备市场调查与行业前景预测专题研究报告](#)》

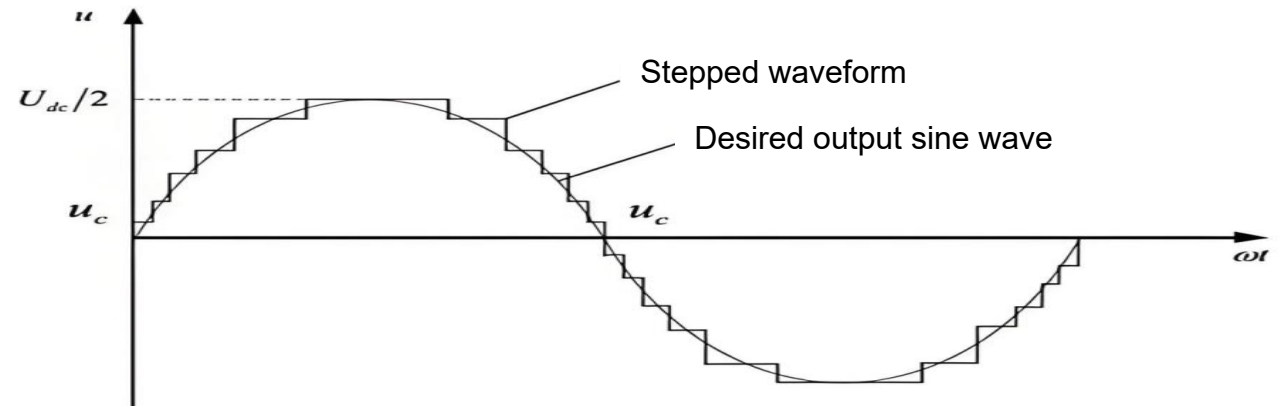
In 2025, the power loss of HVDC converter valves in China reaches **54.677 billion kWh**, equivalent to approximately **2.7 billion dollar (0.05 \$ /kWh)**.



Topology of HVDC

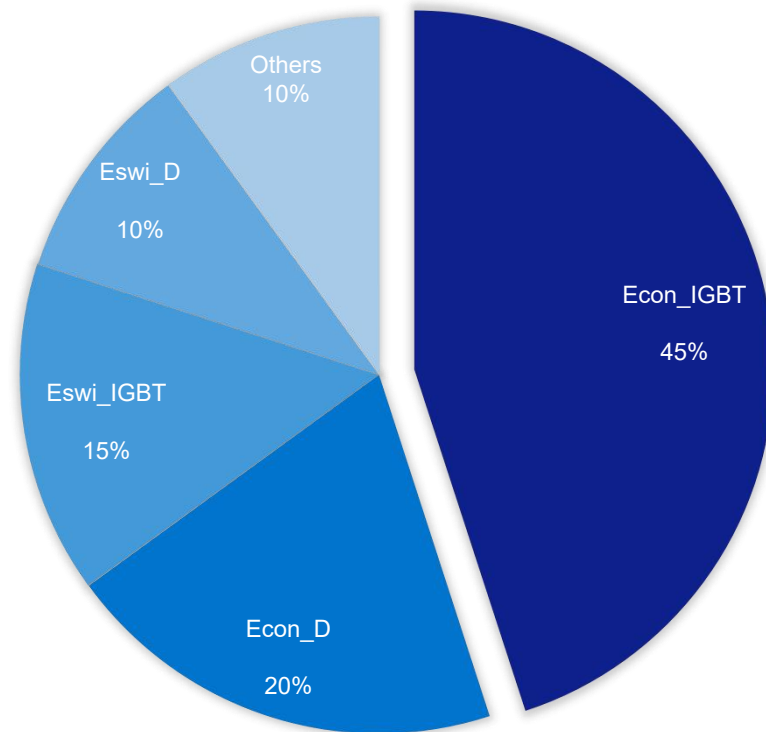


Nearest Level Approximation Modulation (NLM)



VSC-HVDC adopt Modular Multilevel Converter, the frequency is about 100~300Hz

Proportion of Losses in the Converter Valve



$$P_{con} = V_{cesat} * I_c$$

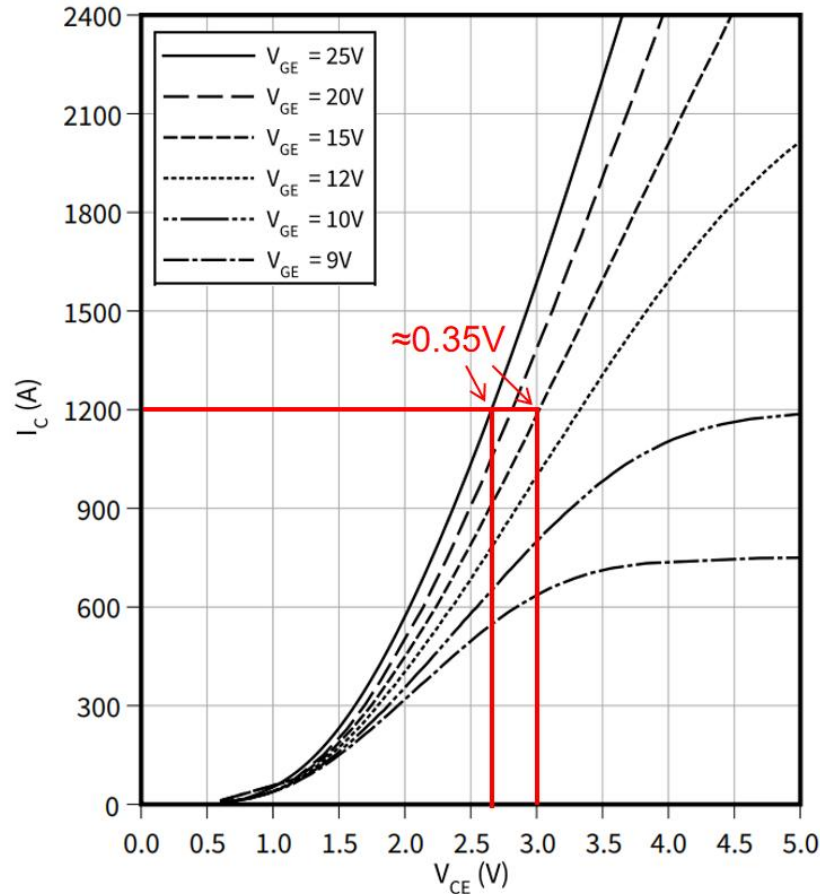
1. Forward voltage drop of the PN junction
2. Voltage drop caused by the residual resistance in the high-voltage N⁻ drift region
3. MOS channel, current spreading region, metallization, bond wires, and other parasitic resistances

Resource: 潘武略,徐政,张静,王超.电压源换流器型直流输电换流器损耗分析[J].中国电机工程学报,2008,28(21):7-14.

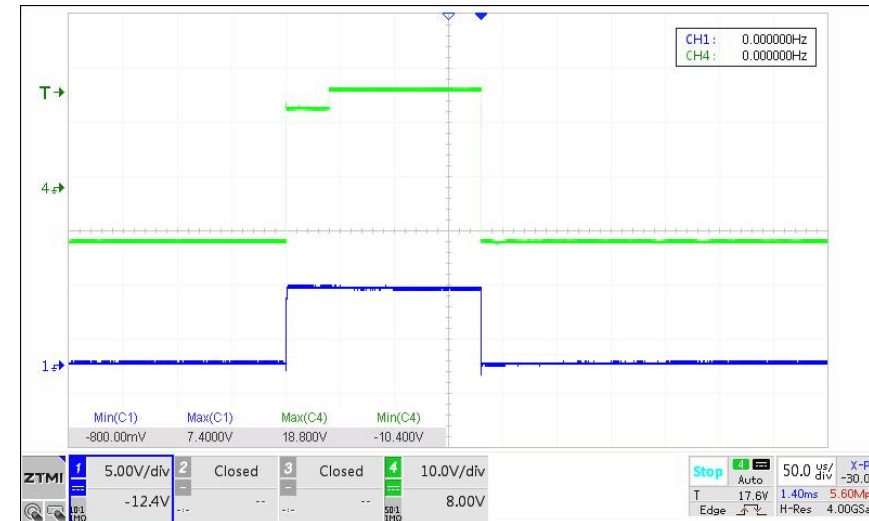
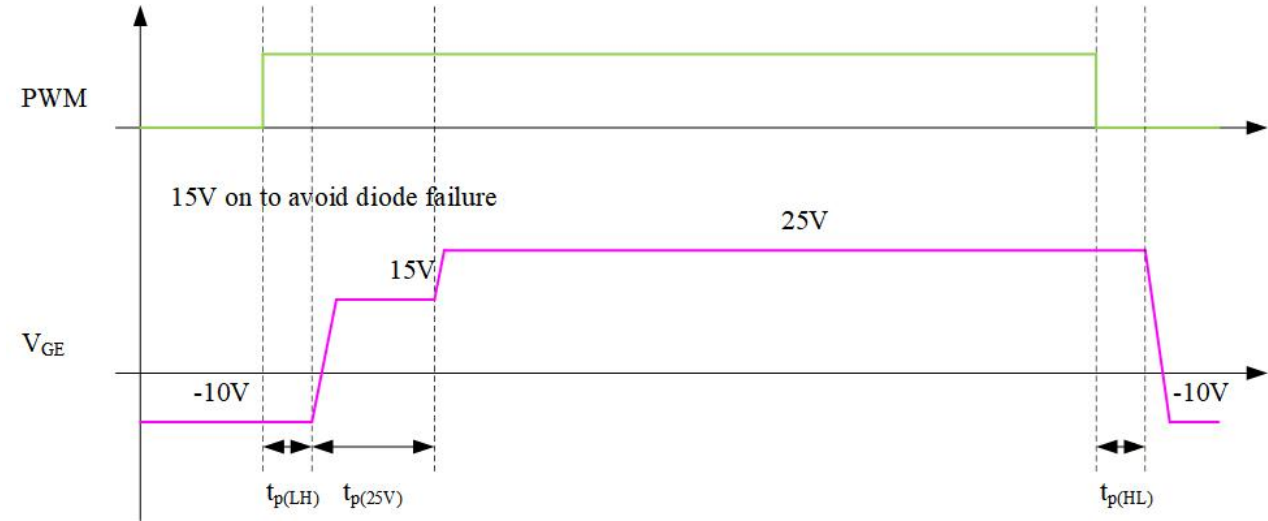
1% decreasing of the Econ saving ca. **12 million \$**

$V_{CE} = f(V_{GE})$

Datasheet of FZ1200R45HL3_S7



The IGBT's saturation conduction voltage drop was reduced by 0.35 V when the gate voltage increased from 15 V to 25 V, @ $I_C=1200$ A, 150°C

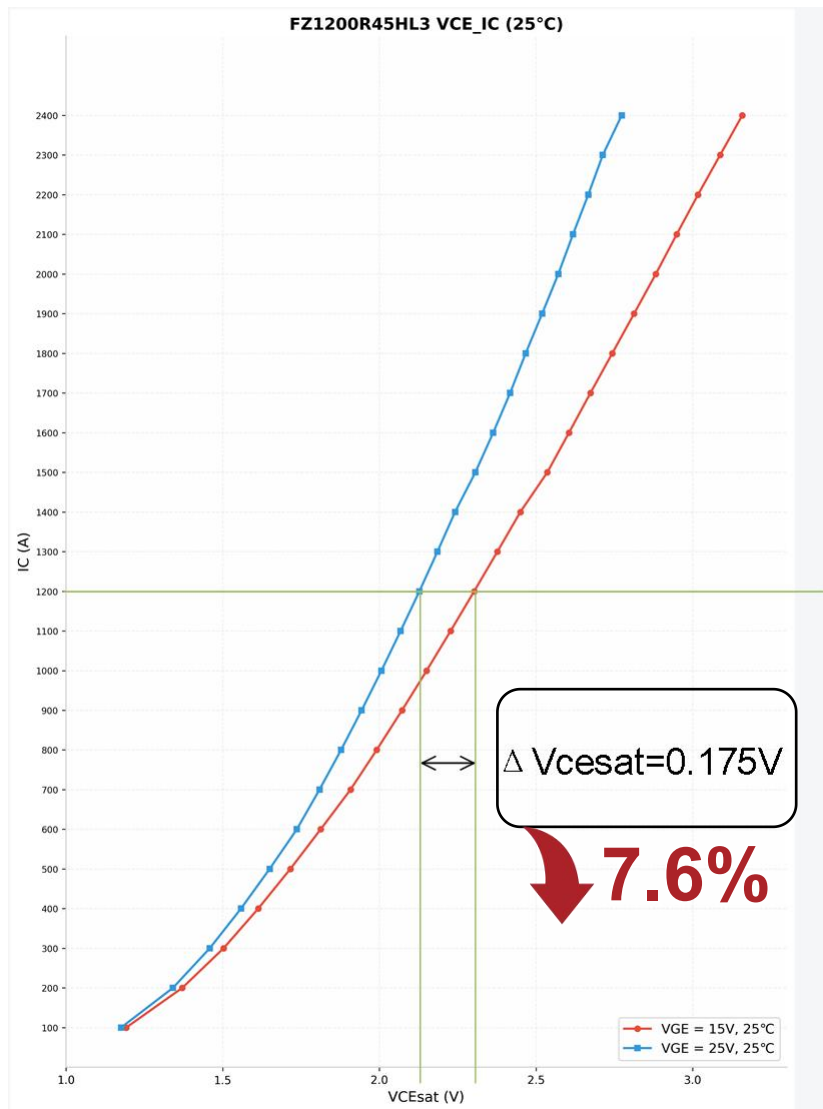


CH1: PWM
CH4: V_{GE}

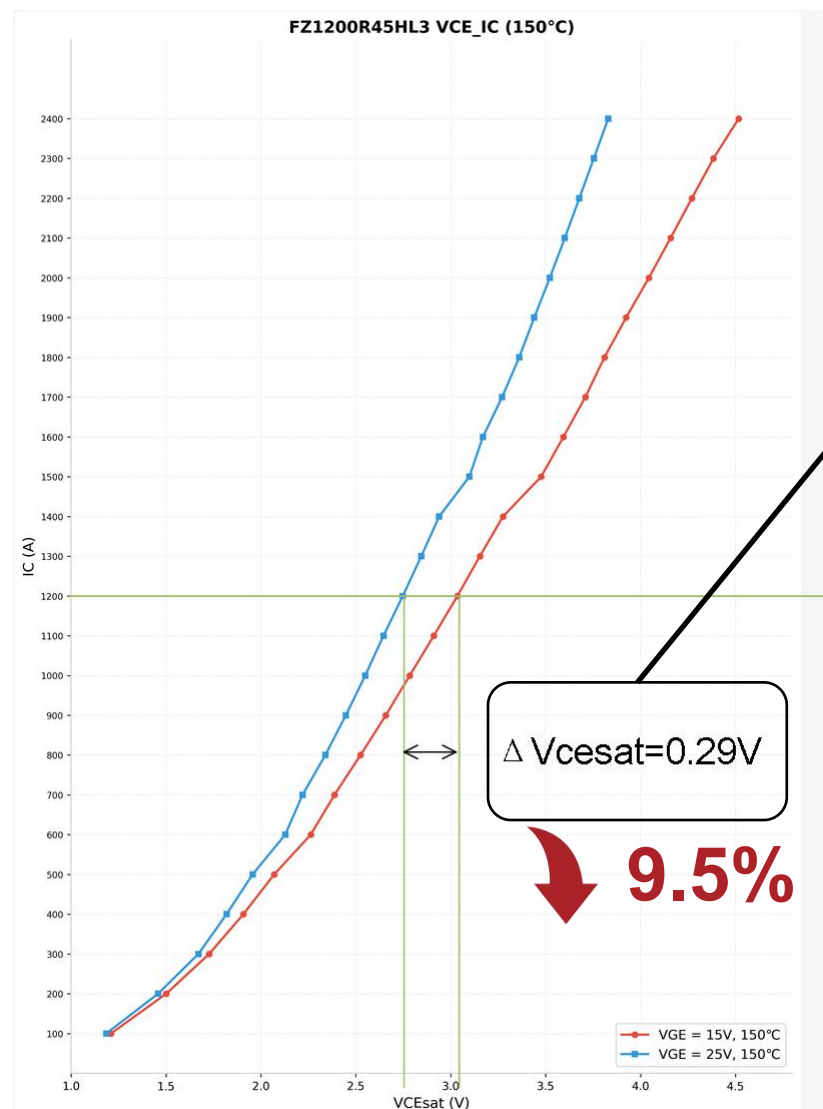
The conduction loss can be decreased by approximately **12% (144 million \$)**



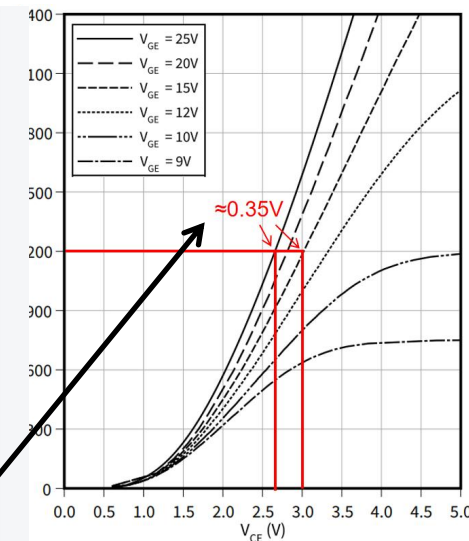
Actual measured V_{CEsat}



$\Delta V_{cesat} = 0.175V @ I_C = 1200A \& 25^\circ C$



$\Delta V_{cesat} = 0.29V @ I_C = 1200A \& 150^\circ C$



Close to data sheet

$$P_{SC} = f(I_c, \frac{di}{dt}, t_{sc}, M_p)$$

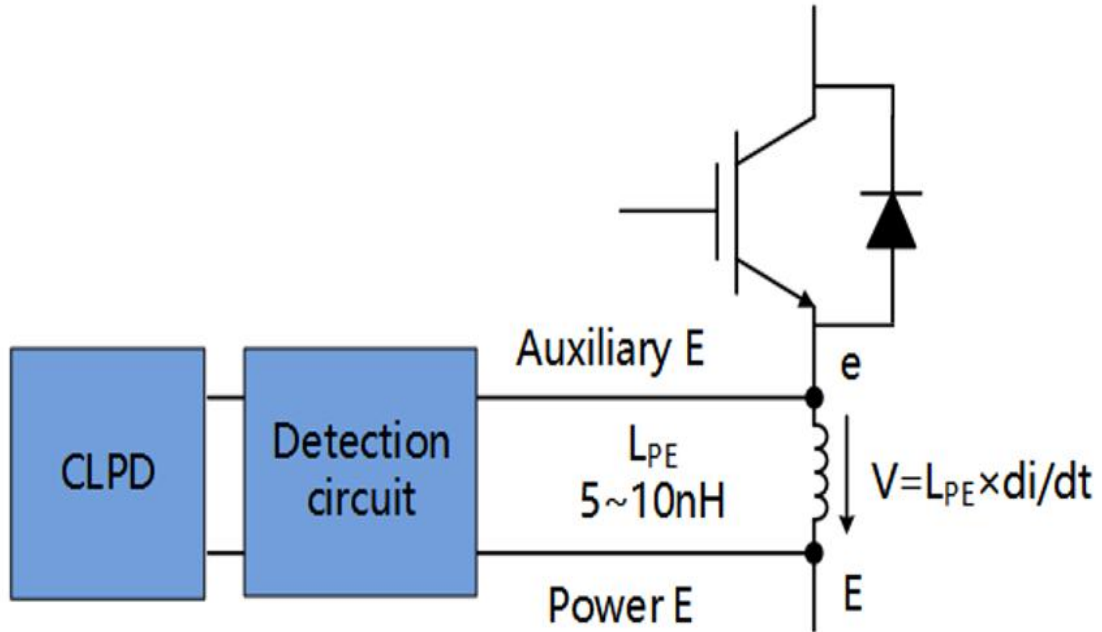
I_c : higher SC current means higher E_{sc}

t_{sc} : fast response is necessary

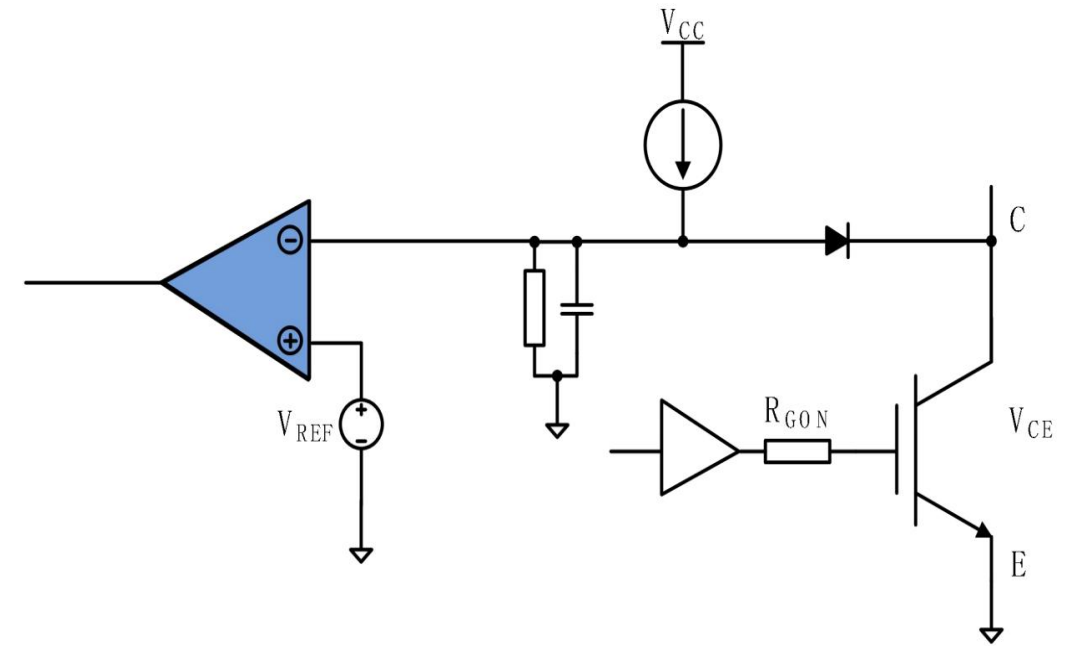
$\frac{di}{dt}$: which type of short circuit

M_p : protection margin, no false triggering

A reliable SC protection in HV system is not a simple matter



di/dt detection protection

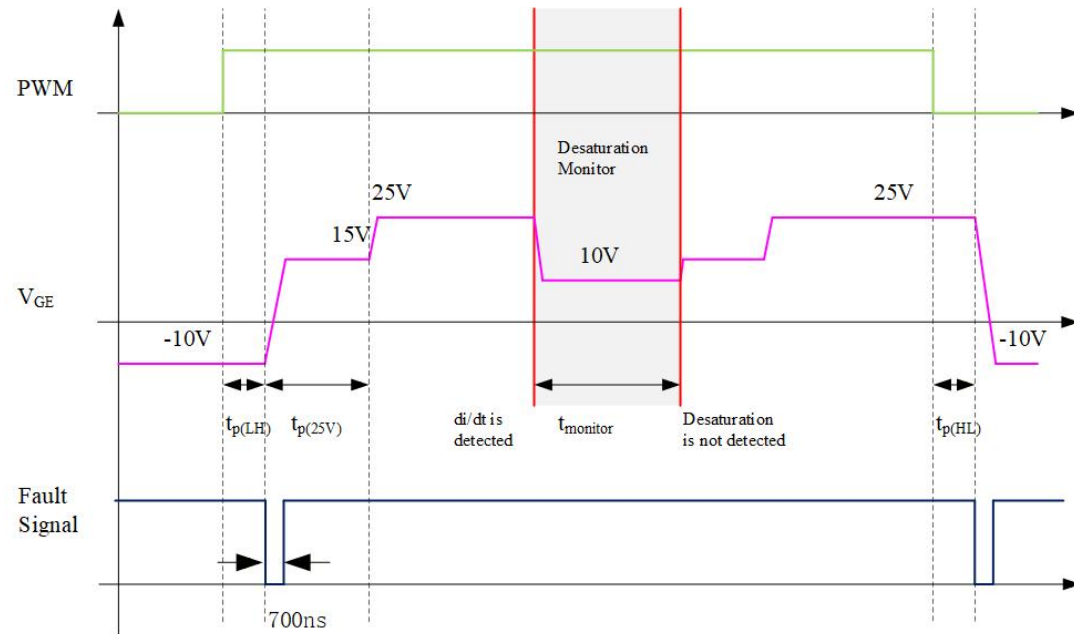


V_{CE} detection protection

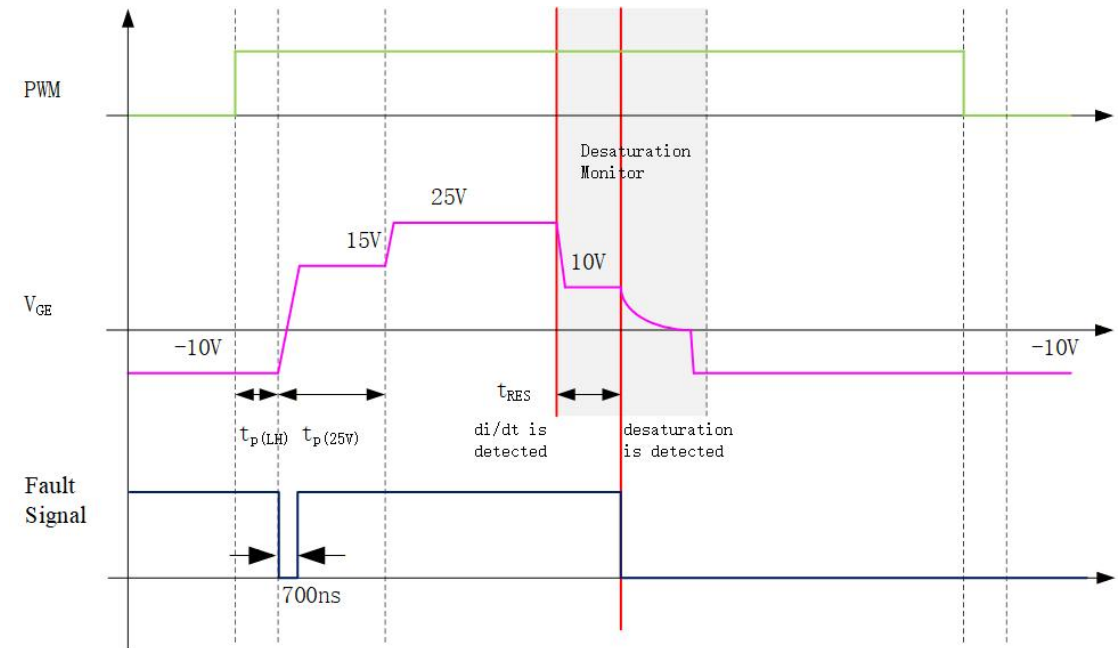
di/dt detection or V_{CE} detection alone is not sufficient to meet the SC protection requirements, what can we do?

Two-step SC protection: **di/dt + V_{CE} detection**

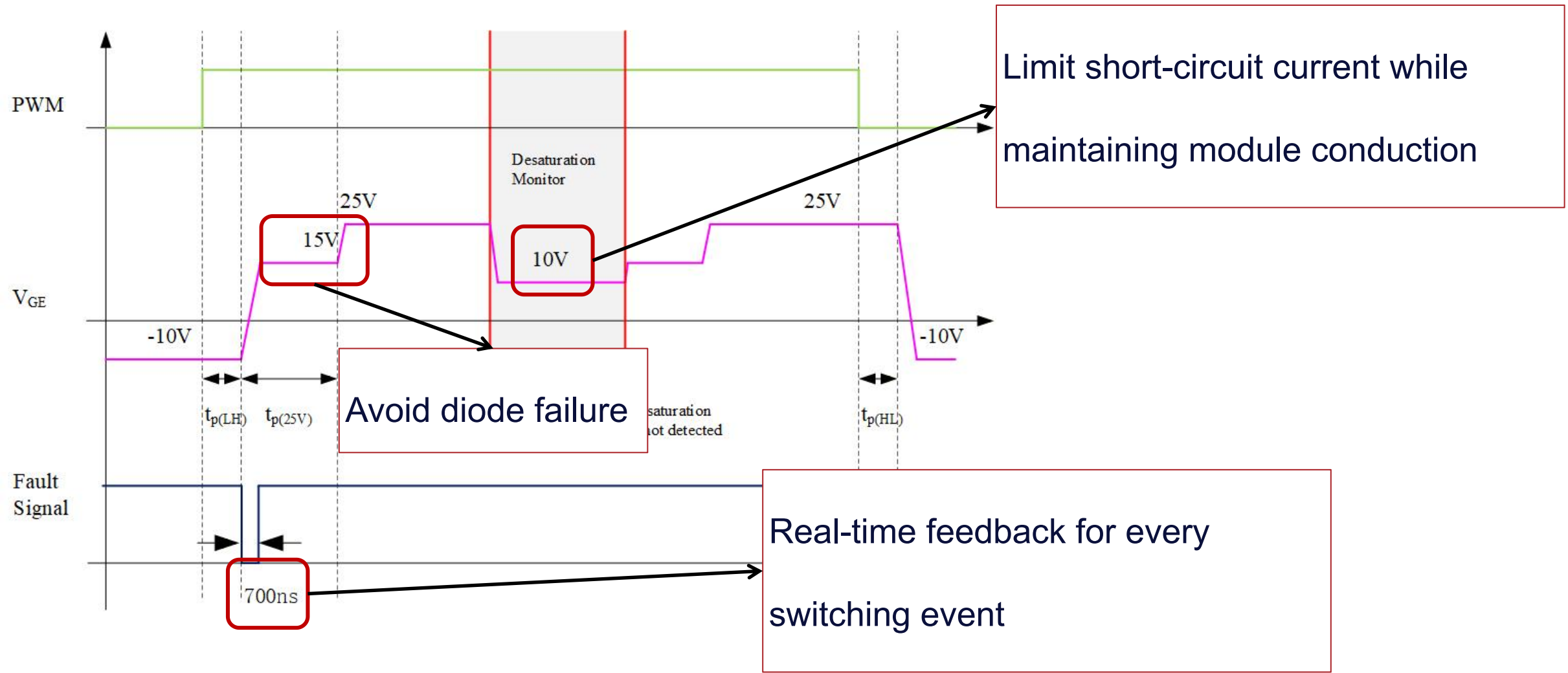
- di/dt detection responds first to the fast current rise
- V_{CE} detection then confirms the SC event



a) Desaturation is not detected with status output

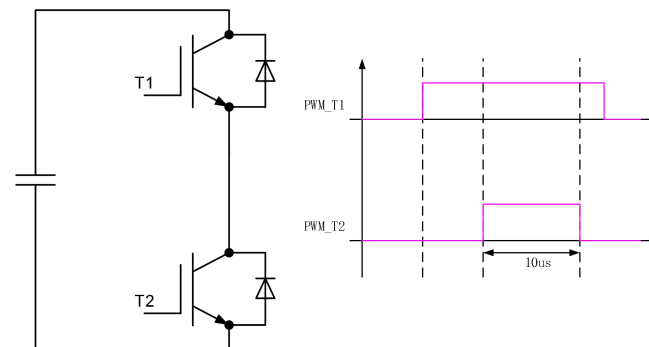
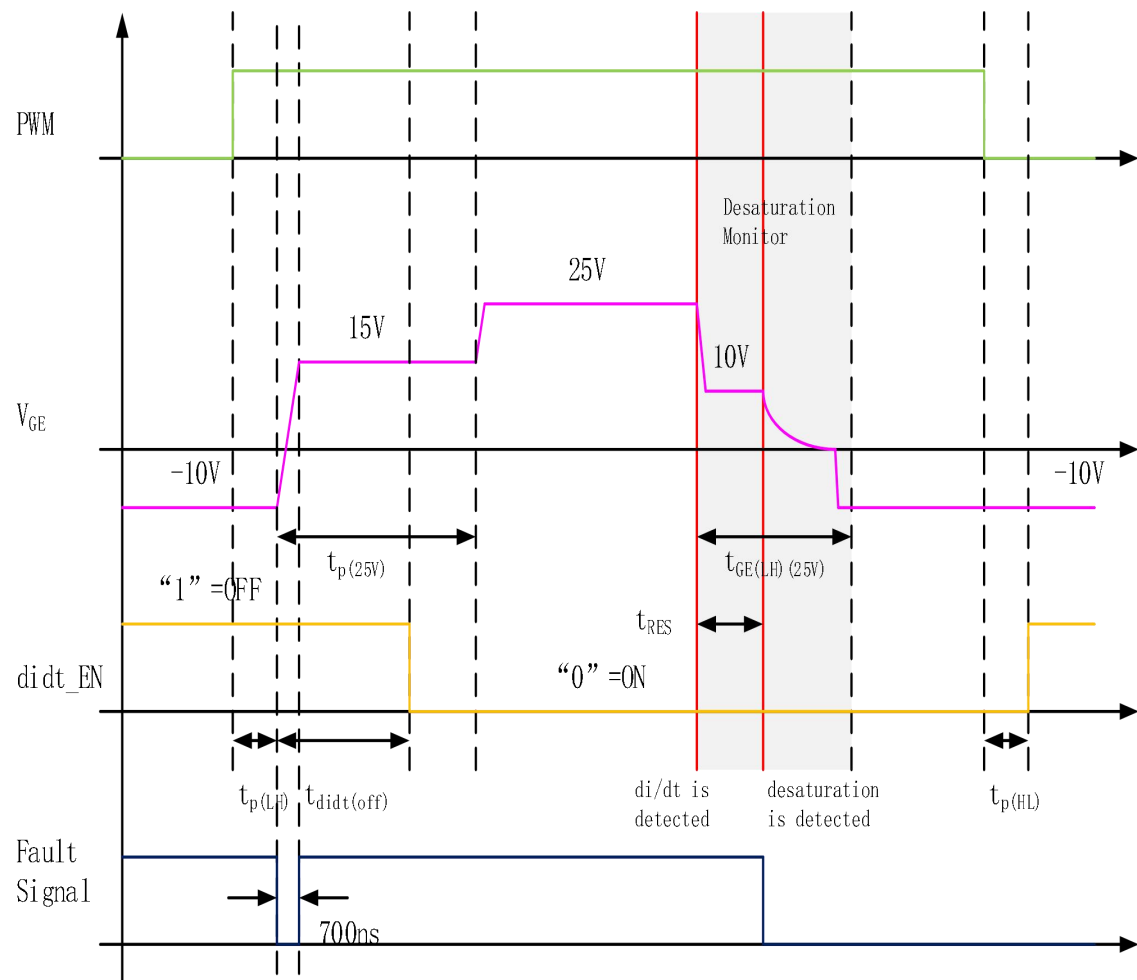


b) Desaturation is detected with status output

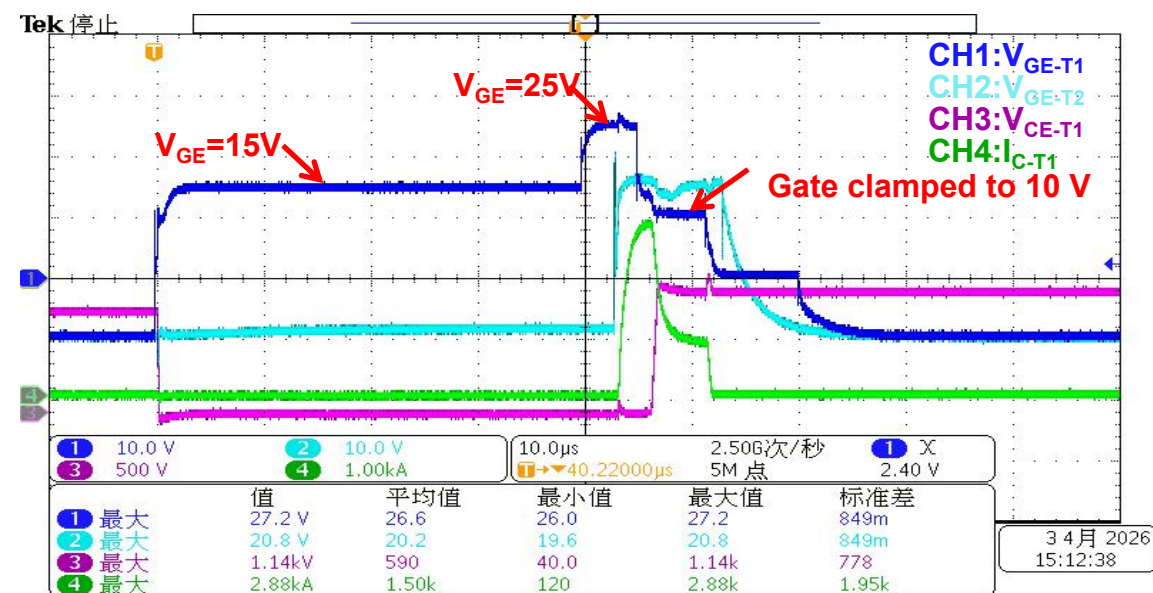




Protection for SCI



Arm short circuit to simulate the Typel short-circuit



$V_{DC}=1000V$; IGBT:FF600R17ME4@25°C

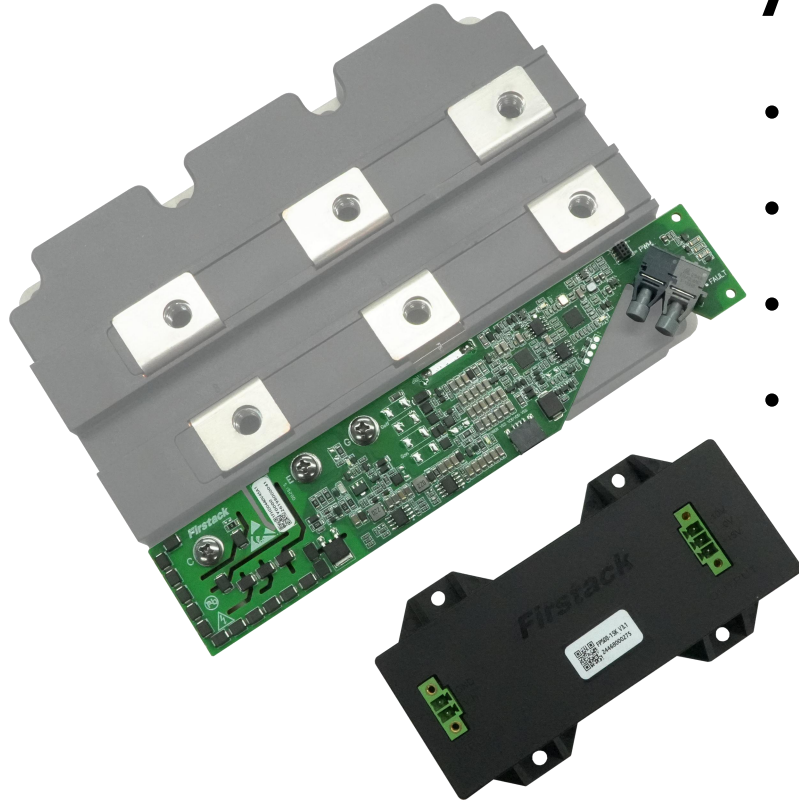


1FHD0440

FIRSTSTACK

ASIC + CPLD

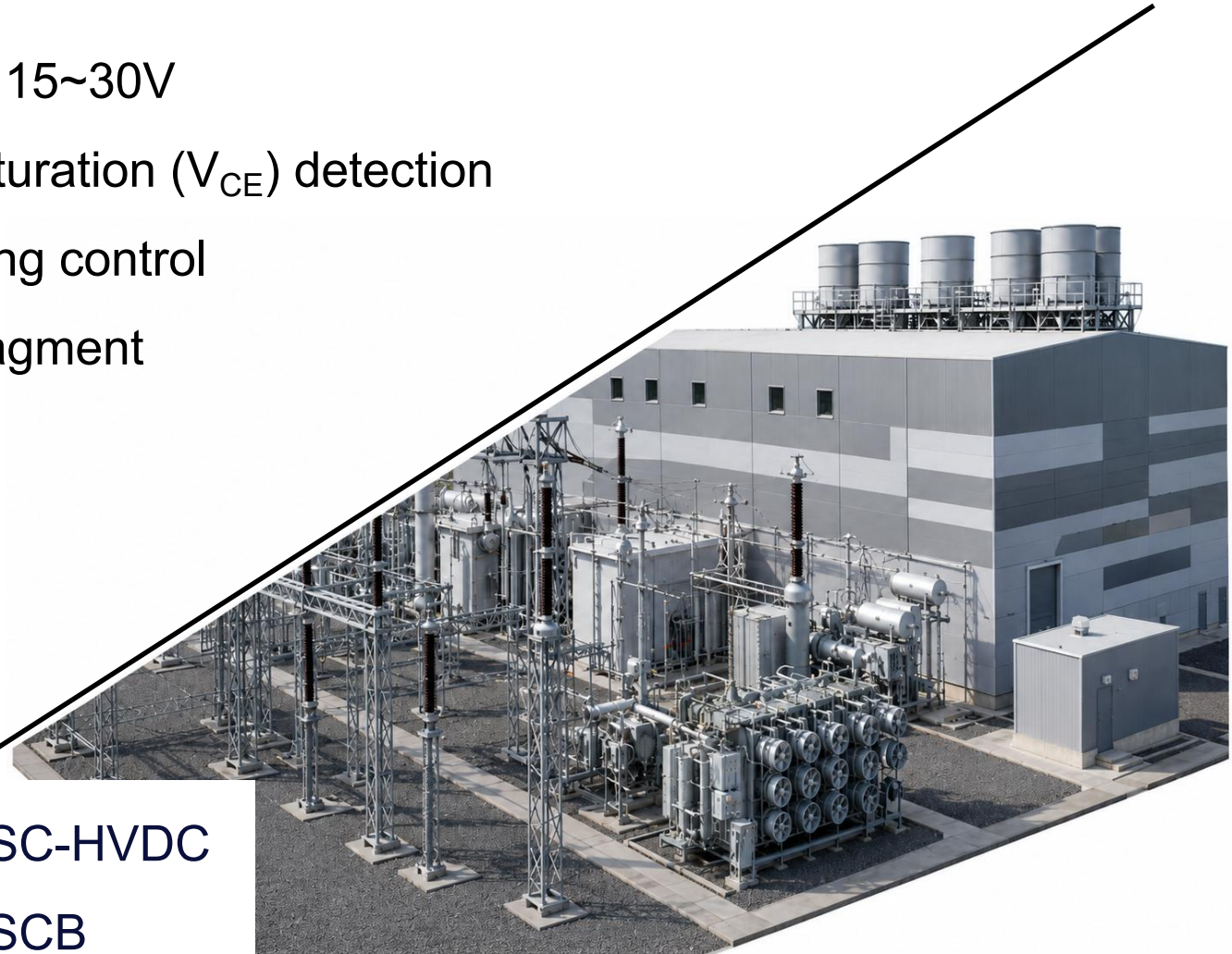
- Gate boost: 15~30V
- di/dt + desaturation (V_{CE}) detection
- Precies timing control
- Faults Managment



4500V IHM-B Module Series

Ø VSC-HVDC

Ø SSCB

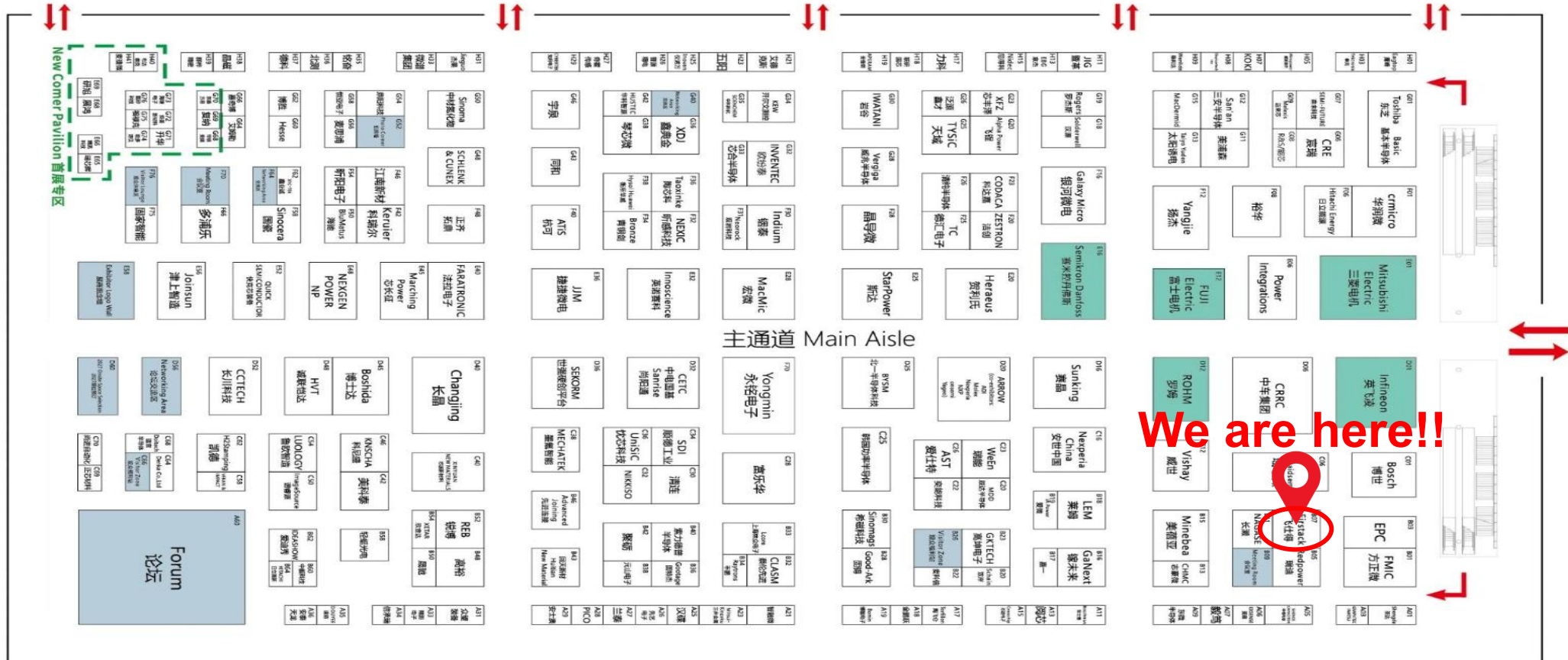




How to find us

FIRSTSTACK

H16-B07



www.firststack.com



www.linkedin.com/company/firststack-technology-co-ltd



www.youtube.com/@FirststackTech

Thanks !

