



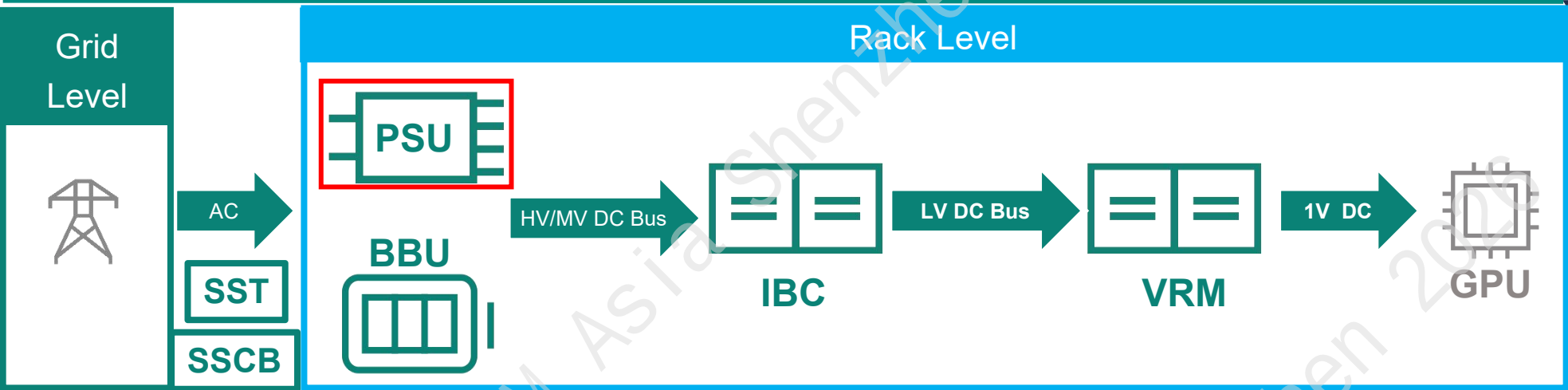
We power AI from Grid to Core

PCIM 2026, Shenzhen

Aug-27, 2026



AI Datacenter Power System

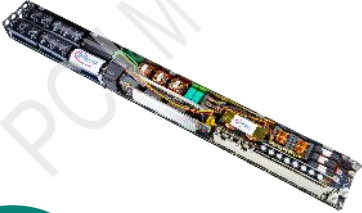
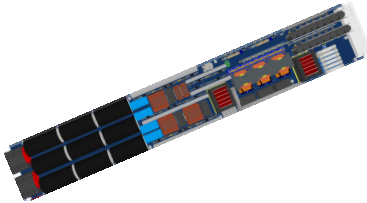
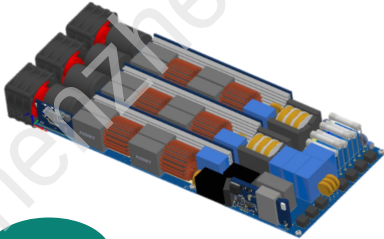
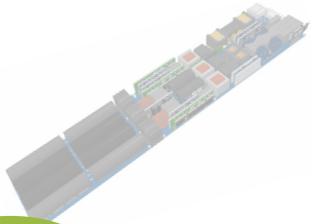


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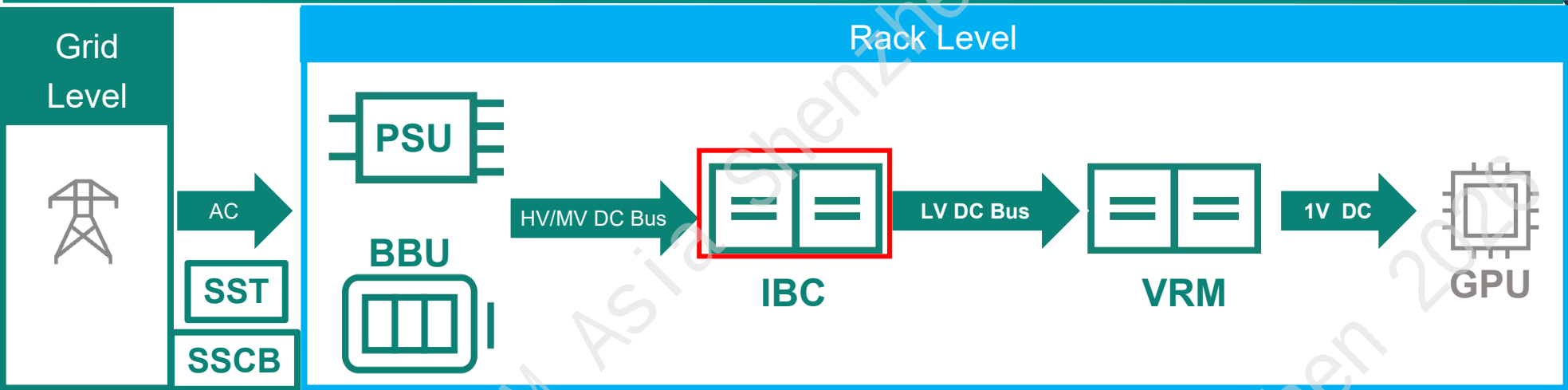


Server Rack PSU moves to higher&higher power driving by AI

Portfolio and roadmap – reference & evaluation boards

1-phase PSU, 50Vdc		3-phase PSU, 50Vdc / 400 to 800Vdc		
Ref. Board*	Ref. Board*	Ref. Board*	Eval. Board*	Ref. Board*
1-Φ PSU 8 kW, 50 Vdc 73.5 x 450 x 40 mm η ~97,5% peak Hold-up: 20ms @ 100% load 100 W/in³	1-Φ PSU 12 kW, 50 Vdc 68 x 640 x 40 mm η ~97,5% peak Hold-up: 20ms @ 100% load 113 W/in³	3-Φ PSU 18 kW, 50 Vdc 104 x 710 x 40 mm η ~97,5% peak Hold-up: 20ms @ 100% load 100 W/in³	3-Φ PFC 30 kW, 890 Vdc 133 x 330 x 40 mm η > 99% peak (PFC only)	3-Φ PSU 27+ kW, 400V 133 x 715 x 40 mm η >98% peak Hold-up: 20ms @ 100% load 110+ W/in³
REF_8KW_HFHD_PSU	REF_12KW_HFHD_PSU	REF_18KW_HFHD_3P_PSU	EVAL_30KW_TTYPE_PFC	REF_27KW_HFHD_3P_PSU
8 kW	12 kW	18 kW	30 kW	27+ kW
				
Available	Available	Available	Available	Upcoming
Interleaved Totem-Pole PFC, Full-bridge GaN LLC	3-Level FC Totem-Pole PFC, Full-bridge GaN LLC & SR	5-level ANPC 3-Φ PFC, 3L SiC LLC, GaN SR	Interleaved T-Type Vienna 3-Φ PFC topology & MCU demonstrator	5-level ANPC 3-Φ PFC, 3L LLC & SR
Si SiC HV GaN XMC	Si SiC HV GaN MV GaN XMC	Si SiC MV GaN XMC PSOC C3P8	SiC HV BDS PSOC C3P8	Si SiC PSOC C3P8
Q4/24	Q3/25	Q2/26	Q2/26	Q3/26

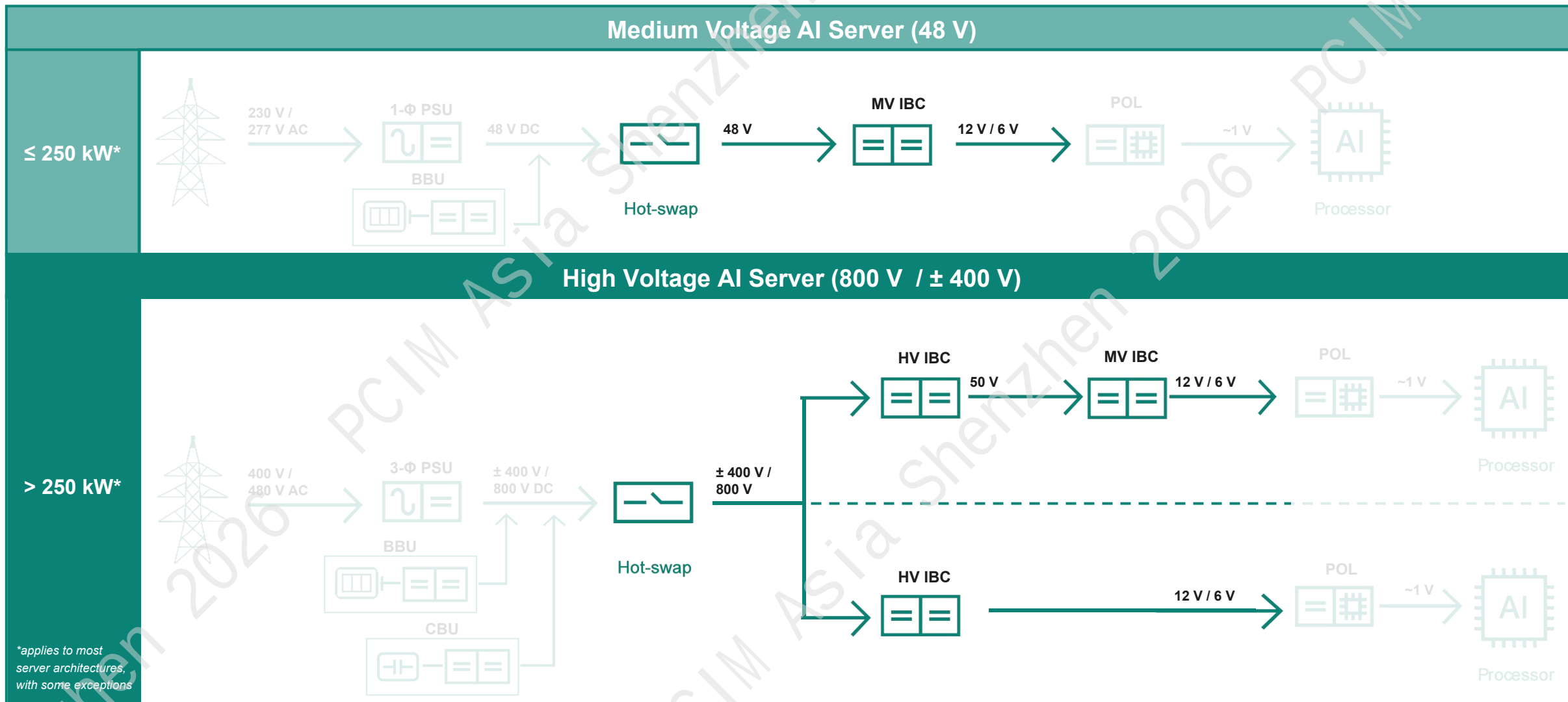
AI Datacenter Power System



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MV and HV IBC in AI Data Center Power System

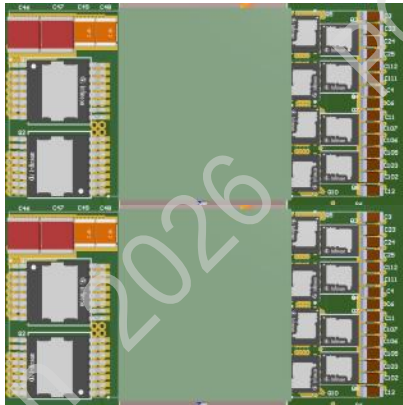


Leading GPU/CSP players currently investigate all paths from 800V DC to core

800V to 50V/12V/6V

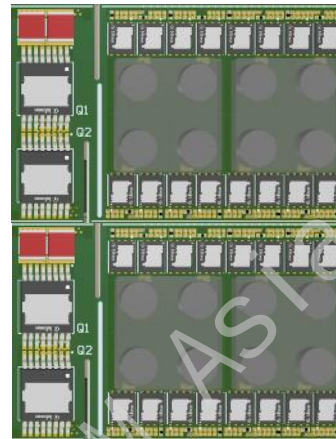
6kW 800V→50V

- ISOP **Half-bridge** LLC topology
- 60mm x 60mm x **11mm**



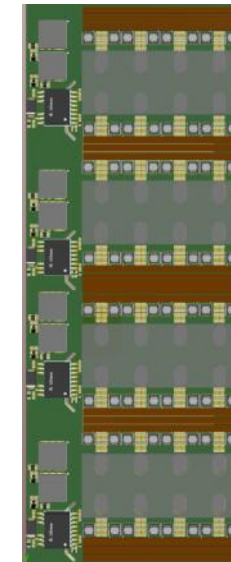
6kW 800V→12V

- ISOP **Half-bridge** LLC topology
- 62mm x 80mm x **8mm**



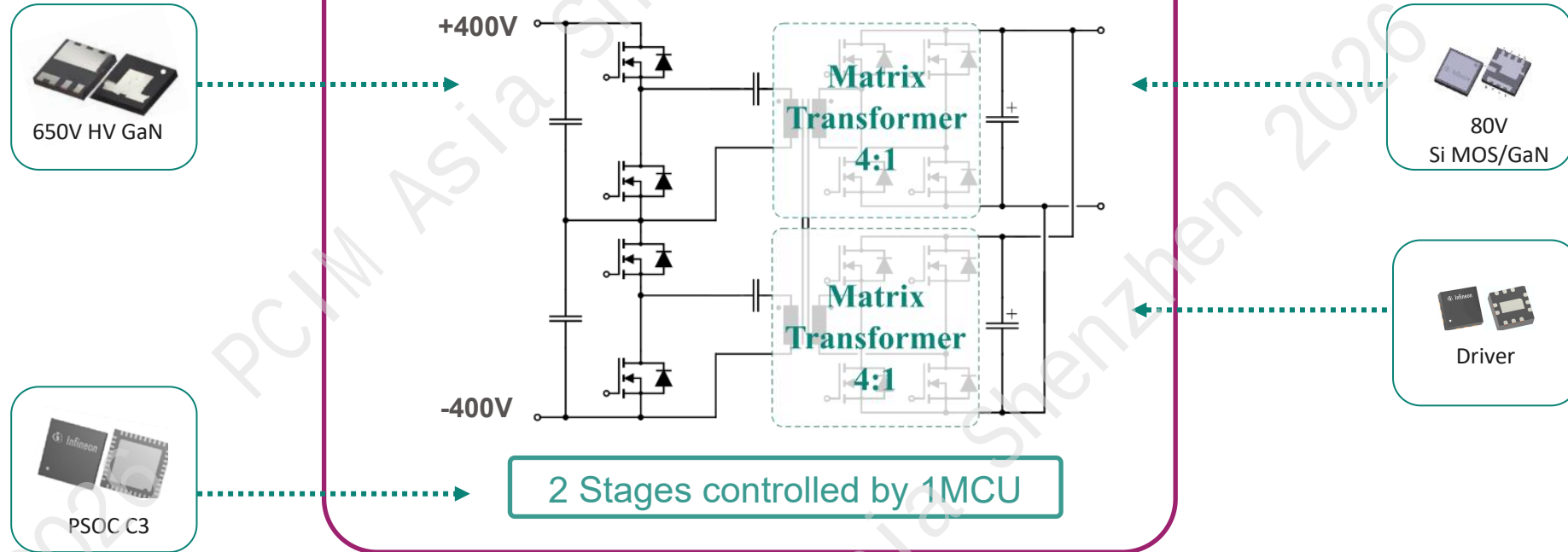
10kW 800V→6V

- ISOP **Full-bridge** LLC topology
- 165mm x 62mm x **6.5mm**



ISOP topology shows excellent efficiency and power density in HV IBC module

GaN is preferred. SiC can also be candidate as a trade-off of density and maturity.

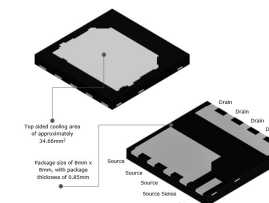


GaN vs SiC vs Si in Primary Side

- Switching frequency is at MHz level thus switching loss is critical to achieve target efficiency by achieving expected power density.
 - GaN offers the best switching performance with super lower dynamic parameters.
 - SiC can be alternative candidates in some design
 - Si MOSFET is no longer a good option in main stream HV IBC design

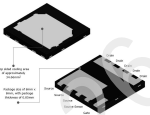
Partnumber	Cooling	Package	$R_{\text{dson,typ}} @ 25^{\circ}\text{C}$	The lower, the better		
				$Q_g @ 400\text{V}$	$Q_{\text{oss}} @ 400\text{V}$	$C_{\text{iss}} @ 400\text{V}$
Si IPLT60R024CM8	Top side	TOLT 10x15x2.3 mm ³	24mΩ	122nC		5382pF
SiC IMLT65R020M2H	Top side	TOLT 10x15x2.3 mm ³	20mΩ	57nC	108nC	2038pF
SiC IMLT65R033M2H	Top Side	TOLT 10x15x2.3 mm ³	33mΩ	34nC	65nC	1213pF
GaN IGLT65R025D2	Top side	TOLT 10x15x2.3 mm ³	25mΩ	11nC	82nC	780pF
GaN IGLC65R020D2	Top side	VHSON 8x8x0.95 mm ³	20mΩ	11nC	82nC	780pF

Top side cooling or dual side cooling is preferred for better thermal dissipation as all switch will be on top side



CoolGaN™ discrete for IBC

DSC 8*8 is preferred, and TOLT is also recommended

CoolGaN™ Transistor G5										
R _{DS(on, typ)} [mΩ]	650 V							700 V		
	ThinPAK 5x6	DFN 8x8	DSO TSC	ThinPAK 8x8	TOLL	TOLT	DSC 8x8	DPAK	ThinPAK 5x6	
										
500								IGD70R500D2S		
270	IGLR65R270D2							IGD70R270D2S	IGLR70R270D2S	
200	IGLR65R200D2							IGD70R200D2S	IGLR70R200D2S	
140	IGLR65R140D2	IGLD65R140D2		IGL65R140D2	IGT65R140D2			IGD70R140D2S	IGLR70R140D2S	
110		IGLD65R110D2		IGL65R110D2		IGLT65R110D2	IGLC65R100D2			
80		IGLD65R080D2		IGL65R080D2			IGLC65R065D2			
55		IGLD65R055D2	IGOT65R055D2	IGL65R055D2	IGT65R055D2	IGLT65R055D2				
45			IGOT65R045D2		IGT65R045D2	IGLT65R045D2				
30/35			IGOT65R035D2		IGT65R035D2	IGLT65R035D2	IGLC65R030D2			
25			IGOT65R025D2		IGT65R025D2	IGLT65R025D2	IGLC65R020D2			
17										
ES timeline	Released							Available	Released	
QS timeline								Q3CY26		
SOP								Q4 CY26		

*timeline is subject to change

Released

Coming soon

MV GaN value proposition in 2nd side comparing with Si MOSFET

Technology	Partnumber	Cooling	Package [mm³]	Q_{oss} @ 40V [nC]	$Q_{gs,ZVS}$ [nC]	$R_{ds(on),max}$ @ 25°C [mΩ]	$R_{ds(on),max}$ @ 100°C [mΩ]
Si	ISC013N08NM8SC	Dual side (drain-down)	5x6x0.75	159	76	1.3	1.9
Si	ISC016N08NM8SC	Dual side (drain-down)	5x6x0.75	147	61	1.6	2.4
GaN	IGD0xxK08S2	Dual side (drain-down)	5x6x0.75	84	20	0.9	1.3

GaN dynamic parameter is better than Si thus supporting higher frequency design with high efficiency

GaN provides lower $R_{ds(on)}$ in the same package making it possible to reduce quantity in parallel

Each switch needs a driver

Primary Side: 2EDR7259X

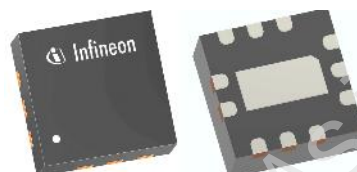
- 2-channel isolated gate driver for Si and SiC MOSFETs and GaN HEMTs power switches
- Fast input-to-output propagation (38 ns) with excellent stability (+9/-5 ns)
- Strong output stage: 5 A/9 A source/ sink
- Fast output clamping for $V_{DDA/B} < UVLO$
- Fast UVLO recovery time ($< 2 \mu s$)
- Four VDDA/B UVLO options: 4 V, 8 V, 12 V, 15 V
- CMTI $> 150 V/ns$
- Available in 16/14-pin 300 mil DSO package



DSO-14

2nd Side Driver for Si 2EDL6014

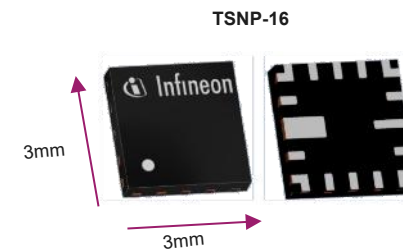
- Level-shifted dual channel floating output driver
- Wide gate driver supply voltage **4V to 16V** (VDDA/VDDB)
- 3.3 V and 5 V compliant INx and STA pins
- **4 A** source / **6 A** sink output current capability
- **120 V** absolute maximum voltage on VDDA and VDDB
- -5 A output pin reverse current capability
- **-20 V** absolute maximum negative voltage on GNDA/GNDB
- **20 ns** fast propagation delay and **1 ns** typical delay matching
- **10 ns** minimum pulse width
- Adjustable pull-up strength(1/8 pull-up strength) for **soft startup**
- **Self input supply** as option
- $R_{th-ic(bottom)}=4.1 K/W$



2.2 * 2.2 mm

2nd Side Driver for Si and GaN 2EDL90XG3

- **Level-shifted dual channel floating output driver**
- Wide VDD supply voltage range 4 V - 15 V
- 5V gate clamp for high efficiency GaN driving
- UVLO: 3.8 V rise and 3.6 V fall
- Configurable PWM input
 - Single PWM input supported tri-state, adjustable deadline
 - Hi/Li and Hi/ Li invert independent PWM input
 - HSCC HS/ LS modes
- 3.3 V compliant PWM input logic and endure 5 V max
- **2EDL900G3** 4 A / 6 A source and sink current for **Si MOS**
- **2EDL901G3** 1.6 A/ 6 A source and sink current for **GaN**
- 120 V absolute maximum voltage on HB and LB
- 15 ns typ prop delay
- 6ns – 100 ns adjustable deadline or turn-on delay (DTC)
- Inductor DCR/ shunt based current sensing and report (CS)
 - 5 MHz typ bandwidth
 - Common mode voltage up to 35 V

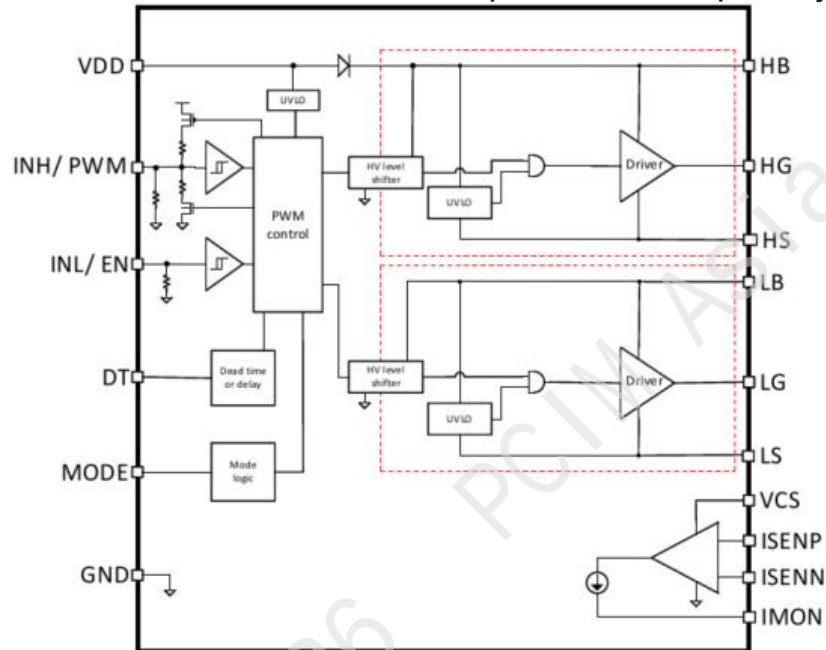


Emmy: 2EDL90xG3

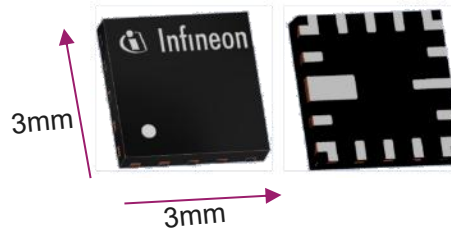
Common footprint driver for Si and GaN switches for easy multi-platform use

2EDL900G3 (Si Driver)

4 A / 6 A source/sink output current capability

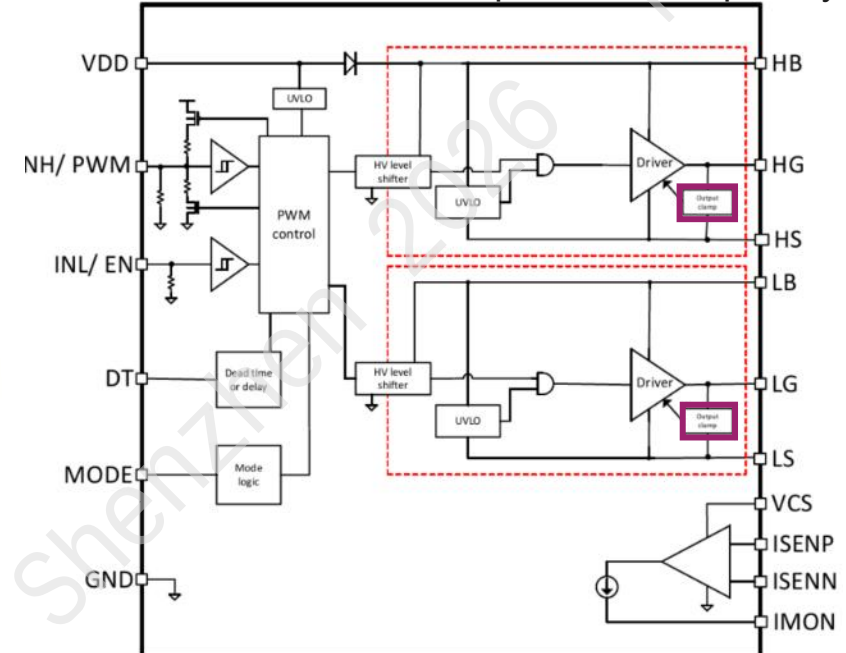


TSNP-16



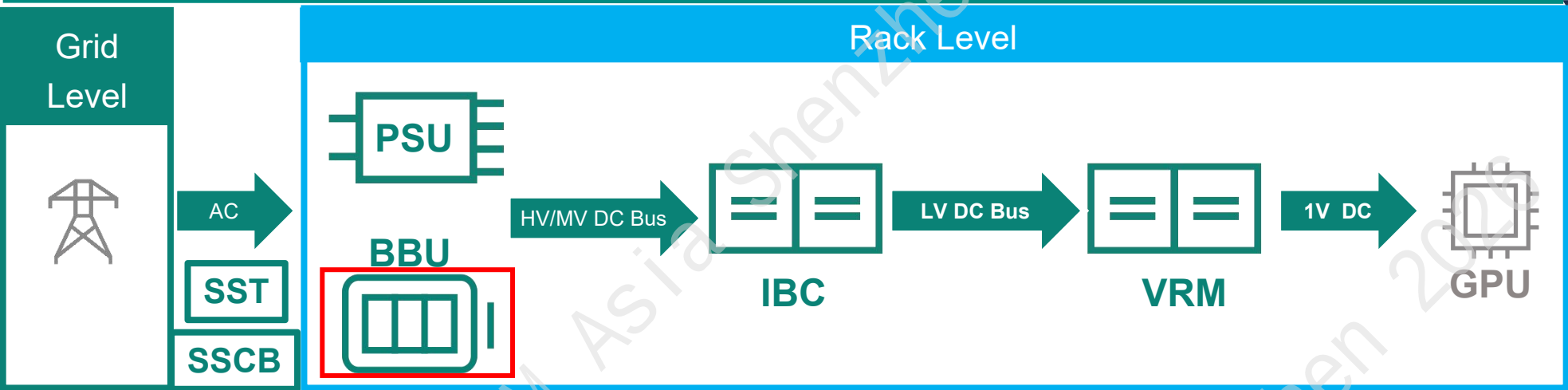
2EDL901G3 (GaN Driver)

1.6 A / 6 A source/sink output current capability



5V gate clamp
for high
efficiency GaN
driving

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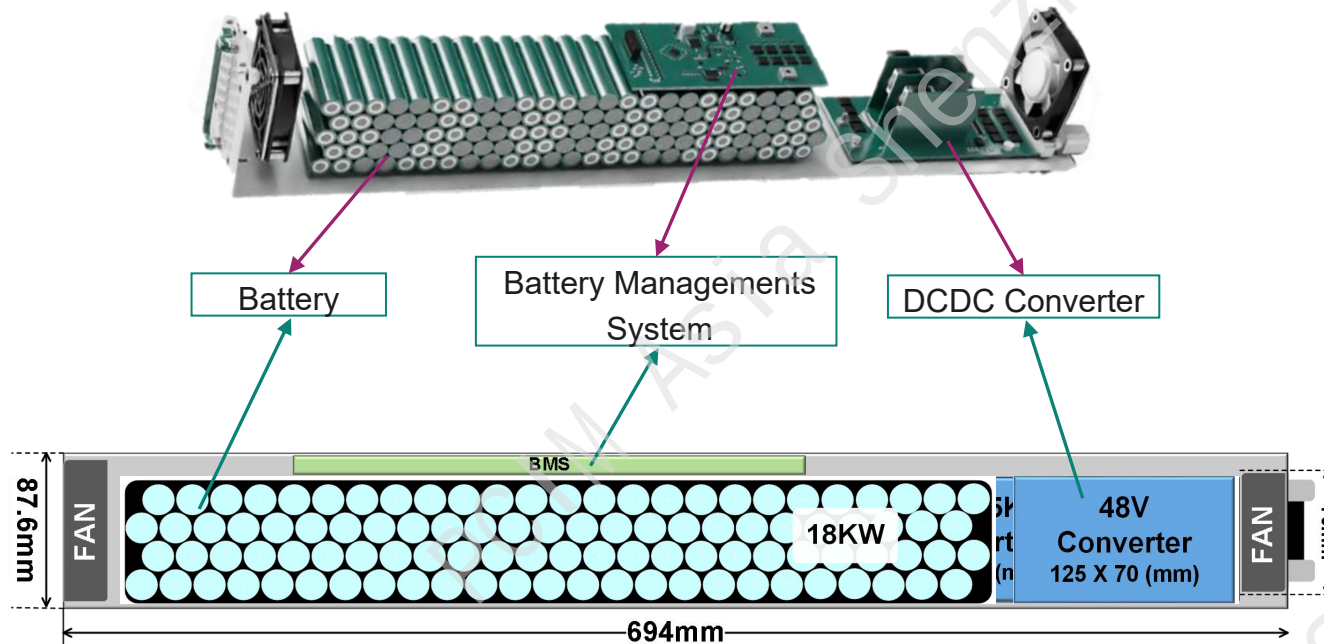


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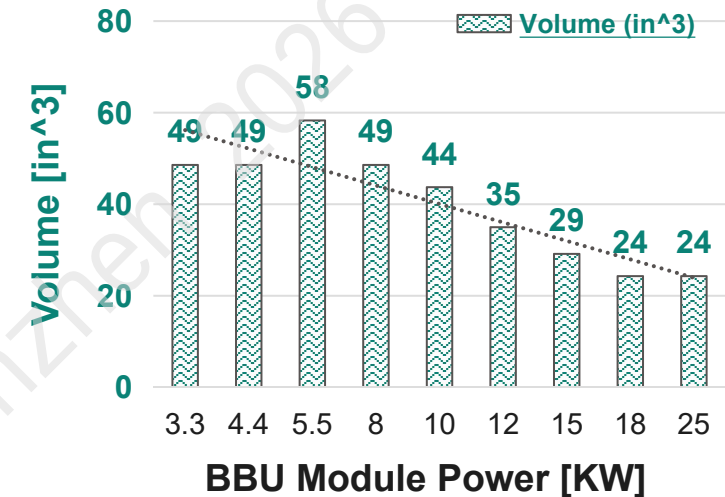


Increasing battery cells number decreases the available space for the power converter, requiring higher power density

BBU Overview



BBU Power v/s Volume available



Upgrades in BBUs,

Demands to Increase

- Battery Size → *to increase capacity [Ah]*
- Converter power density → *to fit the reduce volume for converter*
- Efficiency → *to extend backup time, reduce thermals & optimize Battery Size*

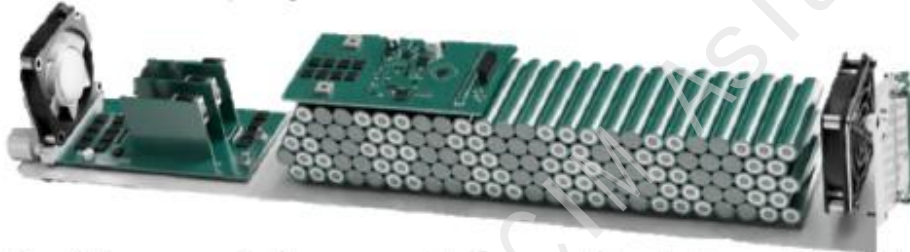
Infiniteon solutions for BBU applications, showing power density and integration

48 V BBU with Li-Ion cells

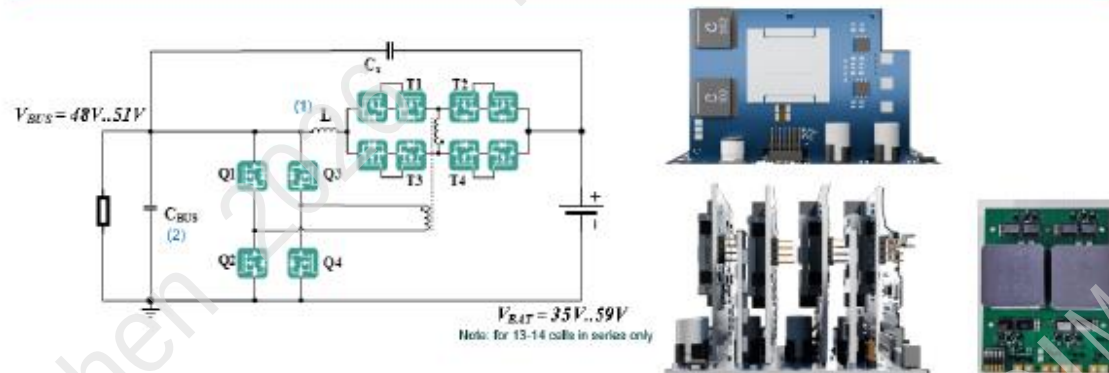
~3-24 kW BBU (48 V)

Driving **efficiency and power density** supported by the following trends:

- High efficiency (>99%) and x4 power density
- Scalability
- Usage of **GaN** for >12 kW Buck Boost or alternative DCDC bidirectional topologies



Partial power Infineon solution or Buck Boost GaN based



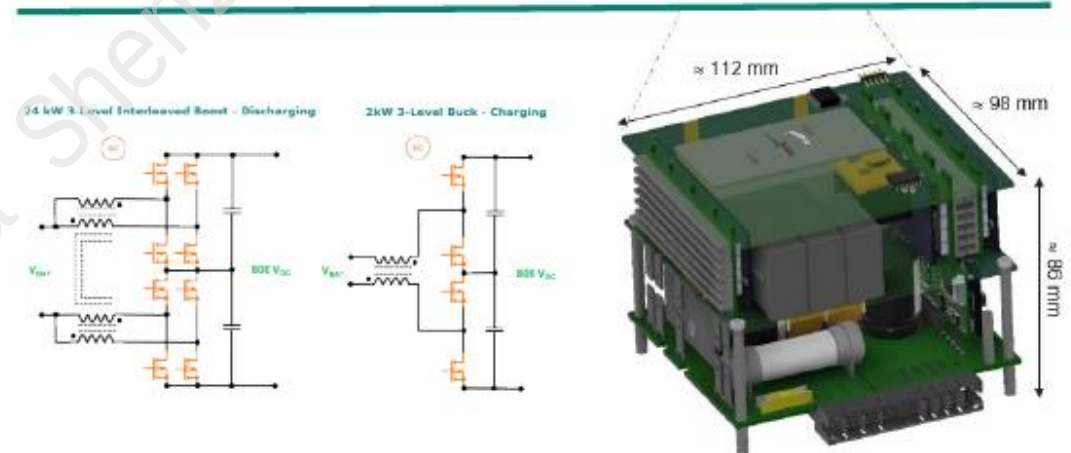
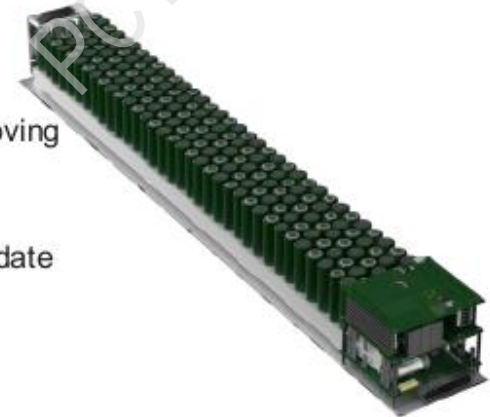
HV BBU with Li-ion cells

24-30 kW BBU (400 V and 800 V)

Driving **efficiency and power density** supported by the following trends:

- High efficiency and power density improving thermals
- Scalability (also with cards concept)
- Wide input voltage ranges to accommodate various chemistries
- WBG devices for optimal switching performance
- Advanced magnetic materials

HV BBU Infineon solution (Multilevel Boost converter) based on 650V SiC



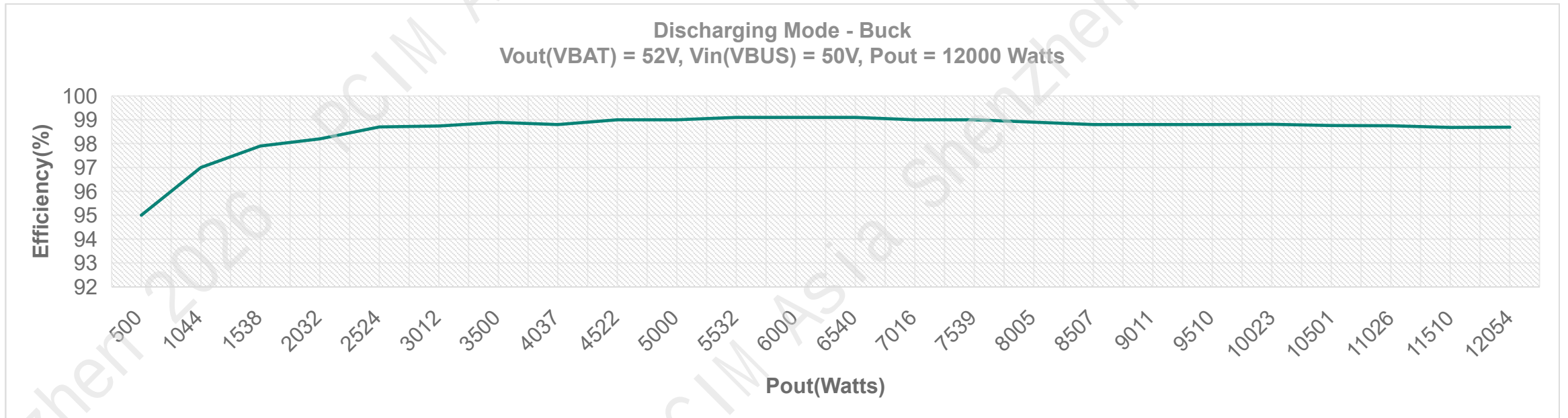
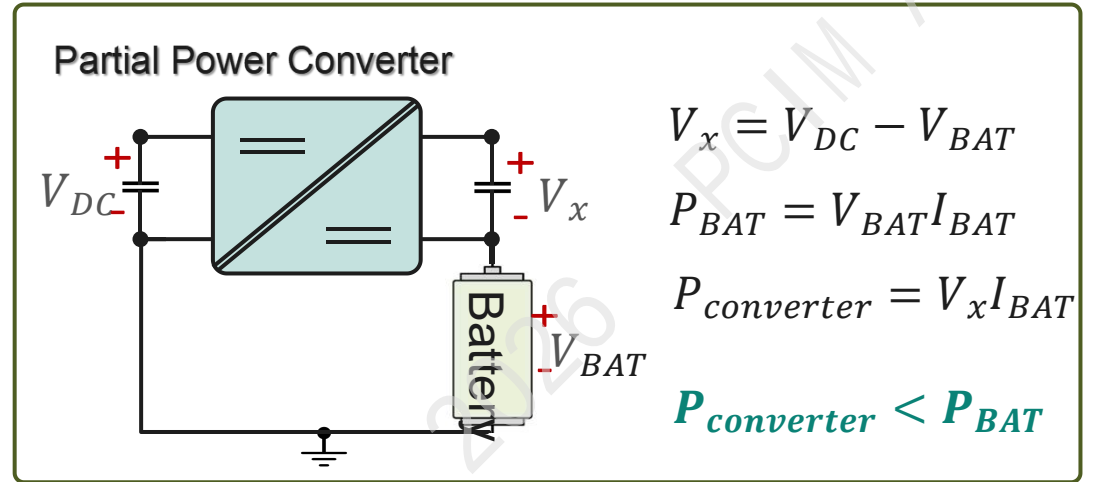
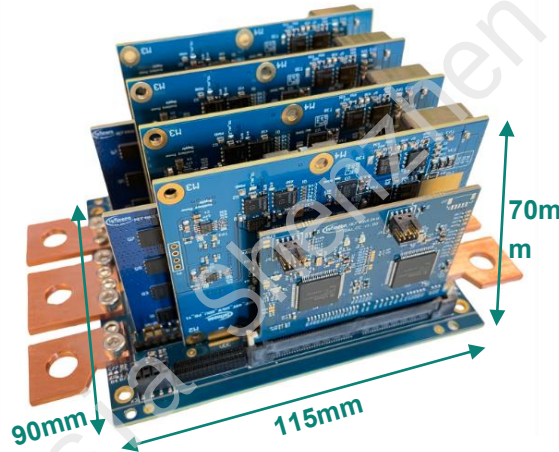
12kW/50V BBU Evaluation Board

Available



12 KW Board consists of

- 4x Power board(PB) – (3 KW Rated Power)
- 1x Controller card – 2x PSoC-C3 MCU's
- 2x Protection/ORING card
- 1x Main Board

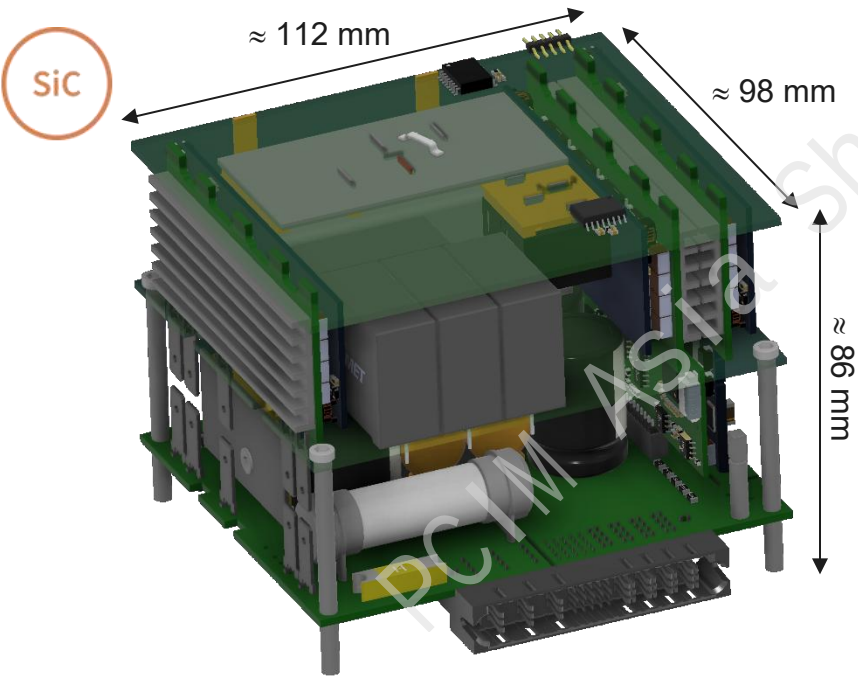


24 kW / 800 V_{DC} Battery Back Unit system demo board

Available end of
2026



24 kW BBU 800V



Technical details	
Target Application	HV Battery Backup Unit
Battery pack voltage range	[2.5V – 4V] x 168 cells → [420V – 672V]
Bus voltage range	[795V – 825V]
Output power discharge to bus	24 kW nominal during 120 s
Efficiency in discharge to bus	≈ 98.5 %
Output power charge to battery	2.4 kW nominal CC-CV curves
Efficiency in charge to battery	≈ 98.5 %
Ambient temperature	-5°C to 45°C

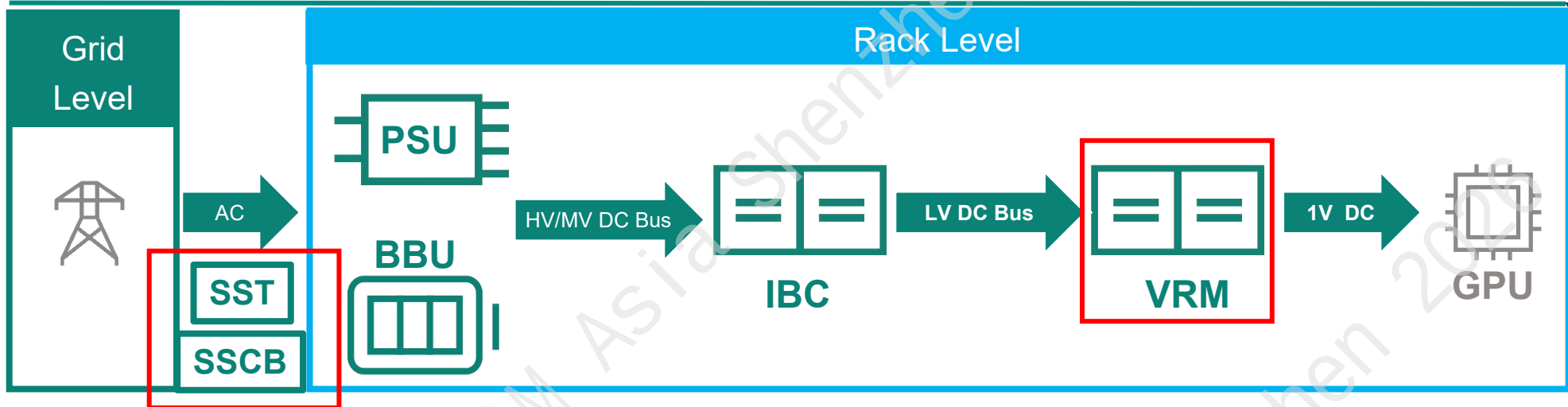
Learn More				
Infineon components	SiC	650V	3-Level cell boost	IMT65R033M2H
	SiC	650V	3-Level cell buck	IMT65R060M2H
	SiC	1200V	Oring / Hotswap	IJC120RM5XD1
Controller	PSOC C3 M8/P8			

Features

- › Input battery side: 420-705V_{DC} ; Output bus side: 795-825V_{DC} (800V_{DC} nominal)
- › Highest efficiency & power density with CoolSiC™
- › Multi-phase multi-level boost interleaved
- › Integrated/coupled magnetics
- › High efficiency to meet thermal requirements
- › Full digital control

- › Power density ≈ 450W/in³
- › Full-power discharge 24 kW during 120 s
- › Efficiency ~ 98.5% discharge and charge

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