

Research on Current Sharing and Optimization of Three-Chip Parallel IGBT Modules During Switching Process

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Abstract

This paper investigates the current sharing issues of the three-chip parallel IGBT (Insulated-gate bipolar transistor) modules during the switching process. The effects of chip electrical parameters and module parasitic inductances on current sharing during the switching process are studied through simulation, and the differences in power loss and temperature rise caused by uneven current sharing are analyzed. In addition, methods for optimizing current sharing through module package design and chip parameter selection are presented.

Simplified Circuit Mode

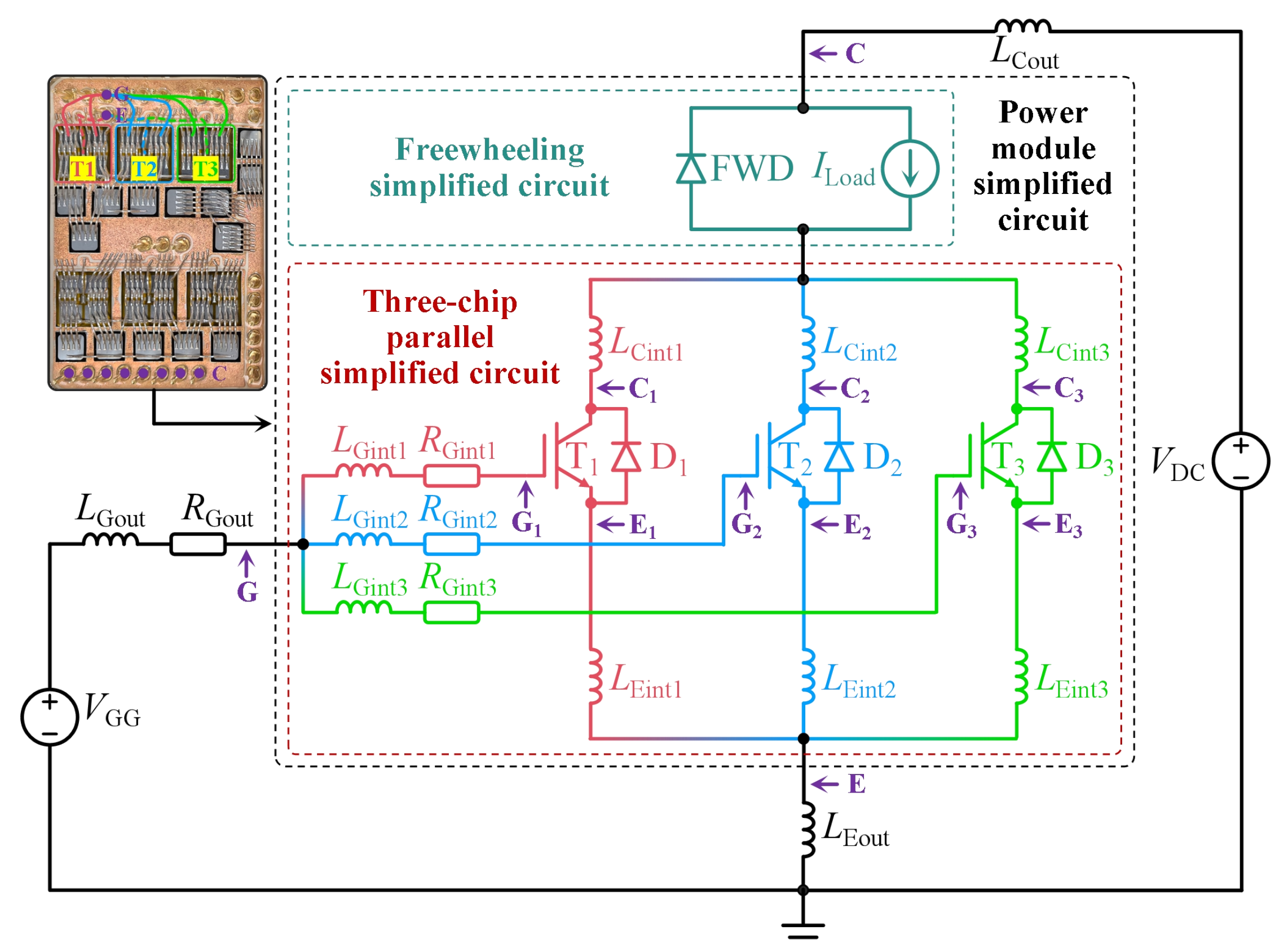


Figure 1. Three-chip parallel IGBT power module.

Effects of L_{Eint} and V_{th} on the Current Sharing

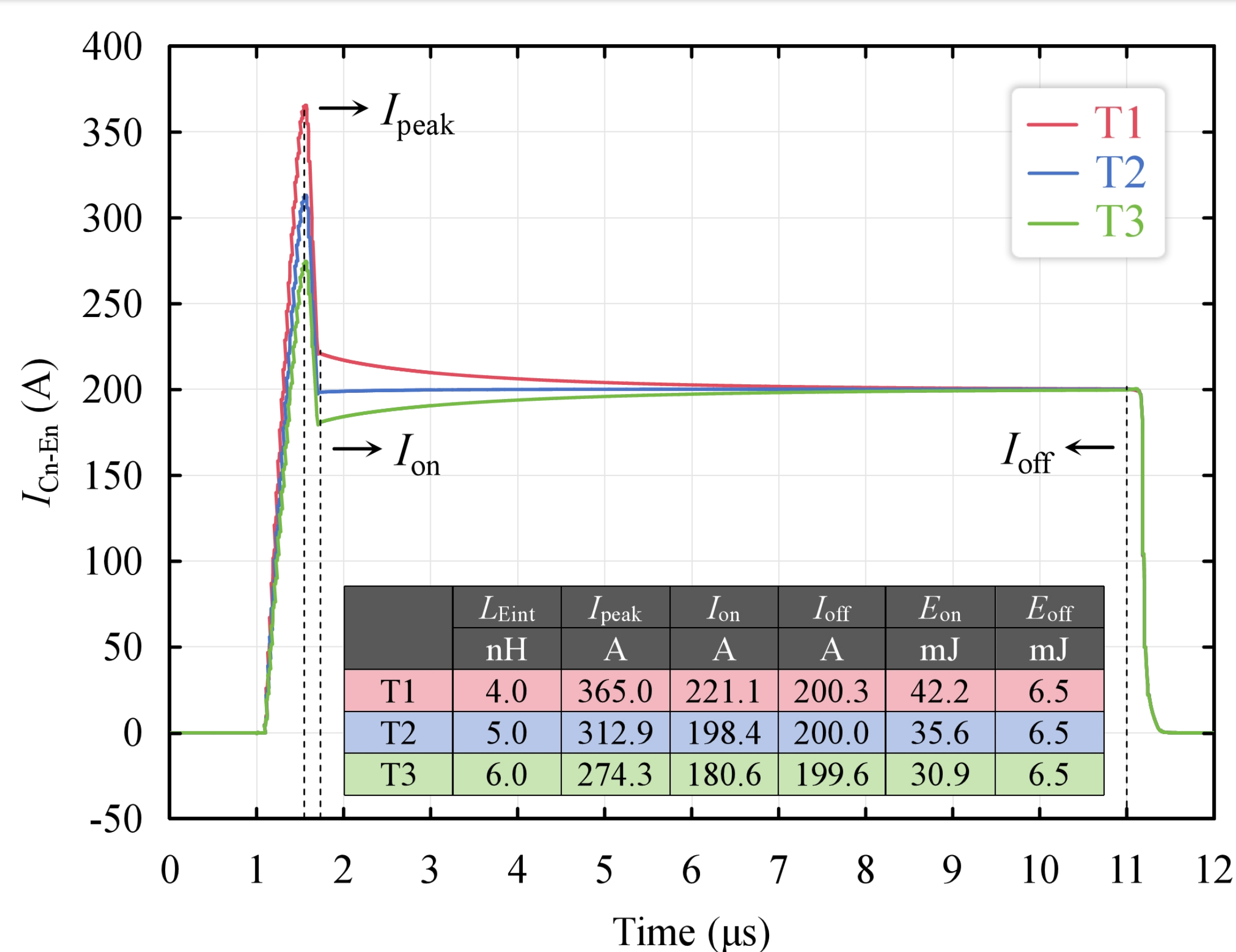


Figure 2. Effects of L_{Eint} on the current sharing.

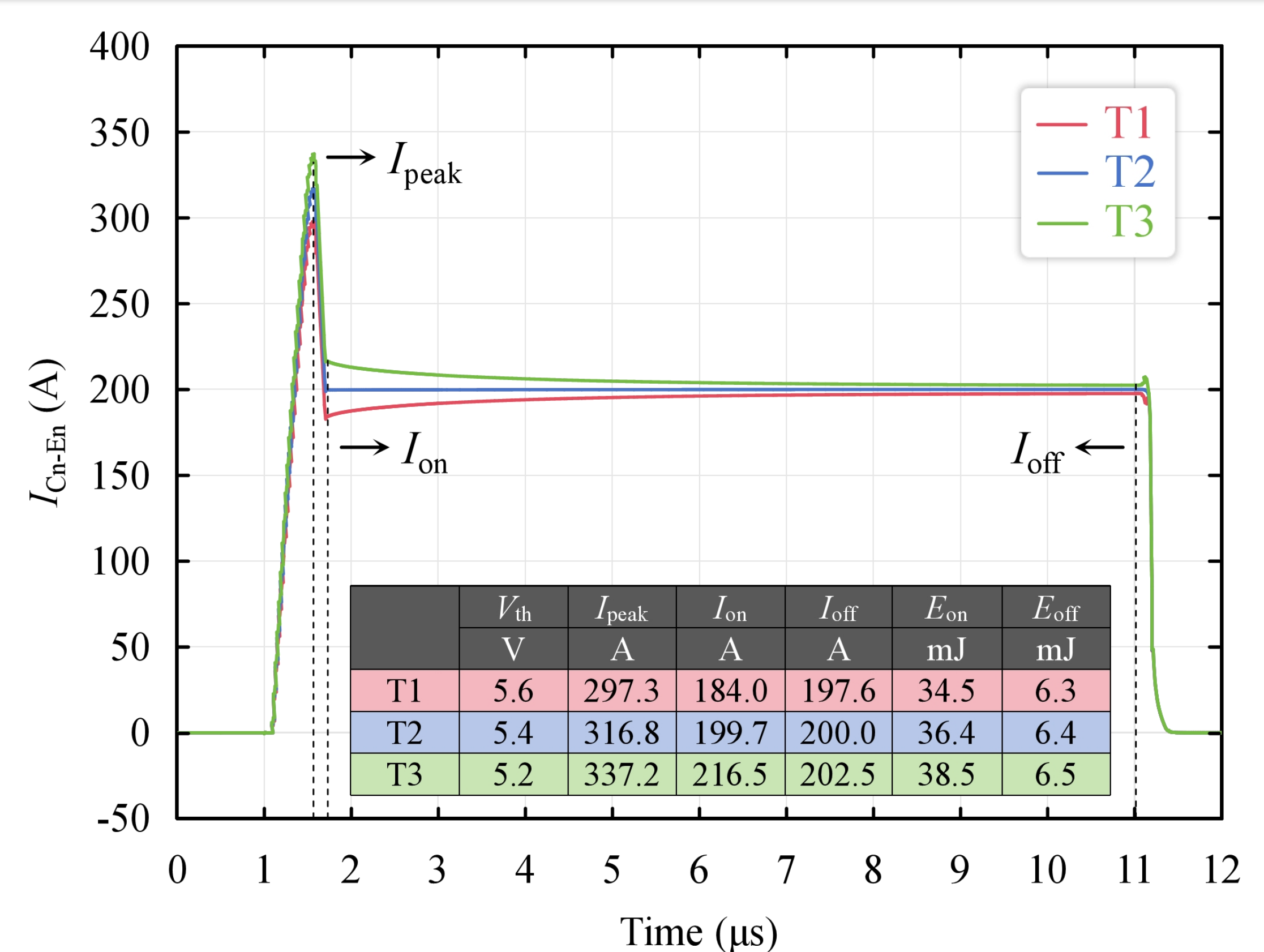


Figure 3. Effects of V_{th} on the current sharing.

Effects of L_{Eint} and V_{th} on P_{sw} , P_{con} and ΔT_{vj} (Under 250 kW Operating Conditions)

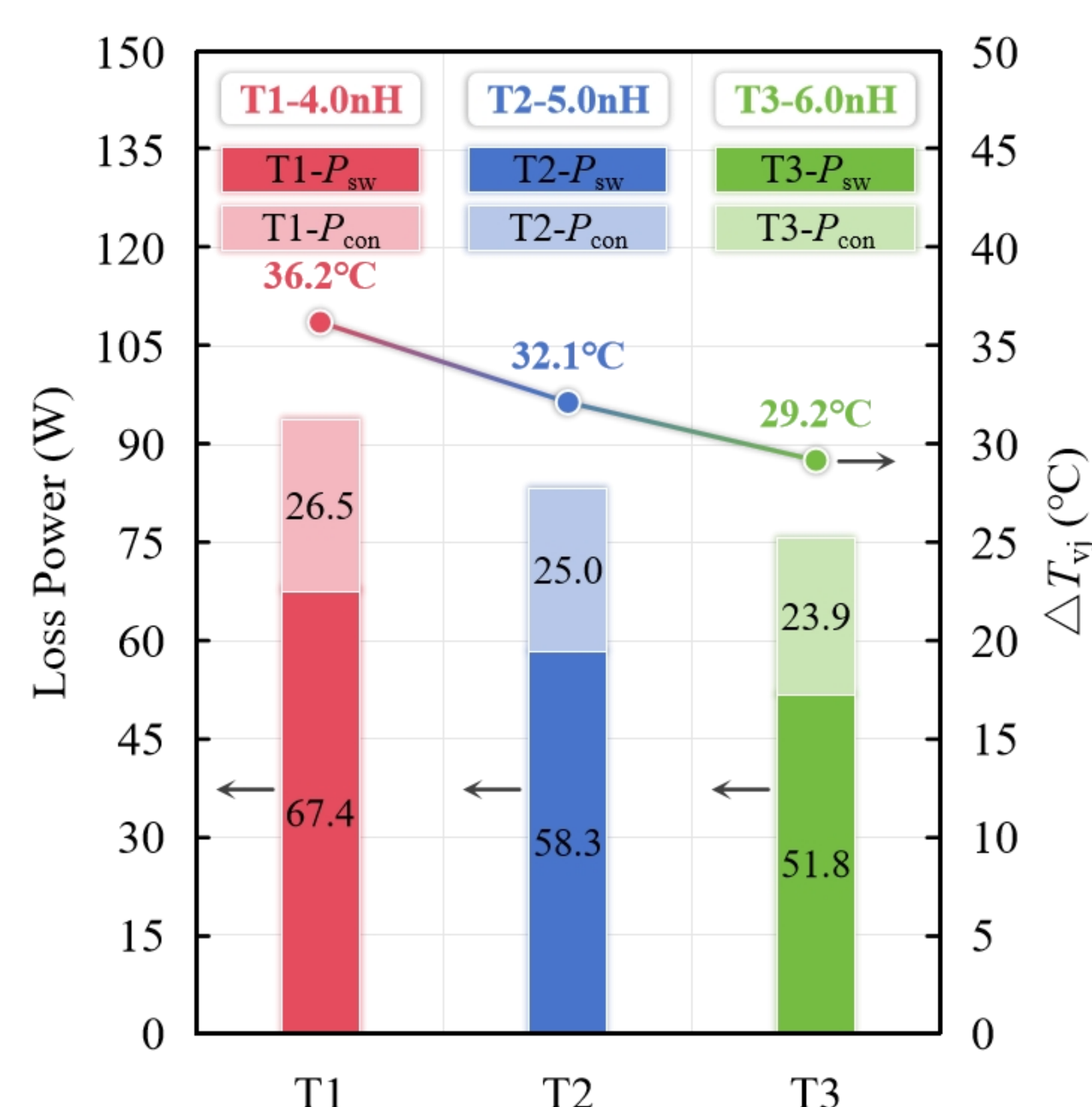


Figure 4. Effects of L_{Eint} on P_{sw} , P_{con} and ΔT_{vj} .

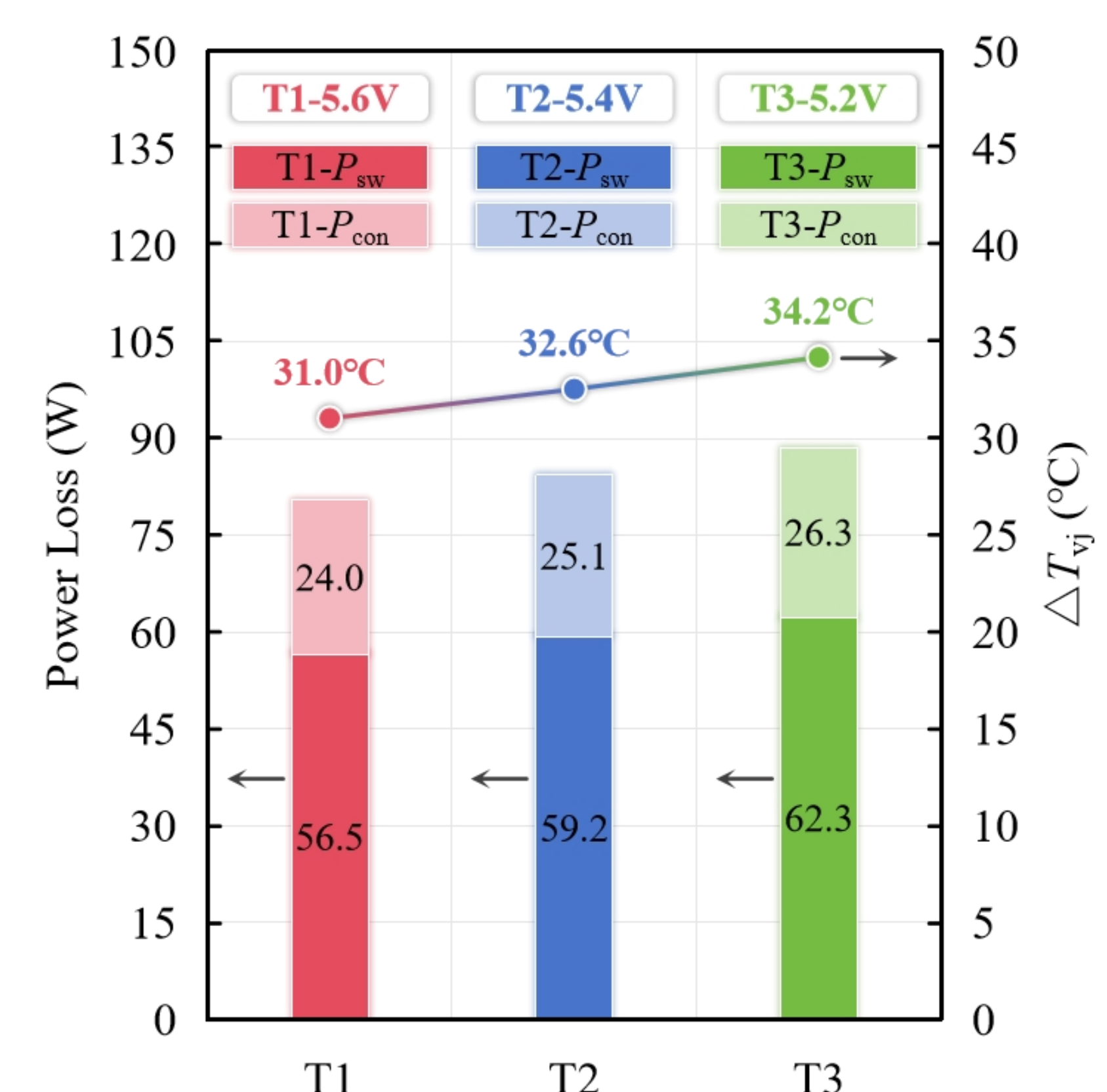


Figure 5. Effects of V_{th} on P_{sw} , P_{con} and ΔT_{vj} .

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Effects of ΔL_{Eint} on E_{on} and E_{off}

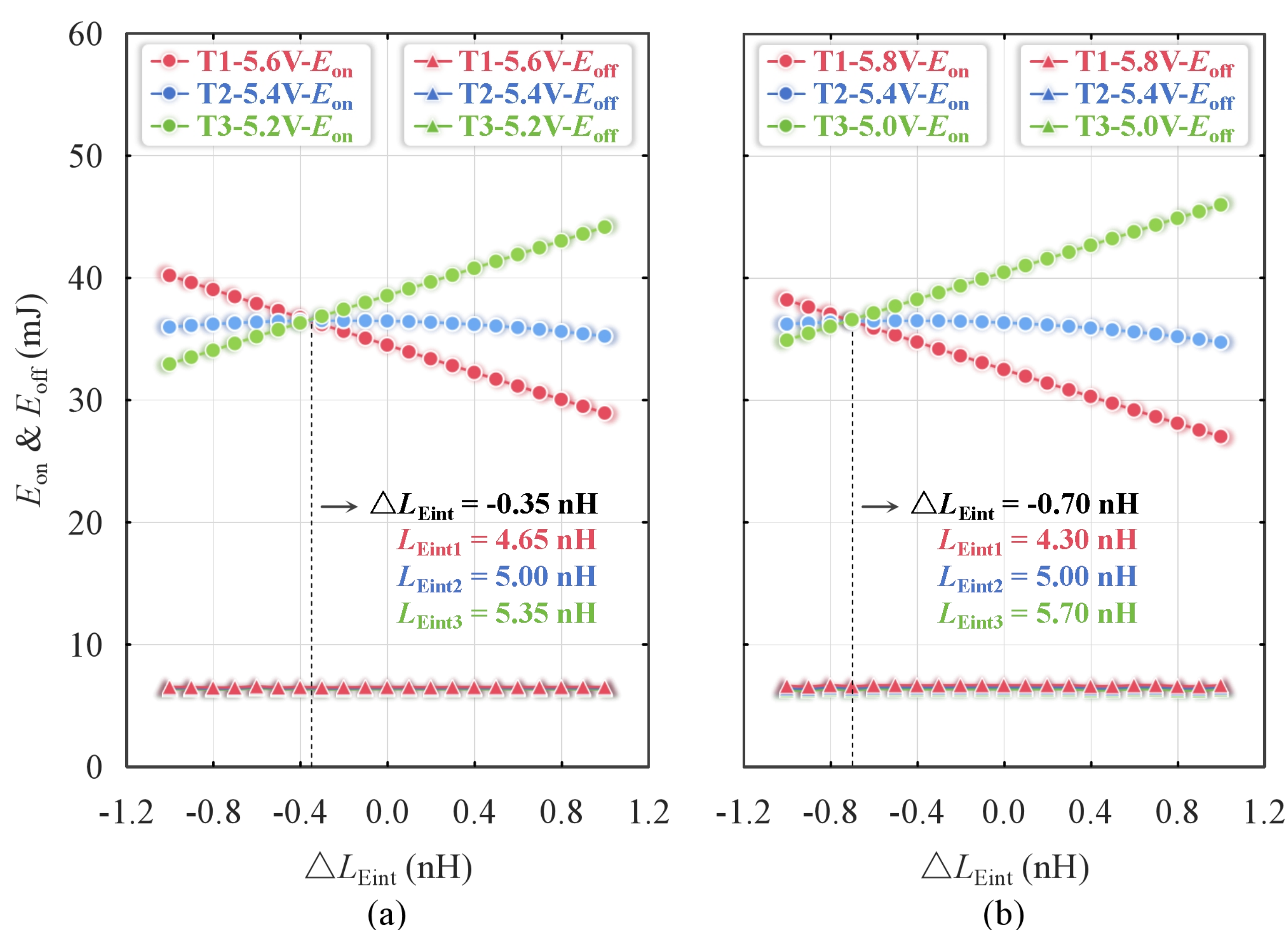


Figure 6. Effects of ΔL_{Eint} on E_{on} and E_{off} at (a). $\Delta V_{th} = 0.2$ V and (b). $\Delta V_{th} = 0.4$ V.

Effects of ΔL_{Eint} on the current sharing

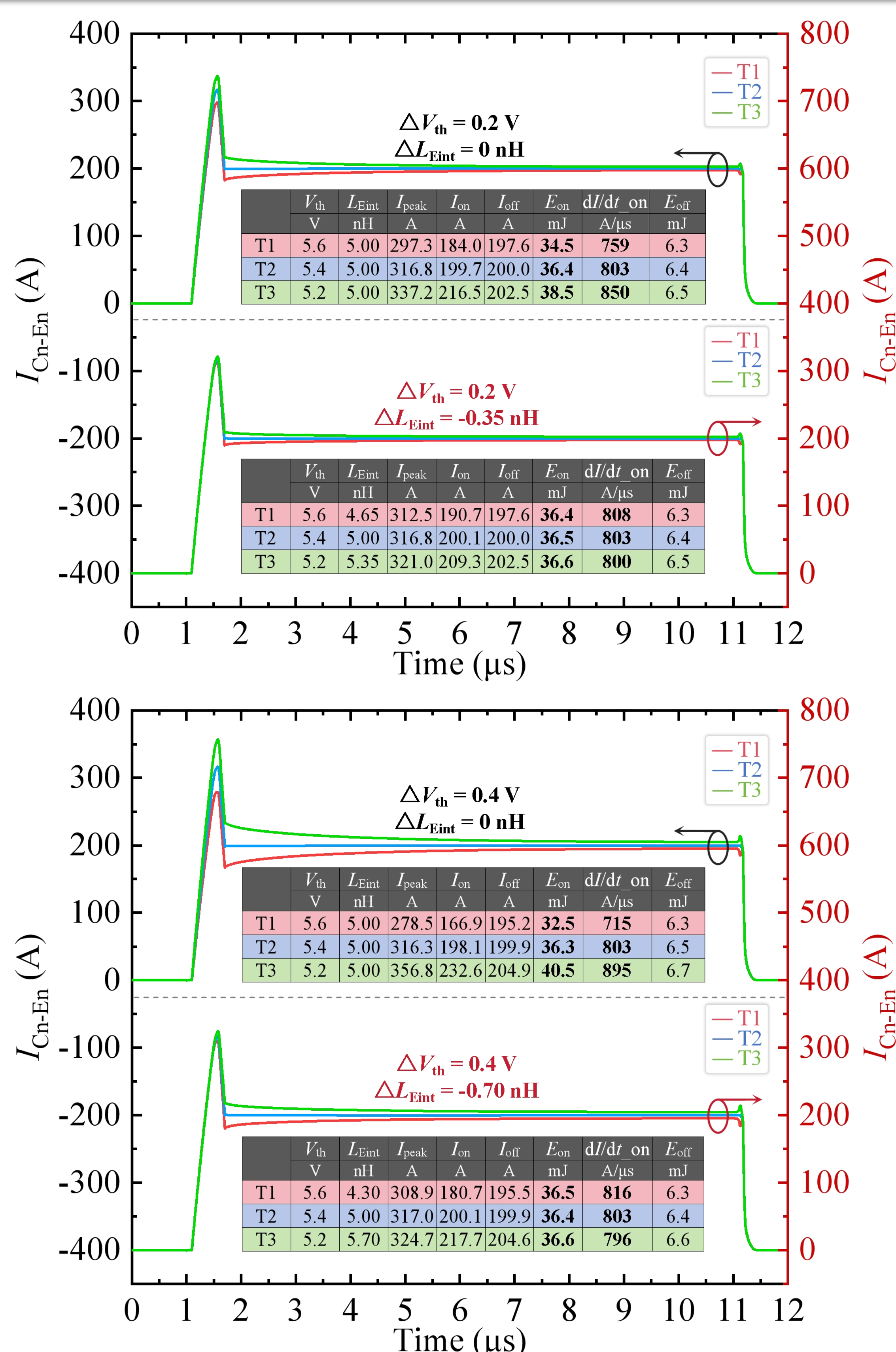


Figure 7. Effects of ΔL_{Eint} on the current sharing.

Effects of ΔL_{Eint} on P_{sw} , P_{con} and ΔT_{vj}

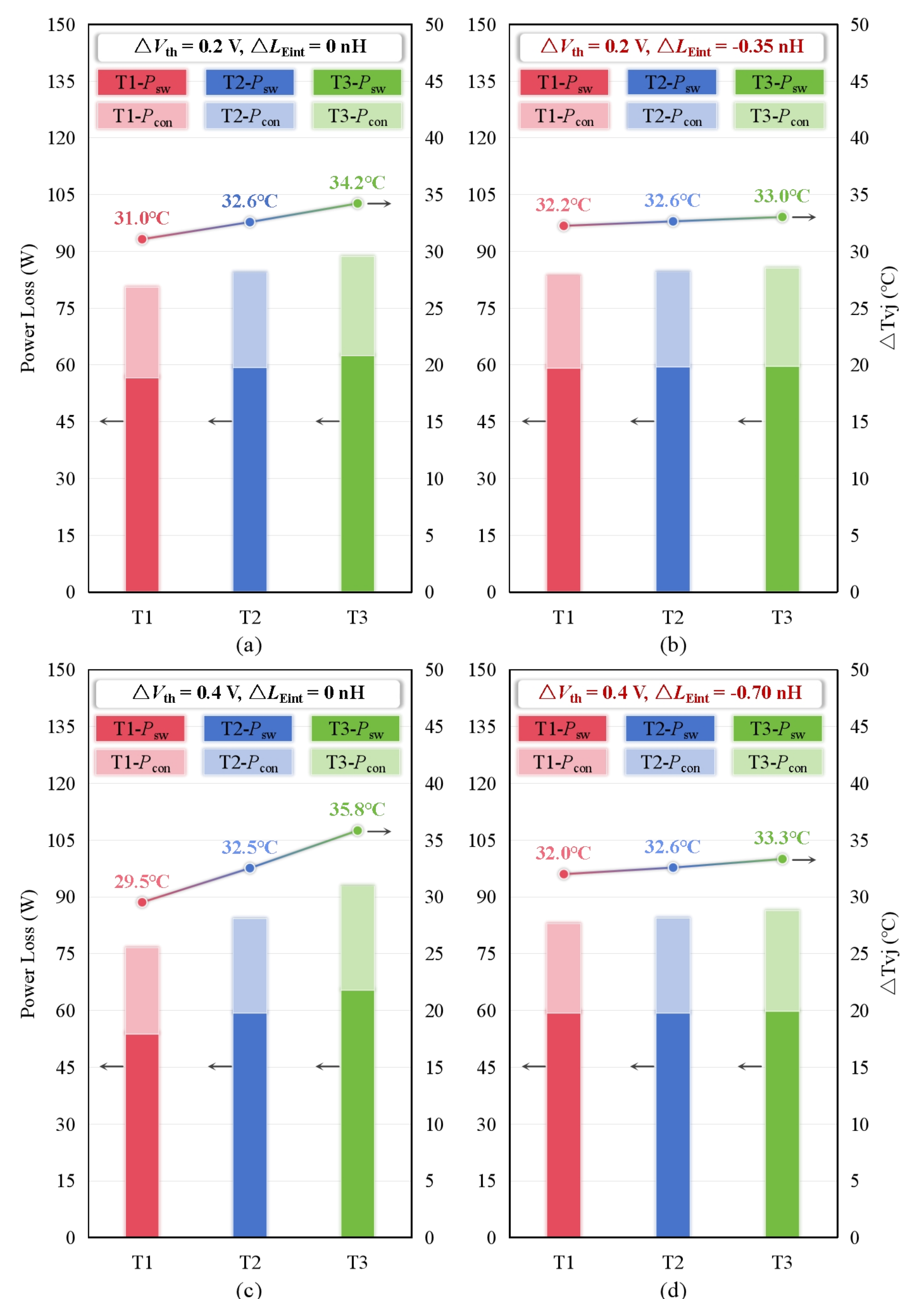


Figure 8. Effects of ΔL_{Eint} on P_{sw} , P_{con} and ΔT_{vj} at $\Delta V_{th} = 0.2$ V and $\Delta V_{th} = 0.4$ V.

Conclusion

This paper investigates the current sharing in the three-chip parallel IGBT modules during the switching process, quantifying the impacts of chip threshold voltage (V_{th}) variations and package emitter parasitic inductance (L_{Eint}) asymmetries. Both factors are the dominant determinants of turn-on current sharing and energy loss with negligible effect on turn-off, and L_{Eint} mismatch causes more severe thermal imbalance than equivalent V_{th} variation. A mutual linear compensation relationship exists between L_{Eint} and V_{th} , either by introducing controlled L_{Eint} asymmetries to offset inherent V_{th} variations, or by matching V_{th} parameters to compensate for package L_{Eint} mismatches, switching losses and junction temperatures across parallel chips can be effectively balanced. Under 250 kW operation, this method reduces the maximum chip temperature difference from 6.3 °C to 1.3 °C, providing a practical optimization approach for high-reliability multi-chip IGBT module design.