

Design Considerations of Active Neutral Point Clamped Inverter for Energy Storage System

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Abstract

The rapid increase in electricity demand driven by various external factors has intensified the need for Energy Storage System (ESS) capable of providing stable and reliable power. In response, grid forming ESS architectures are gaining importance, resulting in higher power requirements within Power Conversion System (PCS). Among the various Neutral Point Clamped (NPC) topologies used in ESS PCS, the Active Neutral Point Clamped (ANPC) inverter offers improved efficiency and reduced thermal stress compared to conventional NPC circuits. To minimize system losses, the combination of IGBTs, Si diodes, and SiC MOSFETs is commonly employed. However, the use of SiC MOSFETs introduces crosstalk challenges that must be addressed for stable operation. This paper presents an effective mitigation strategy for SiC MOSFET induced crosstalk within ANPC inverter. Additionally, it highlights the performance advantages achieved by replacing IGBT and Si diode with RC IGBT.

Introduction

The increasing demand for ESS and the growing requirement for high power operation have led to the need for more efficient PCS designs. Although the ANPC topology involves more complex control compared to conventional NPC, it enables configurations that achieve higher efficiency. In this structure, SiC MOSFETs are employed on the inner switches, while IGBTs with low $V_{CE(sat)}$ and Si Diodes with low forward voltage drop (VF) are used on the outer and neutral point sides. This combination allows the PCS to achieve higher efficiency than traditional NPC implementations. However, the use of SiC MOSFETs introduces several issues associated with their fast-switching characteristics. This paper presents the crosstalk that arises in such configurations and proposes mitigation methods validated on an actual ANPC circuit. In addition, by replacing the IGBT and Si diode combination with RC IGBTs, the results demonstrate reduced device temperature and potential cost savings. The proposed approaches are verified using an ANPC module implemented with onsemi's F5BP package as shown in Fig. 1.

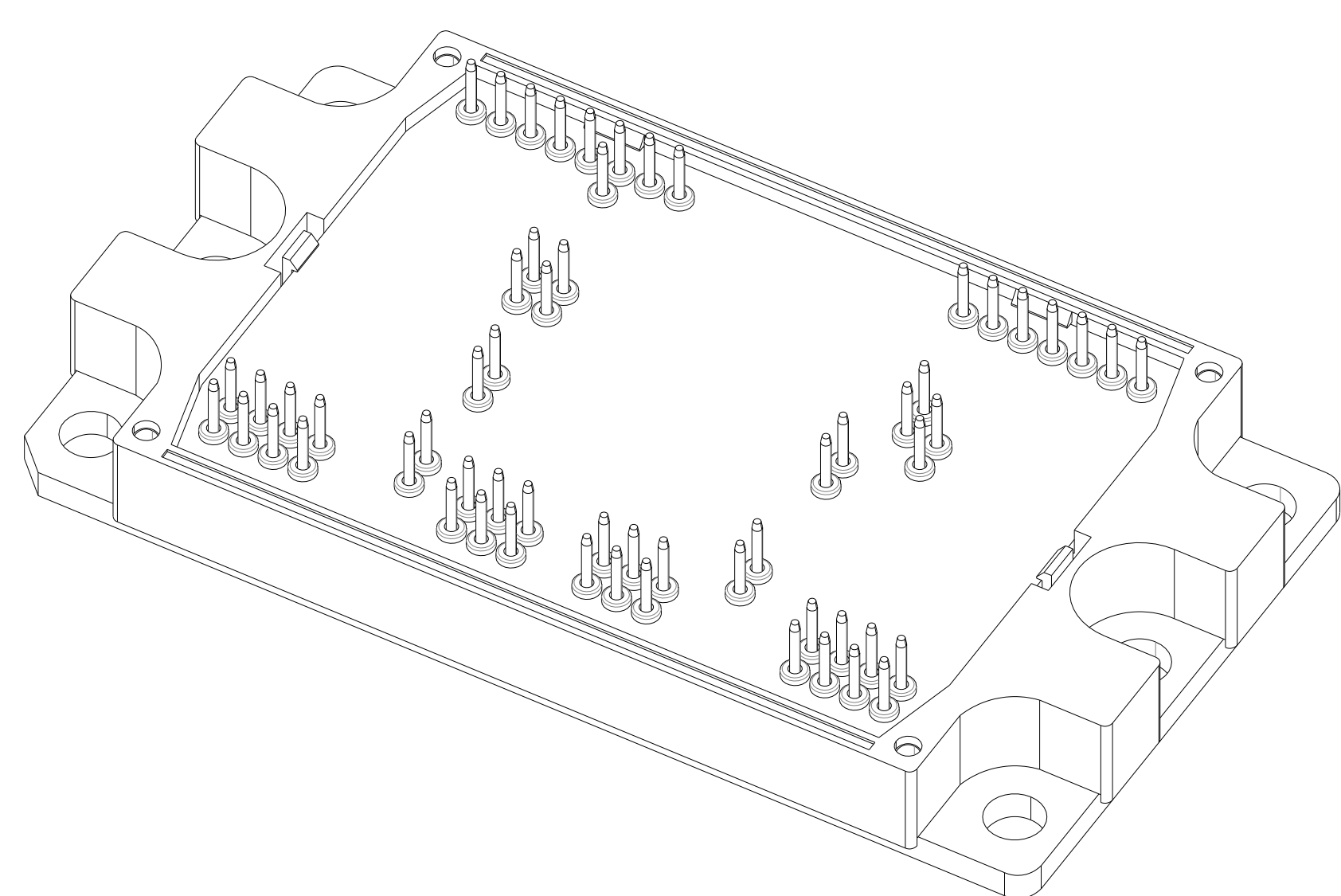


Fig. 1 ANPC Inverter Power Module from onsemi

Design Considerations

The onsemi ANPC module is configured with six parallel connected SiC MOSFETs for the inner switches, while each outer and neutral point switch is implemented using a single IGBT and Si Diode. In this circuit, the SiC MOSFETs operate at the switching frequency, whereas the IGBTs and Si Diodes operate at the line frequency. When the ANPC inverter is implemented using the device combination, several critical design considerations arise. First, the high switching speed of the SiC MOSFET can lead to significant crosstalk effects, which can compromise device reliability. Second, since the current conduction is governed by the line-frequency cycle, the IGBT and Si diode are subjected to relatively high continuous conduction currents for extended durations.

Consequently, the junction temperatures of these devices must be carefully evaluated and managed to ensure reliable inverter operation.

2.1 Crosstalk

When the SiC MOSFETs operate in a complementary manner, their fast-switching behavior generates a high dv/dt , which in turn causes the gate voltage of the non-switching SiC MOSFET to fluctuate. This phenomenon, known as crosstalk, can lead to issues such as false turn-on or gate voltage overshoot beyond the SiC MOSFET's allowable V_{GS} rating, potentially resulting in device failure. To examine the effects of crosstalk, the upper SiC MOSFET is selected as device under test (DUT), while the lower SiC MOSFET is configured to operate in its body diode conduction mode. The simulation is performed using SIMetrix, where each device is modeled with its corresponding SPICE model. In addition, the parasitic inductances and resistances of each node are incorporated using Ansys' Q3D extraction. The simulation circuit is shown in Fig. 2. As shown in Fig. 2, the upper switch is configured as a single device and labeled as M2, while the lower switch

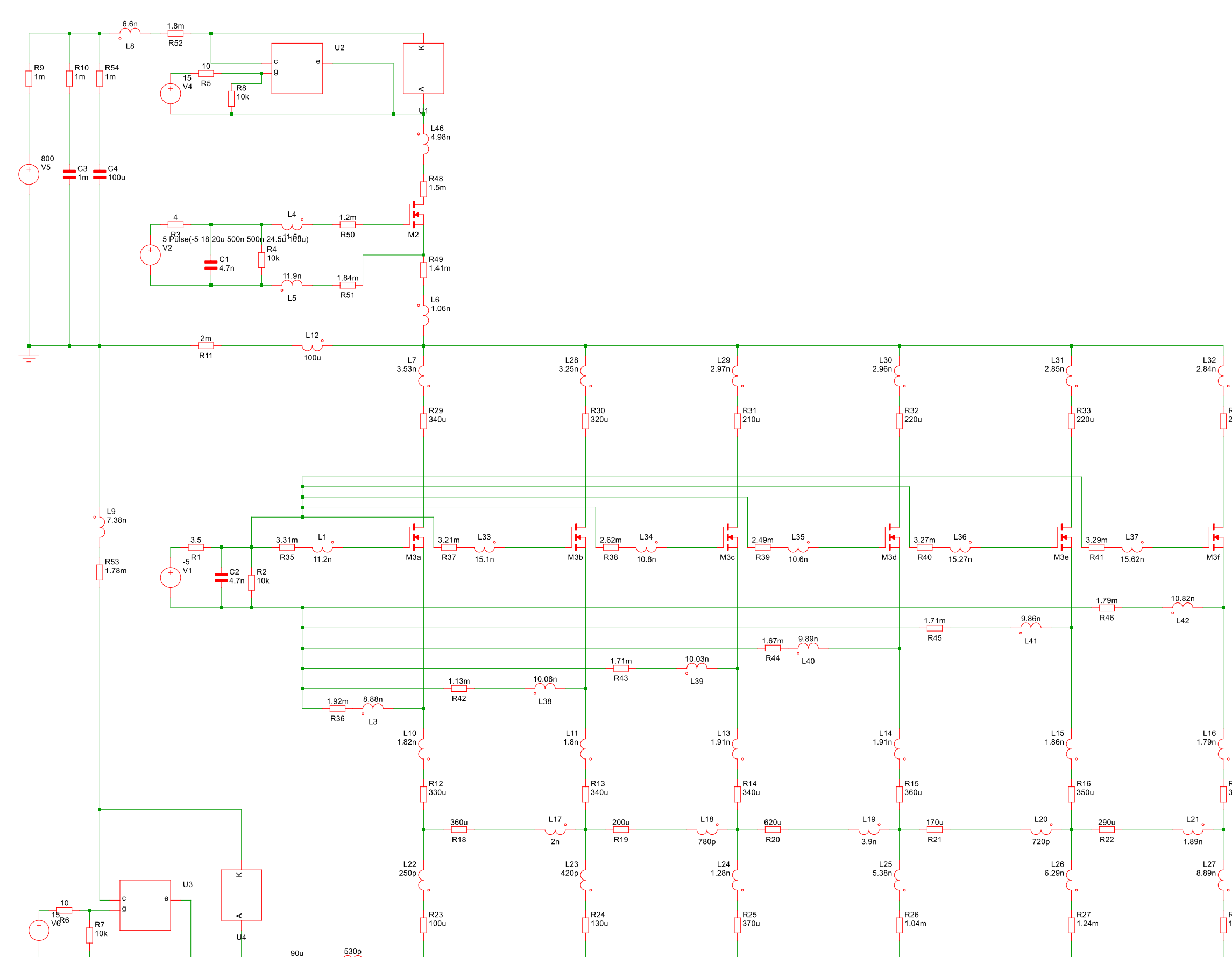


Fig. 2 Simulation Circuit

consists of six parallel-connected devices, designated as M3a, M3b, M3c, M3d, M3e, and M3f. For the simulation conditions, the lower switches are driven with a gate source voltage of -5 V, and crosstalk is evaluated under a current of 600 A. The results shown in Fig. 3 were obtained with Fig. 2 simulation circuit, where the peak gate voltage swings between +5 V and -17 V. Since the actual V_{GS} rating of the onsemi SiC MOSFET is +22 V to -10 V, such voltage overshoot may potentially damage the device. Fig. 4 shows the corresponding crosstalk simulation results with modified circuit in which the parasitic inductances on the source side are equalized. As a result, the crosstalk is significantly reduced compared to the previous case. Fig. 5 shows the simulation results obtained under identical operating conditions with individual gate resistors (10 Ω) added to the parallel SiC MOSFETs while maintaining the same stray inductances as those shown in Fig. 2. Compared with the case shown in Fig. 3, the crosstalk is reduced. The maximum V_{GS} is -0.5 V, while the minimum V_{GS} reaches -8.6 V. However, larger V_{GS} fluctuations are observed compared to the symmetric layout without additional gate resistors as Fig. 4.

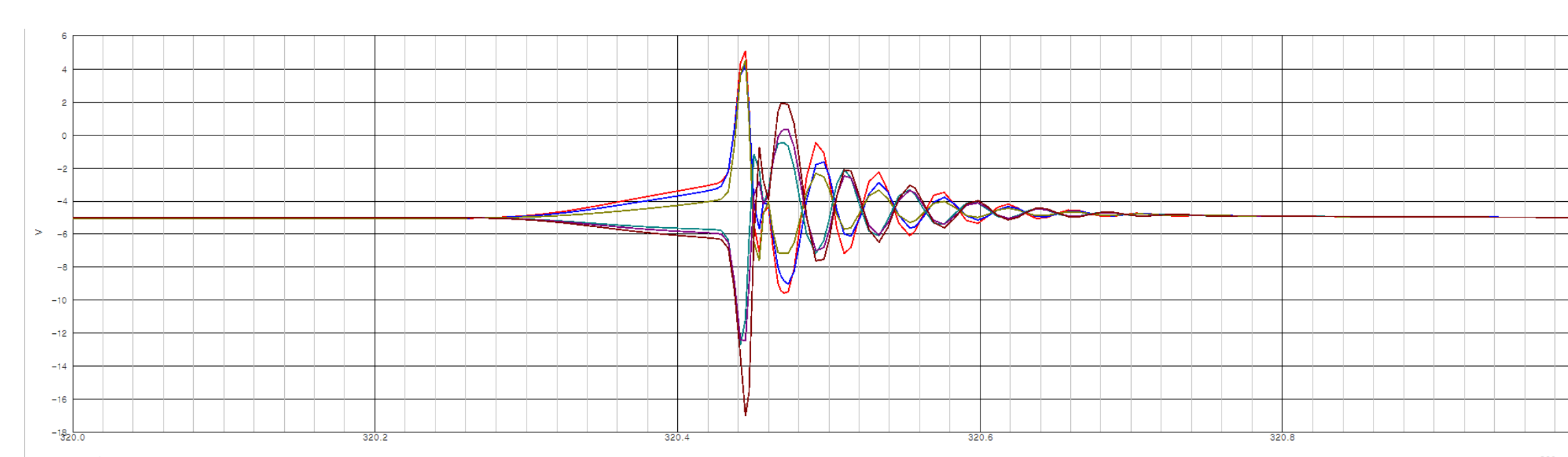


Fig. 3 Crosstalk with Asymmetric Source Stray Inductance

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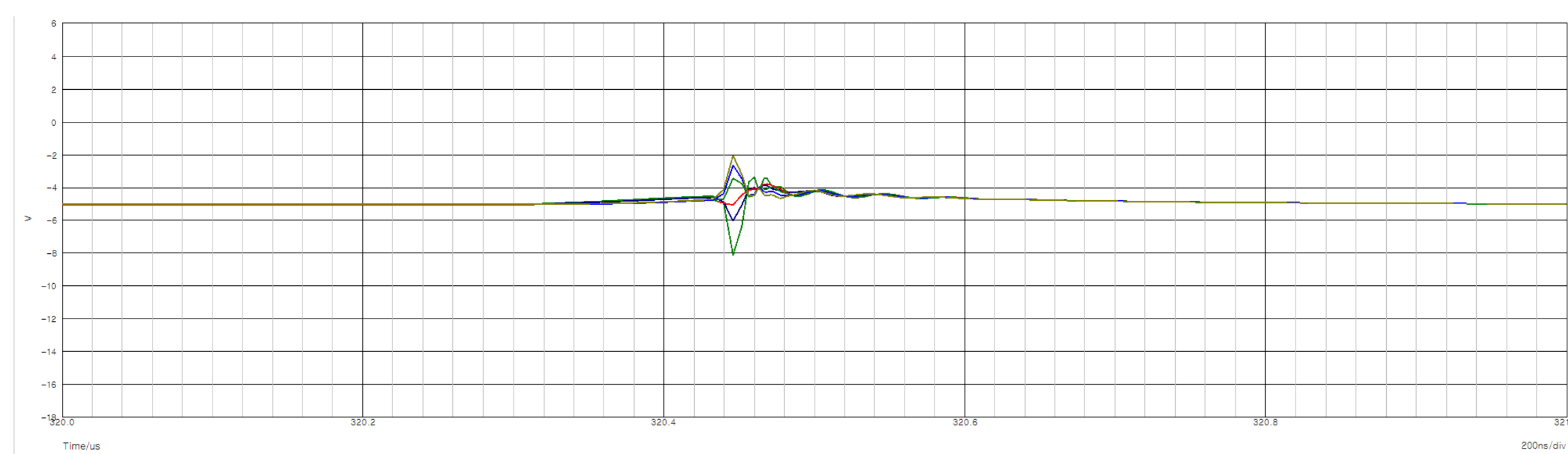


Fig. 4 Crosstalk with Symmetric Source Stray Inductance

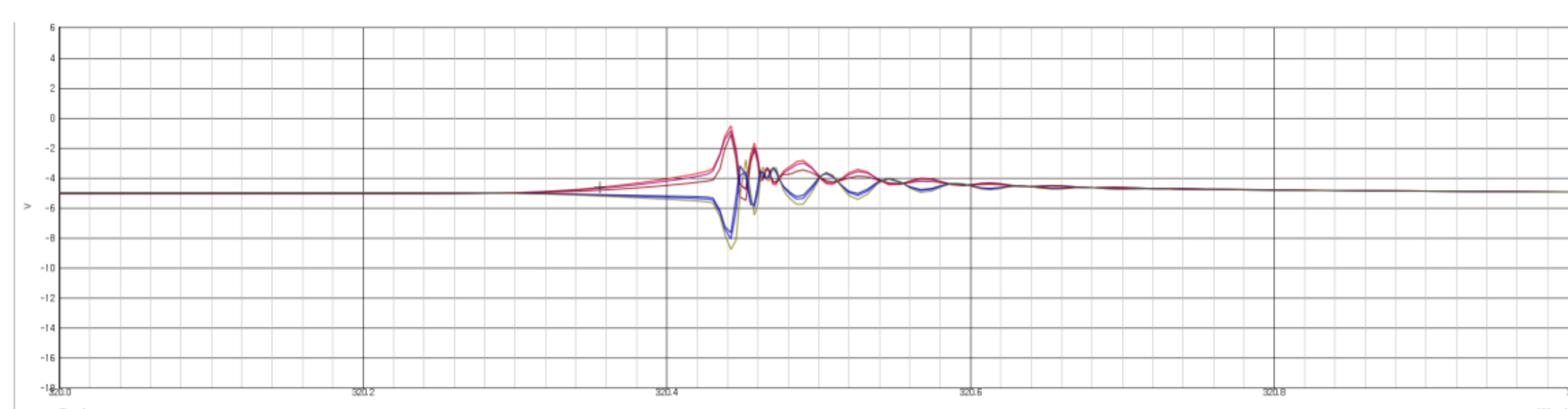


Fig. 5 Adding Gate Resistor with Asymmetric Source Stray Inductance

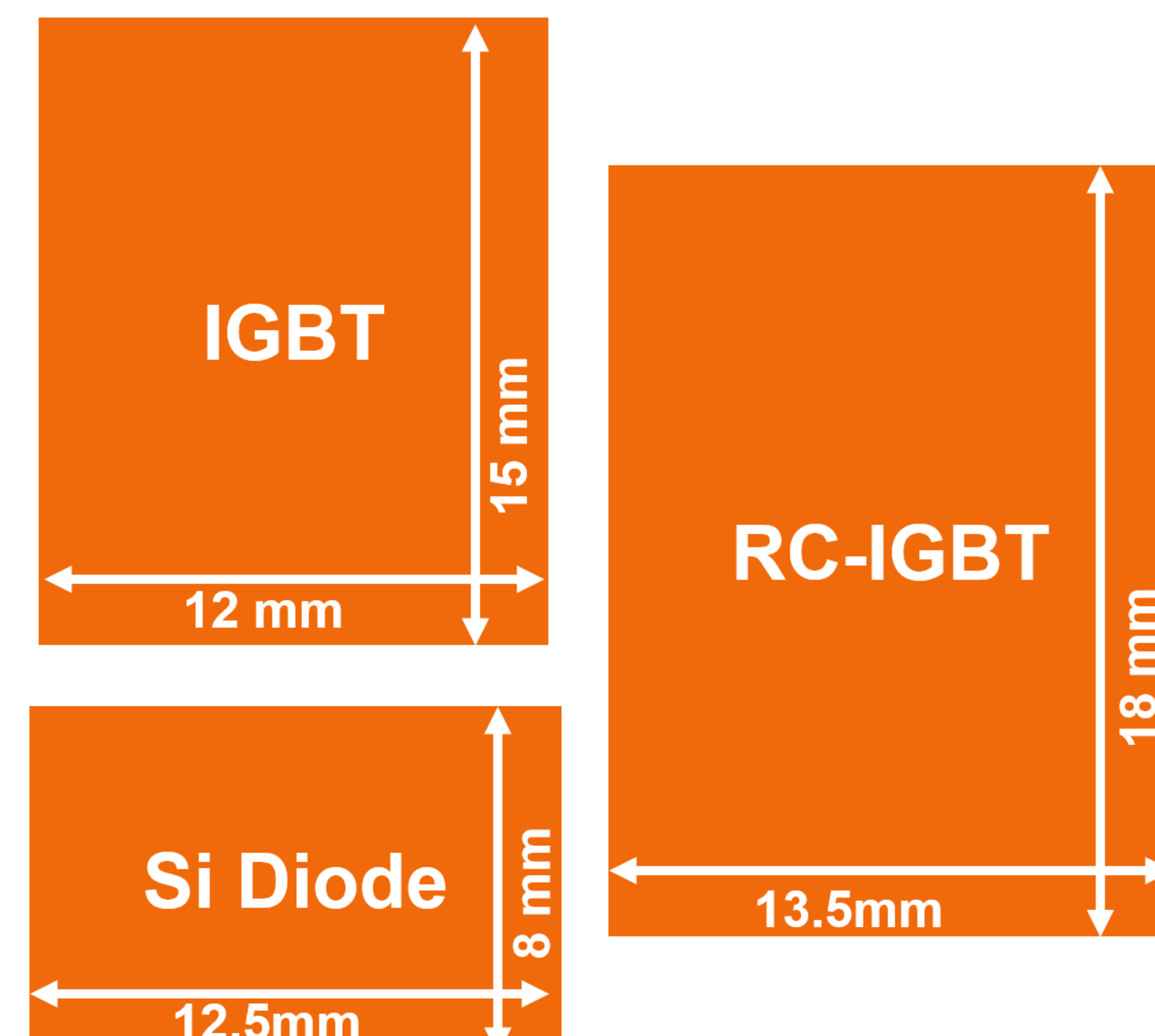


Fig. 6 Comparison of Chip Areas for IGBT, Si Diode, and RC-IGBT

Therefore, it can be concluded that a symmetric layout is more effective than the addition of gate resistors for suppressing crosstalk, making it the most effective design approach for mitigating crosstalk in parallel SiC MOSFETs.

2.2 RC-IGBT

In the ANPC topology considered in this study, the IGBT and Si diode operate at the line frequency. During operation, neither switching losses nor reverse-recovery loss are generated, and only conduction loss is present. Specifically, the IGBT conducts when the power factor is $PF = 1$ which is the battery discharging mode, whereas the Si diode conducts when $PF = -1$ which is the battery charging mode. Under these conditions, the current continuously flows through the devices according to the line-frequency, resulting in a significantly longer conduction interval compared with switching-frequency operating. Consequently, the junction temperature of the devices can increase substantially. To mitigate this issue, either thermal resistance or the conduction loss must be reduced. Reducing conduction loss requires lowering the forward voltage drop, such as $V_{CE(sat)}$ for the IGBT or V_F for the diode; however, the achievable reduction is inherently limited by device characteristics. Therefore, increasing the device chip size to reduce thermal resistance is considered a more effective approach. A conventional IGBT does not contain an intrinsic body diode and therefore requires an antiparallel diode for reverse-current conduction. In contrast, an RC-IGBT incorporates a diode structure within the IGBT itself, allowing reverse conduction through a single device. Furthermore, a conventional IGBT + Si diode implementation requires two separate chips, which limits the available die area for each device. By integrating both functions into a single RC-IGBT, a larger chip area can be utilized within the same package constraints. As a result, the RC-IGBT can achieve lower thermal resistance due to its larger chip size while maintaining $V_{CE(sat)}$ and V_F characteristics comparable to those of the conventional IGBT + Si diode configuration. Therefore, the conduction loss can be preserved at a similar level while significantly improving the thermal performance of the device. This design approach offers a substantial advantage in terms of junction temperature reduction and overall thermal management. To verify the thermal performance under actual overload conditions, the junction temperature characteristics of the conventional IGBT + Si diode configuration and the RC-IGBT are compared. The operating conditions are set for $V_{bus} = 1500$ Vdc, $V_{ac} = 690$ Vac, and $P_{out} = 360$ kW. For a fair comparison, the RC-IGBT chip area is assumed to be 1.35 times larger than that of the IGBT and 2.43 times larger than that of the Si diode as shown in Fig. 6. In the conventional configuration, the maximum conduction loss of the IGBT is 165 W, resulting in a maximum junction temperature of 108 °C. The Si diode exhibits the same maximum conduction loss of 165 W, while its maximum junction temperature reaches 122 °C.

The RC-IGBT is designed to provide the same conduction loss as the conventional IGBT + Si diode configuration. Under these conditions, the maximum junction temperature of the RC-IGBT is 99 °C when operating in the IGBT conduction mode and 94 °C when operating in the reverse conduction (body diode) mode. These results demonstrate that, despite exhibiting comparable conduction losses, the RC-IGBT achieves significantly lower junction temperatures due to its larger chip size and reduced thermal resistance. Therefore, the RC-IGBT offers superior thermal performance under overload conditions compared with the conventional IGBT + Si diode solution.

Conclusion

This paper analyzed the key design considerations of an ANPC inverter for high-efficiency string energy storage system (ESS). In the proposed topology, only the inner switches operate in a complementary switching manner, while the outer and neutral-point devices operate at the line frequency, resulting in conduction loss only. To minimize switching losses, SiC MOSFETs are employed for the inner switches. In addition, IGBTs and Si diodes with low $V_{CE(sat)}$ and V_F characteristics were utilized for the outer and neutral-point devices to reduce conduction loss. As a result, the proposed ANPC topology achieved higher efficiency than the conventional NPC inverter employing IGBTs and SiC Schottky barrier diodes (SBDs). However, several design challenges associated with the proposed ANPC topology must be considered. As discussed in this paper, the high switching speed of SiC MOSFET can induce significant crosstalk effects. This effect may cause the gate-source voltage to exceed the rated gate voltage or the device threshold voltage, potentially leading to device degradation or unintended switching events. To mitigate this issue, two approaches were investigated. The first approach employs individual gate resistors for each device to suppress gate-voltage oscillations. The second approach utilizes a symmetric layout structure, which was shown to be more effective in reducing crosstalk by minimizing parasitic inductance im-balance. Furthermore, for the line-frequency-operated devices that experience only conduction loss, the use of an RC-IGBT was proposed as an alternative to the conventional IGBT and Si diode combination. By integrating the reverse conducting diode into the IGBT structure, the RC-IGBT enables a larger chip area within the same package constraints, thereby reducing the thermal resistance and lowering the junction temperature while maintaining comparable conduction loss. The results demonstrate that both crosstalk mitigation through symmetric layout design and thermal performance improvement through the adoption of RC-IGBTs provide significant advantages for the practical implementation of high-efficiency ANPC inverter. Therefore, these design considerations are essential for improving the reliability, thermal performance, and overall efficiency of ANPC-based string ESS application.