

Effects of Gate Stress on Parameter Stability and Switching Losses in SiC MOSFETs

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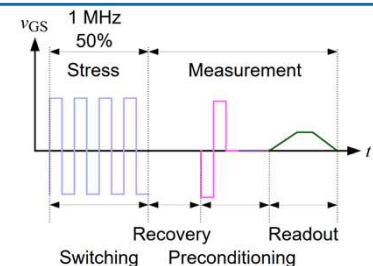
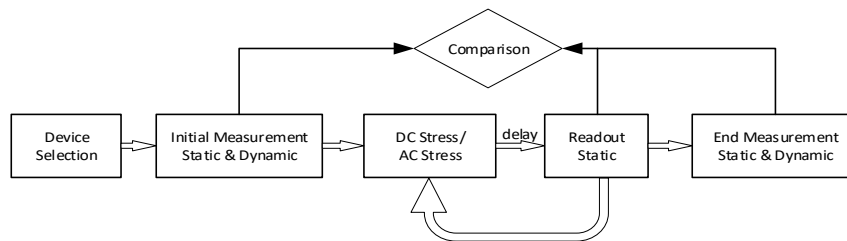
INTRODUCTION

- This work focuses on a systematic investigation of gate stress effects for the application in SiC MOSFETs.
- Six different vendors are tested under DC and AC gate stress with the application relevant condition.
- Usually, only V_{th} is evaluated with gate stress test. In this work the drift is evaluated in key electrical parameters as well as dynamic behavior, such as V_{th} , on resistance (R_{dson}), capacitances, gate charge, and switching losses.

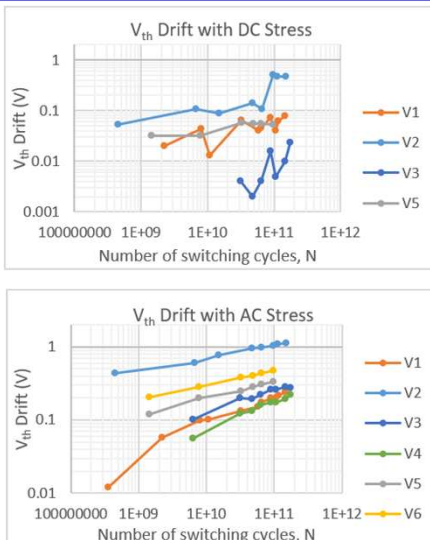
MEASUREMENT CONDITION

Parameter	Description
Package	TO-247-4L
Resistance	50-75 mΩ
Gate structure	Planar/Trench
Vendor	Trench: V1, V2, V5 Planar: V3, V4, V6
AC gate stress	$V_{GS, on} / V_{GS, off}$: +18 V / -5 V
AC gate stress frequency	1 MHz
AC gate stress duty cycle	50%
DC gate stress	$V_{GS, on}$: +20 V
DUT junction temperature	120°C, 150°C

TEST PROCEDURE

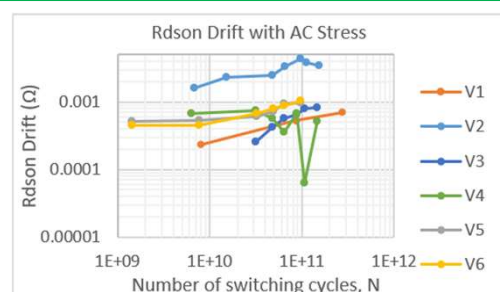


V_{TH}



- V_{th} increases exponentially on a linear scale.
- For all vendors, compared with DC stress, AC stress results in much higher drift.
- The AC drift can vary significantly across different technologies.
- The drift is not sensitive to trench or planar gate structure. Both structures could result in either high or low drift.

R_{DS(on)}



- Vendor V2 exhibits highest R_{dson} drift: with an increase of about 5 %, while the other vendors show only about 1-2 % increase, which indicates larger V_{th} drift tends to have larger degradation in R_{dson} .

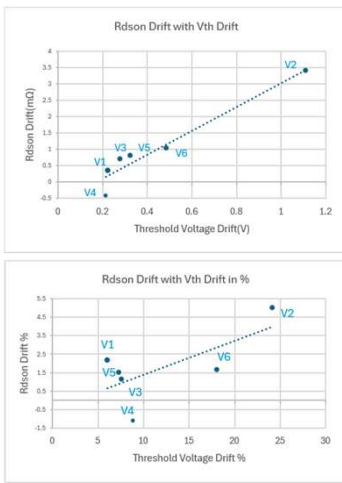
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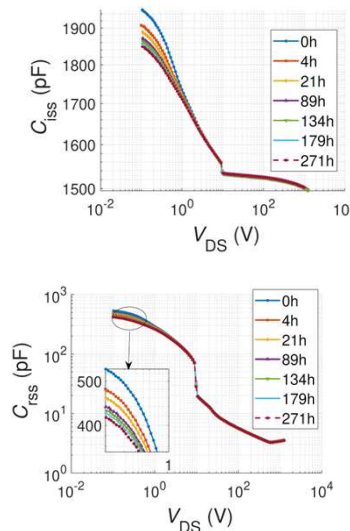
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RDSON VS. VTH DRIFT



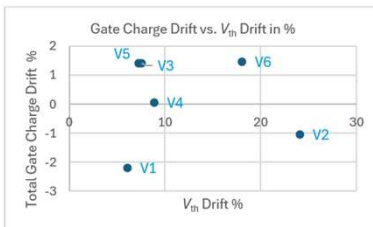
- $R_{ds(on)}$ drift is linearly related to V_{th} drift in absolute value

CAPACITANCE

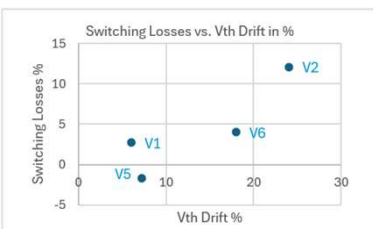


- At low drain source voltages, the capacitances are sensitive to stress time, while at higher voltages, the degradation tends to be limited.
- Vendor V6 shows the largest decrease (about C_{iss} 5.1 %, C_{oss} 6.7%, C_{rss} 20% at $V_{ds} = 0$ V), and the drift happens below 1 V region.
- The impact of gate stress with device capacitances for the application is negligible

DYNAMIC TEST

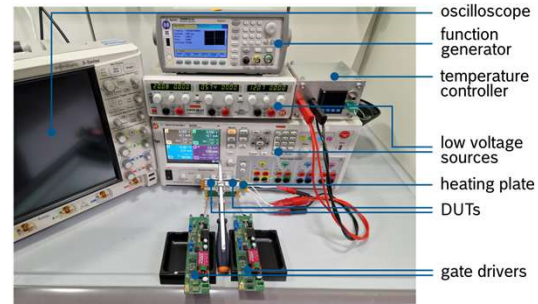


- Q_{gtot} remains largely unaffected for most vendors, indicating that the overall gate drive energy is not severely impacted.



- Compared with evident V_{th} drift after the gate stress, however, the switching losses do not show significant drift.

CONCLUSION



- This work demonstrates the correlation between V_{th} drift and $R_{ds(on)}$ drift as well as switching losses, providing a quantitative framework for designers to establish more accurate end-of-life criteria for SiC based systems.
- The degradation is highly dependent on technology, but not sensitive to trench or planar structure.
- A higher V_{th} drift in absolute value tends to result in higher $R_{ds(on)}$ drift. If considering more parameters such as capacitance, gate charge or switching performance, one technology may perform well in certain parameters but poorly in other parameters.
- The impact of gate stress is not limited to one parameter, such as the commonly evaluated V_{th} ; multiple parameters need also to be assessed to ensure a robust system design over lifetime. This study highlights the effects of degradation and delivers long term design insights for system employing SiC MOSFETs.