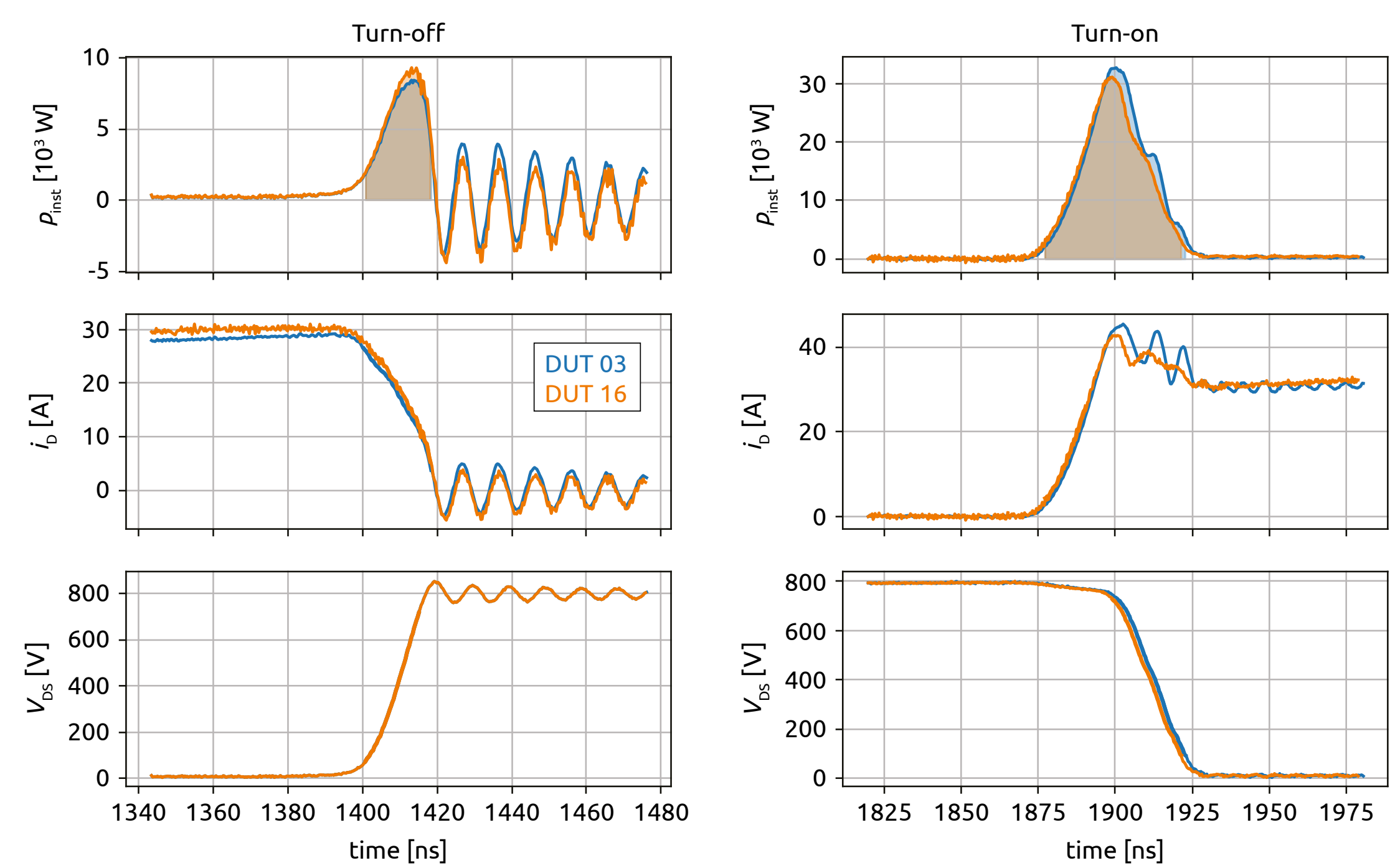


Impact of V_{th} mismatch, layout symmetry and gate resistance on current sharing in parallel SiC MOSFETs

Nima Lotfi¹, Thilo Steinbock², Reinhold Elferich¹, Sebastian Fahlbusch¹, Klaus F. Hoffmann² | nima.lotfi@nexperia.com

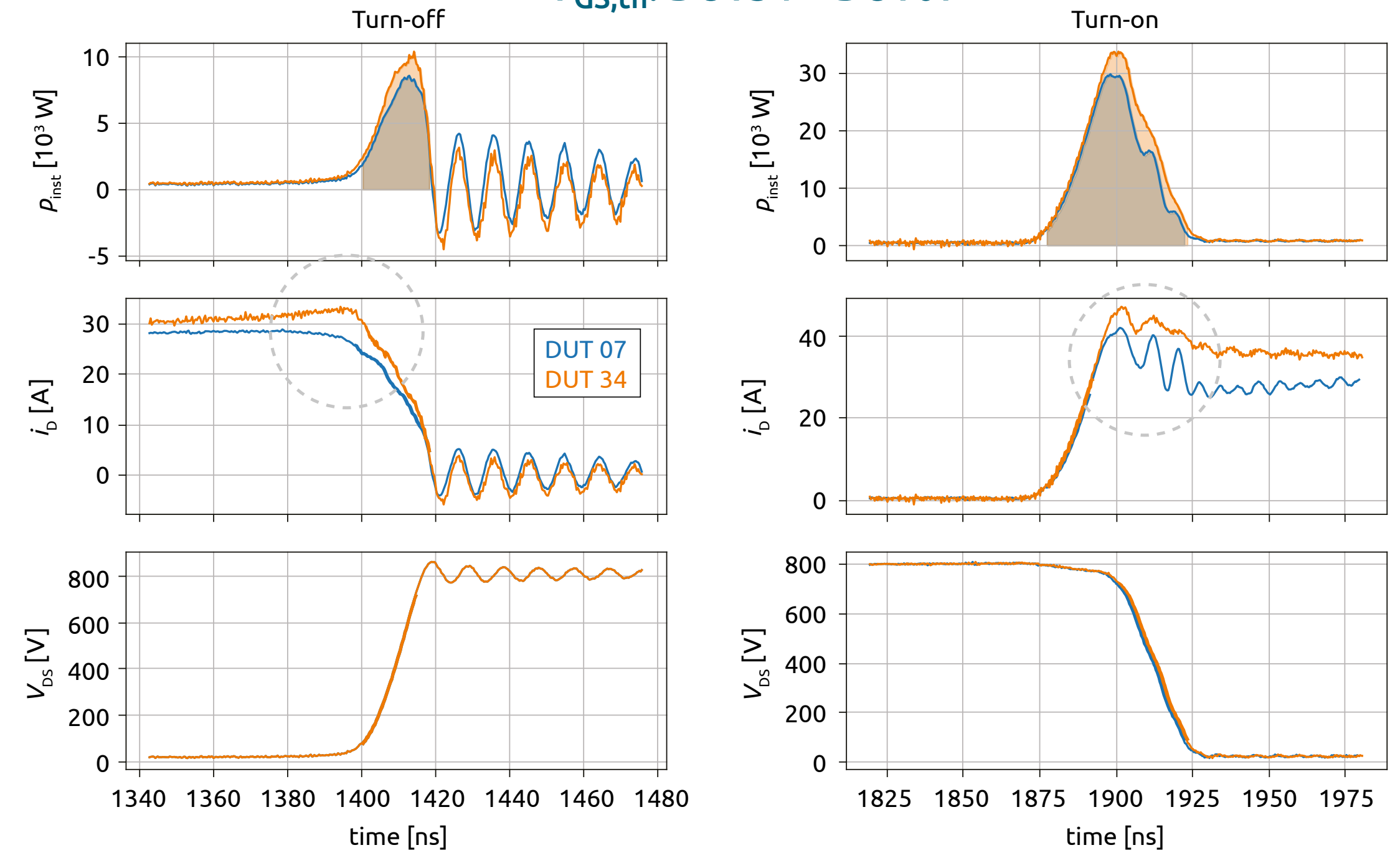
¹Nexperia Germany GmbH, Germany ²Helmut-Schmidt-University, Germany

Case I: Symmetric layout - $V_{GS,th}$ -matched

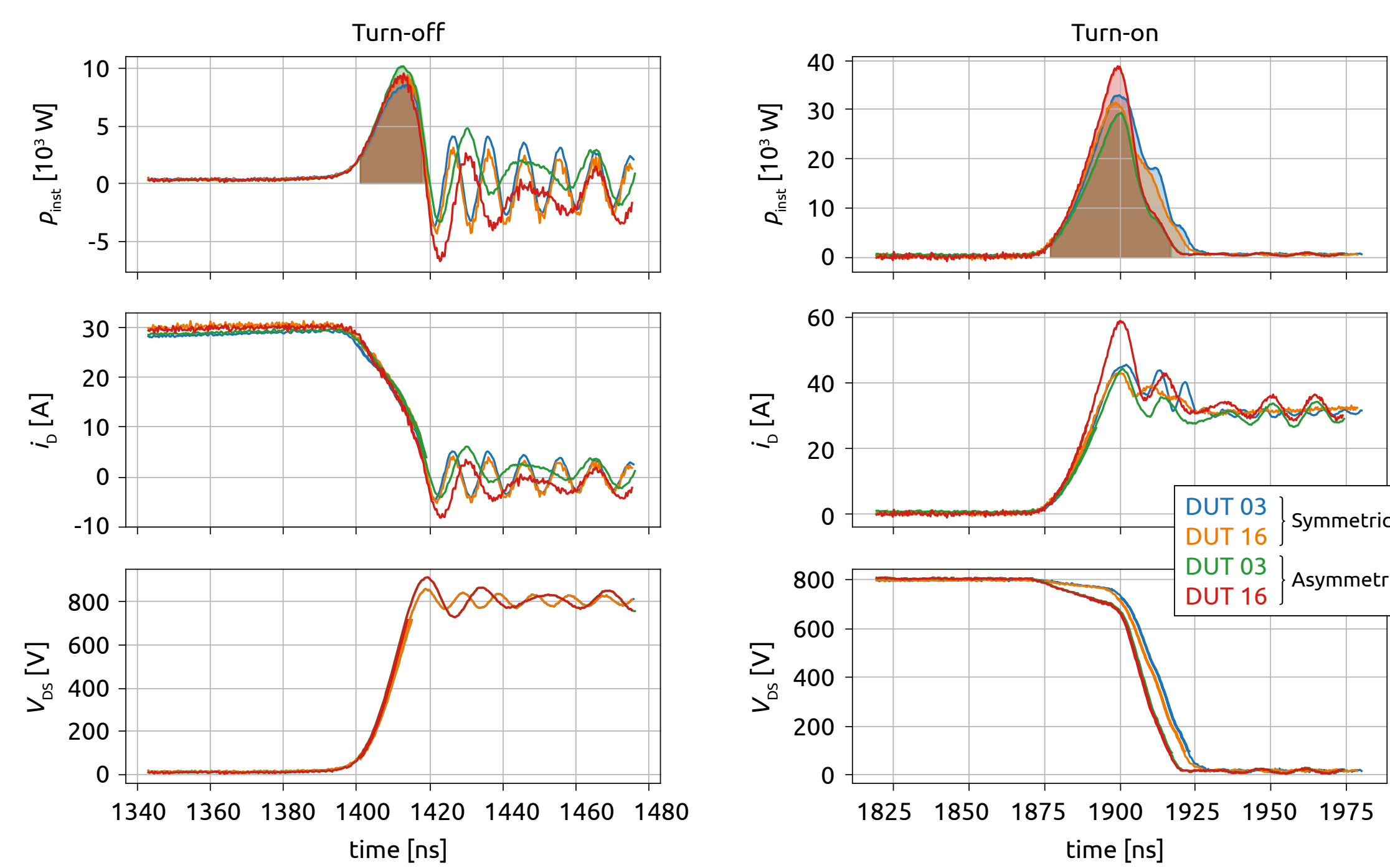


Case I: Symmetric layout - $V_{GS,th}$ -unmatched

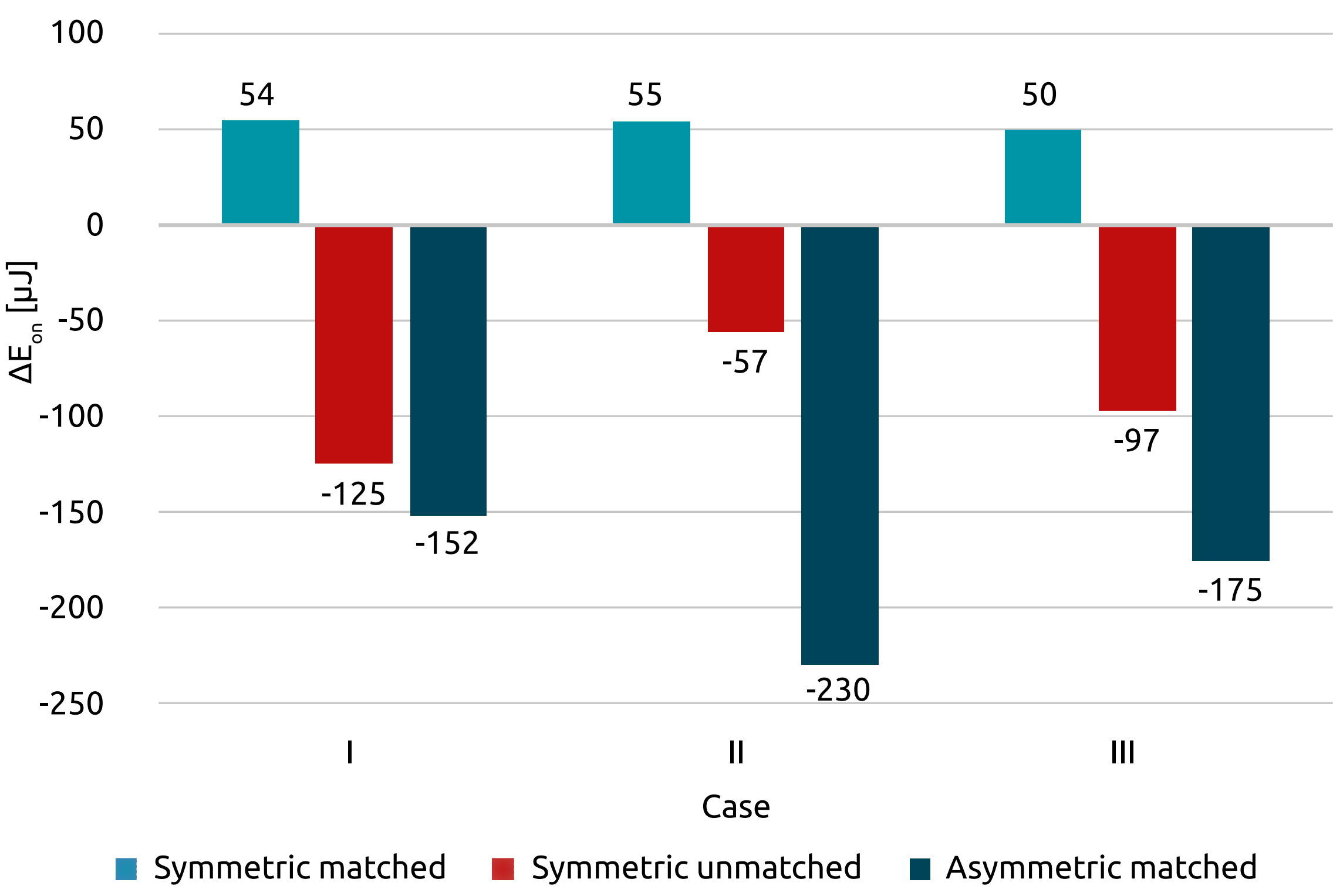
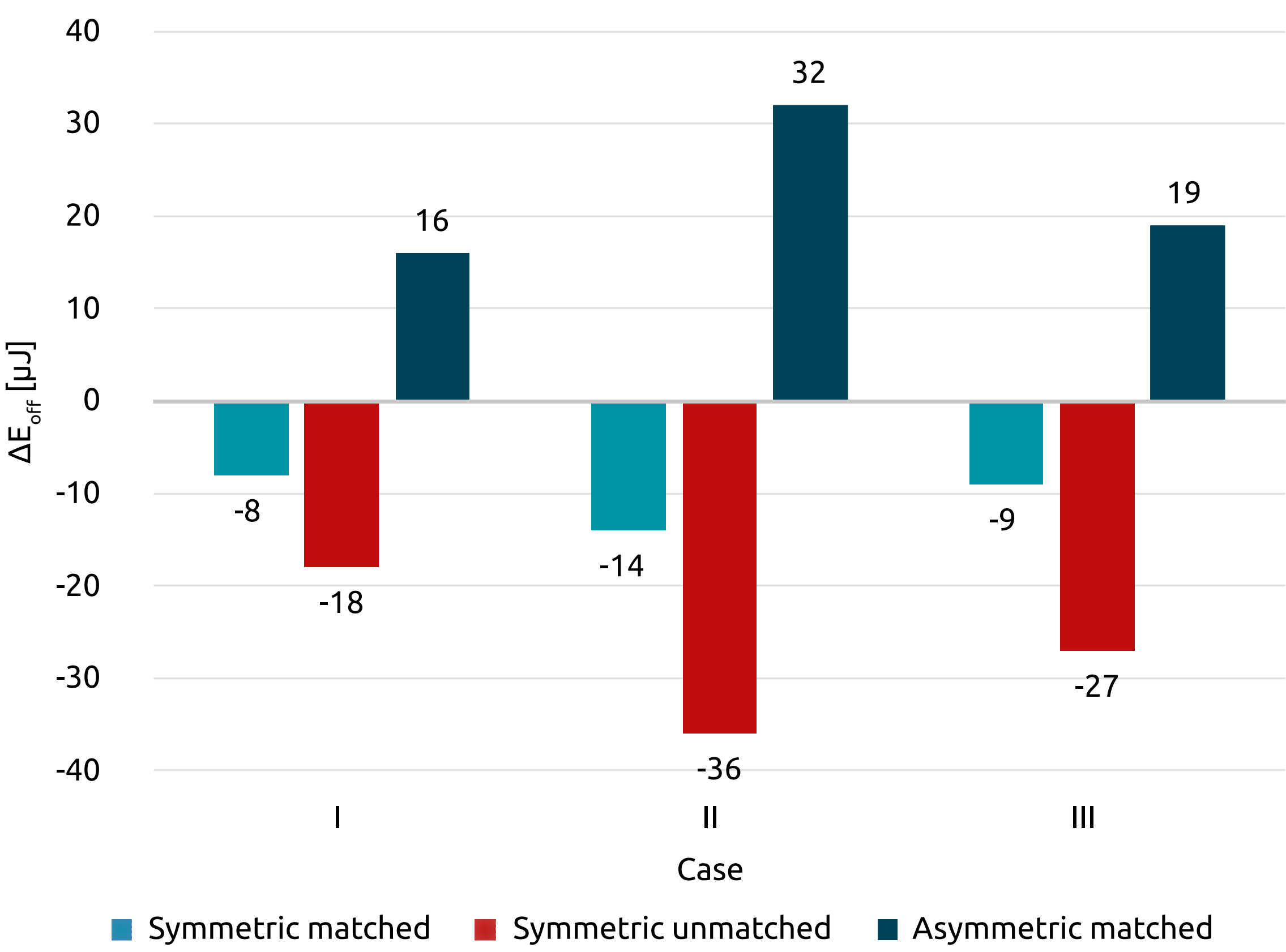
$V_{GS,th}$: DUT34 < DUT07



Case I: Symmetric vs. asymmetric layout - $V_{GS,th}$ -matched



Influence on Switching Energy Distribution



$\Delta E_{xx} = E_{xx,Q3(left)} - E_{xx,Q4(right)}$,
negative values indicate higher switching energy in Q4.

Conclusion

- A. $V_{GS,th}$ mismatch is the dominate source of current imbalance.
- B. The lower $V_{GS,th}$ device experiences higher current stress.
- C. Layout asymmetry changes switching-loss distribution, while current sharing remains balanced.
- D. $R_{G,ext}$ placement mainly affects transients, not current sharing.

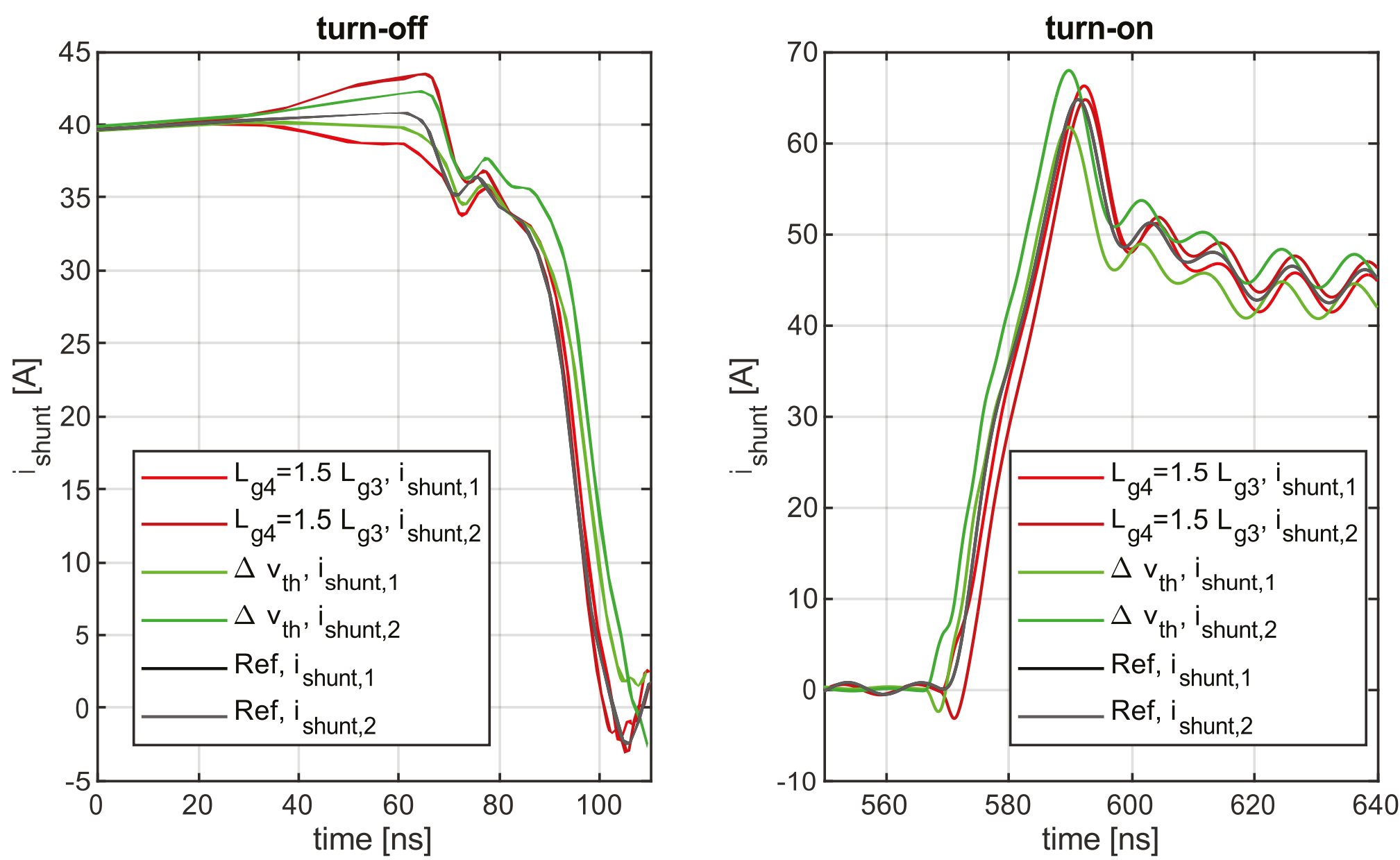
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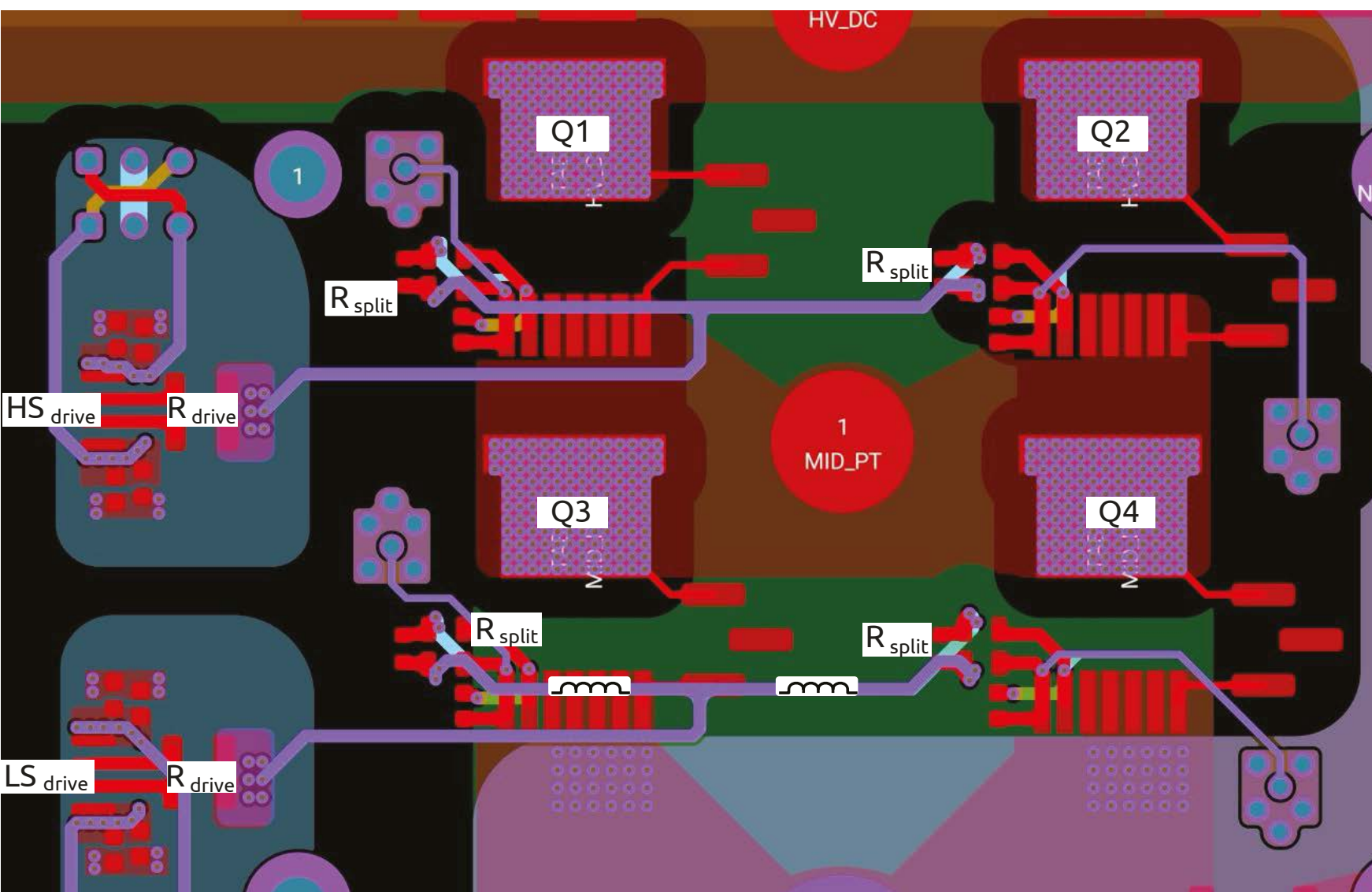
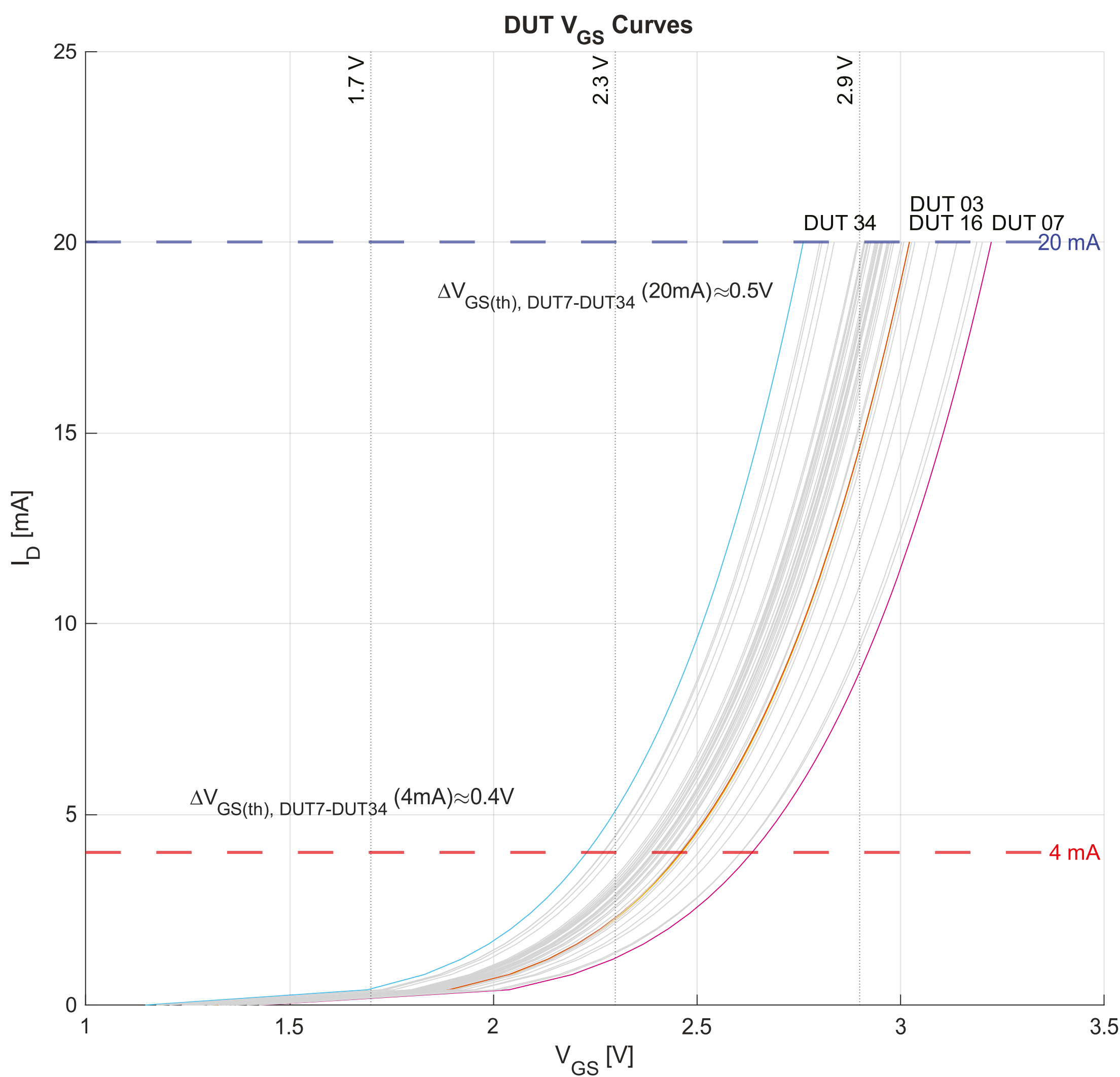
Motivation

- **Rising power demands drive parallelization:**
Increasing power levels in converters require paralleling SiC MOSFETs, but this introduces challenges in device operability.
- **Quantifying impact of design vs. device parameters:**
While intrinsic variations like $V_{GS(th)}$ are known to matter, the relative influence in combination with external factors needs to be assessed.

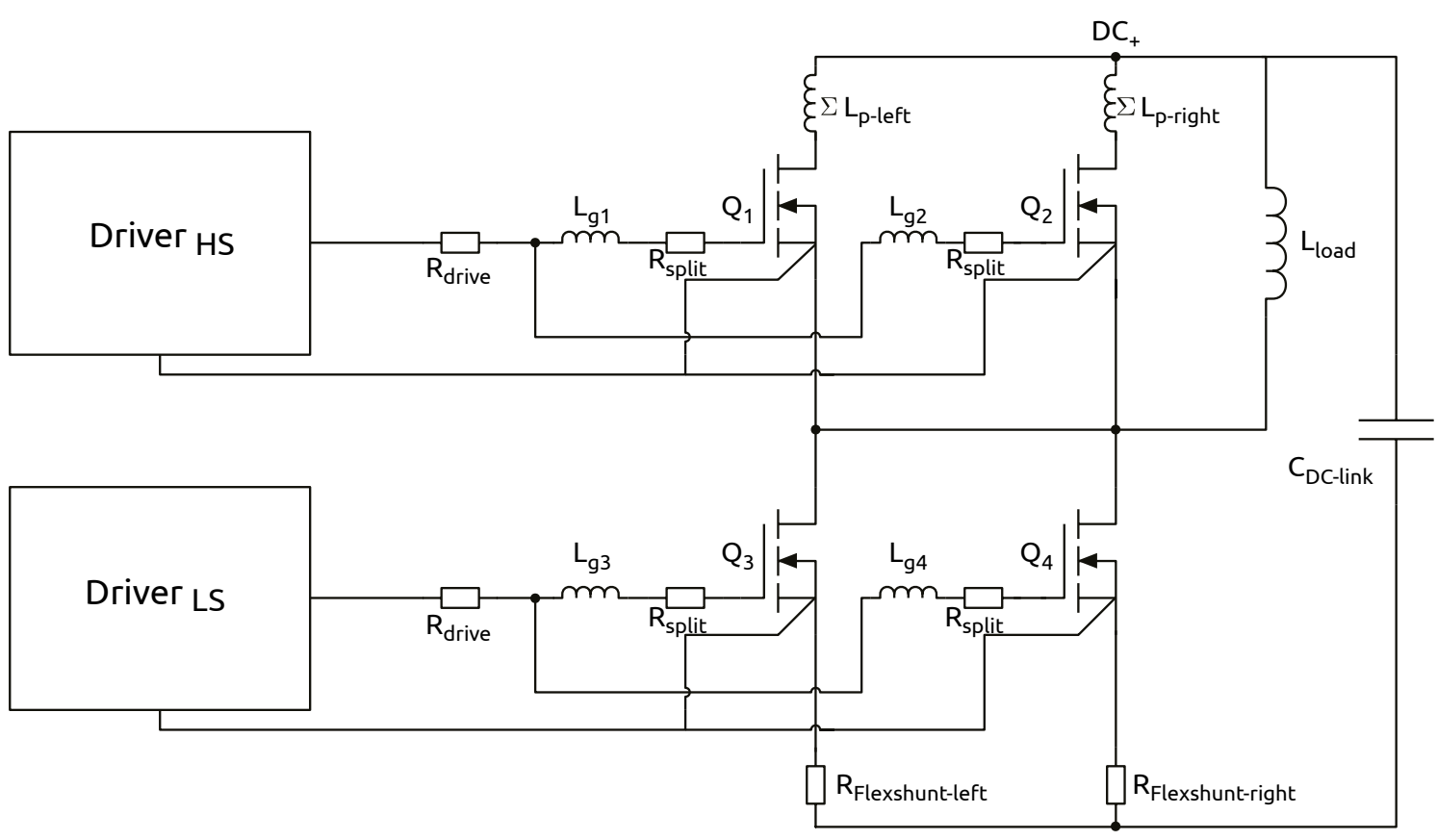
Ltspice sensitivity study



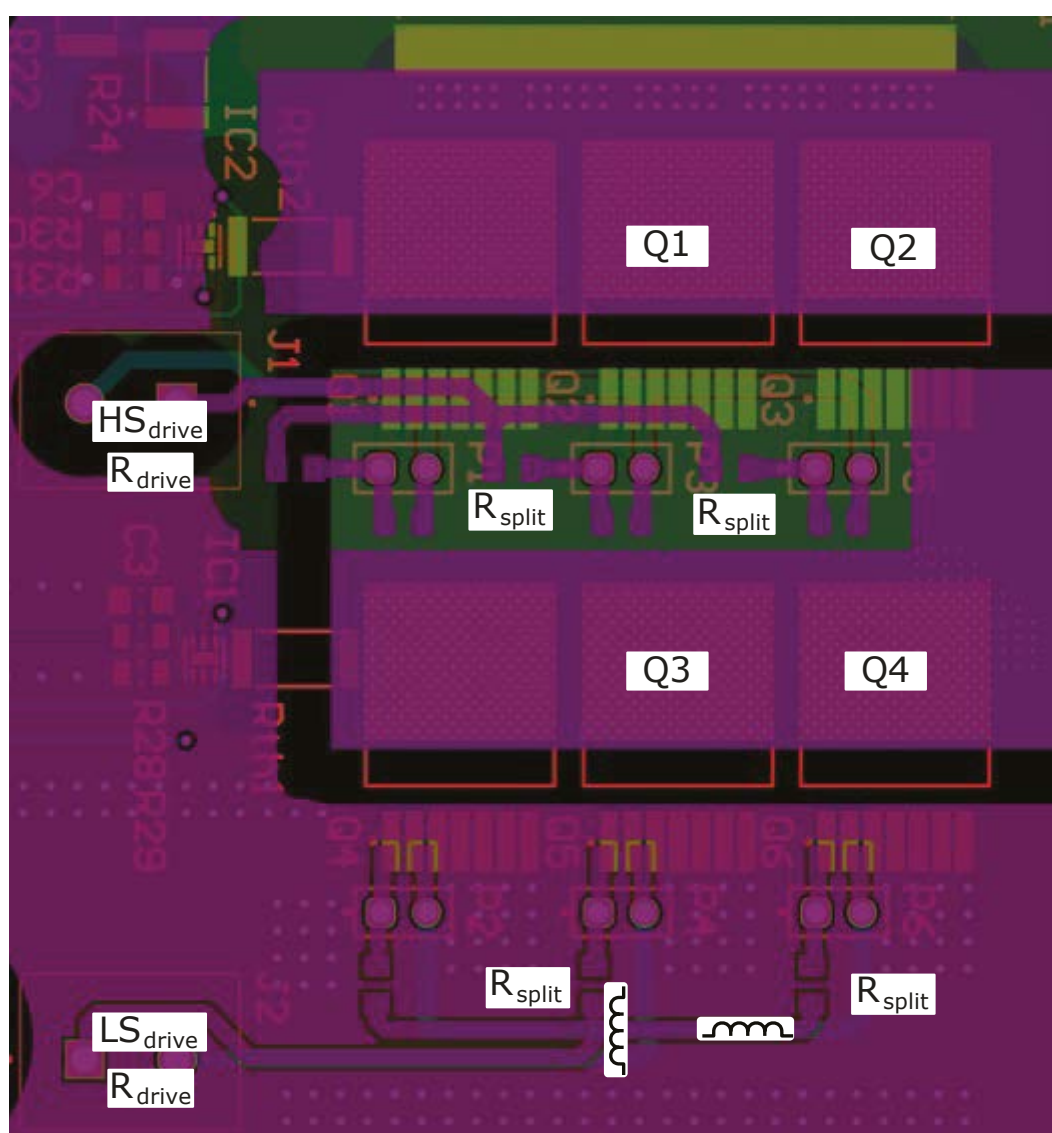
Pre-characterization of DUTs



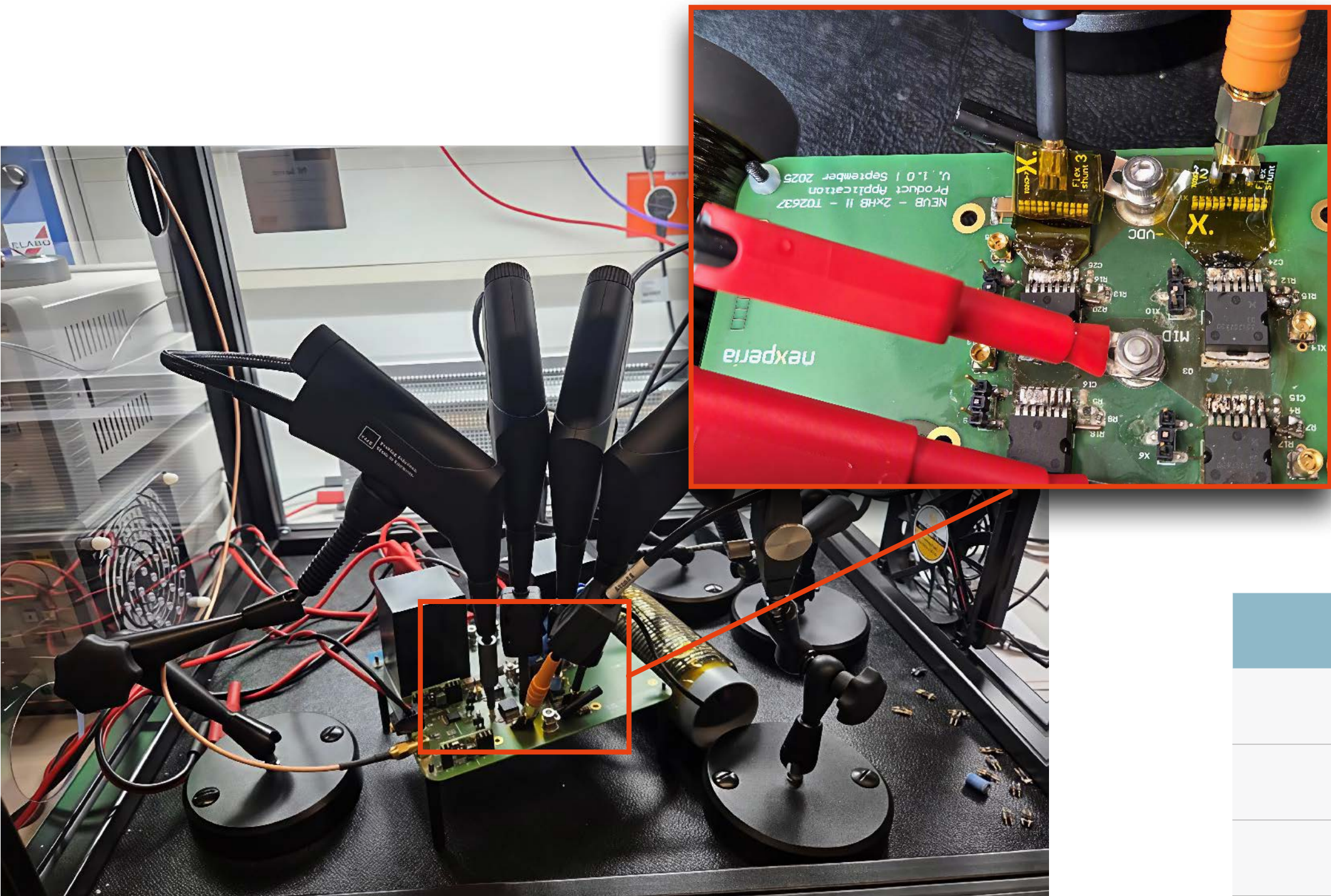
Symmetric Layout



Schematic | $R_{G,external}$ cases



Asymmetric Layout



Case	R_{drive} [Ω]	R_{split} [Ω]
I	0	10
II	5.6	0
III	3	4.3

