

Research on Packaging Structure of T-Type Three-Level GaN/SiC Hybrid Power Module

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Abstract

This work develops a low-inductance package for a T-type three-level GaN/SiC hybrid power module aimed at 800 V electric drives. A modular laminated DBC substrate and strictly symmetric chip/interconnect layout enable multi-chip integration, matched parasitics and dynamic current sharing. Thermal simulation gives $R_{th,jc} = 0.116$ K/W for GaN HEMTs and 0.17 K/W for SiC MOSFETs; double-pulse tests at 400 V/140 A verify all four bridge arms.

1. Hybrid Device Allocation

- 1200V SiC MOSFET Arrangement : They bear full 800V DC bus voltage in off-state. High voltage endurance and strong thermal robustness support long-term high-power operation with sufficient safety margin.
- 650V GaN HEMT Arrangement : Only 400V voltage stress matches GaN rating. Ultra-low gate charge and zero reverse recovery charge cut high-frequency switching loss and voltage oscillation.

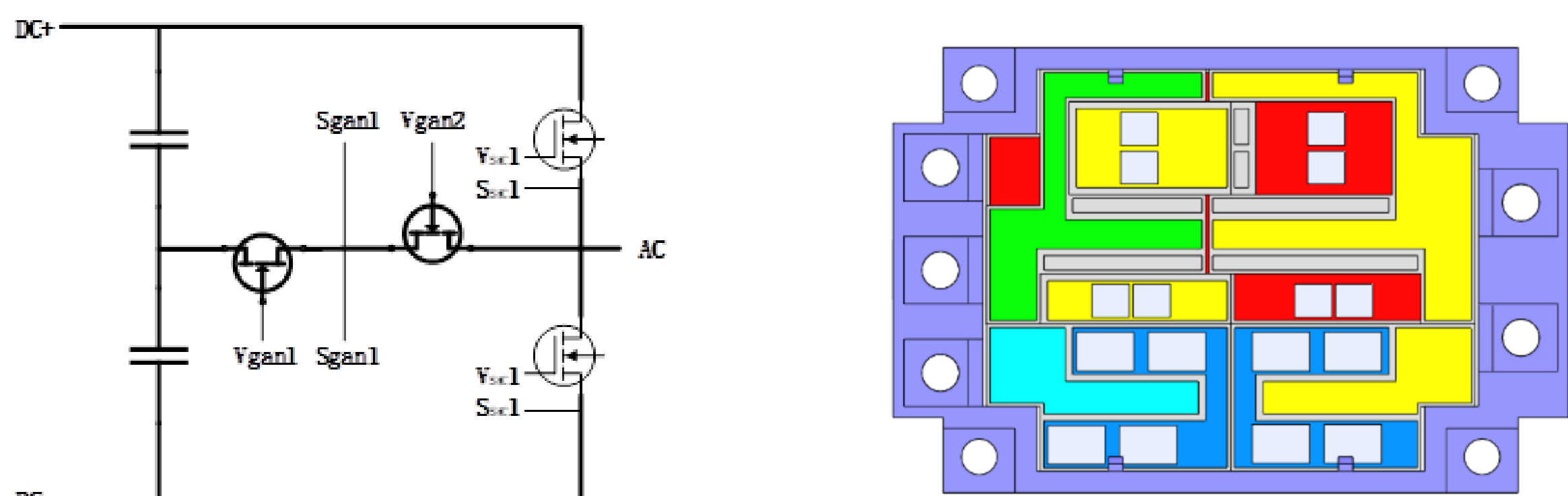


Fig. 1 T-type hybrid circuit and Fig. 2 symmetric DBC layout

2. Symmetric DBC & Packaging

- Modular substrate:** Laminated DBC sub-units control solder-interface area, warpage and residual stress while allowing scalable current rating.
- Matched parasitics:** Mirrored chip placement and equal gate/power paths align loop, gate and common-source inductances across parallel branches; tightly coupled returns reduce commutation-loop area.
- Nine-step process:** Stacked-DBC preparation, die attach, wire bonding, electrical screening, baseplate attachment, housing adhesion, terminal soldering, silicone-gel potting and performance verification support repeatable heterogeneous integration.

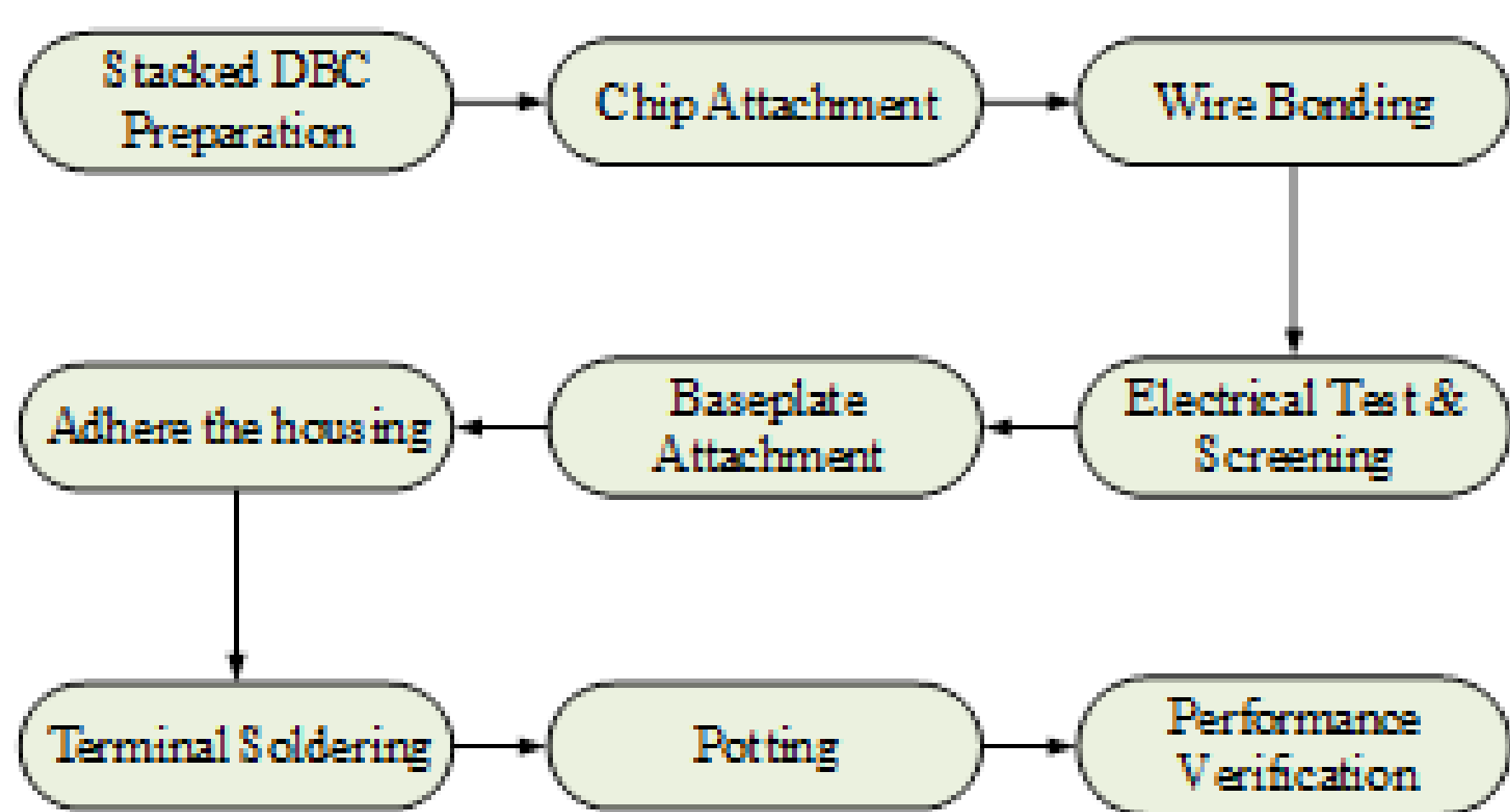


Fig. 3 Nine-step packaging process flow

3. Packaging Advantages

- Manufacturability & Scalability:** Modular split DBC design effectively reduces large-area soldering deformation risk, improves solder layer thickness uniformity and mass production yield. Different numbers of parallel chips can be configured on sub-DBC units flexibly, supporting power module current rating scaling from medium to high power EV drive applications.
- Low-Inductance Electrical Performance:** Perfect mirror symmetric layout unifies parasitic inductance of all parallel power and gate loops, restraining current imbalance, voltage spike and high-frequency oscillation during GaN fast switching. Stacked DBC compactly folds commutation current paths to minimize loop area, which is the core solution to address GaN's high di/dt parasitic sensitivity.
- Diversified Thermal Optimization Scheme:** Two ceramic DBC material solutions are reserved for different application scenarios: low-cost Al_2O_3 for prototype verification and high-thermal-conductivity AlN for high-power-density commercial products, realizing gradient thermal resistance optimization to match continuous overload operating conditions of electric vehicle inverters.
- Heterogeneous Device Compatibility:** The full packaging process chain takes differentiated process demands of SiC and GaN chips into full consideration, avoiding excessive parasitic mismatch and thermal stress differences between two types of wide bandgap devices, which greatly improves the long-term operation reliability of hybrid power modules.

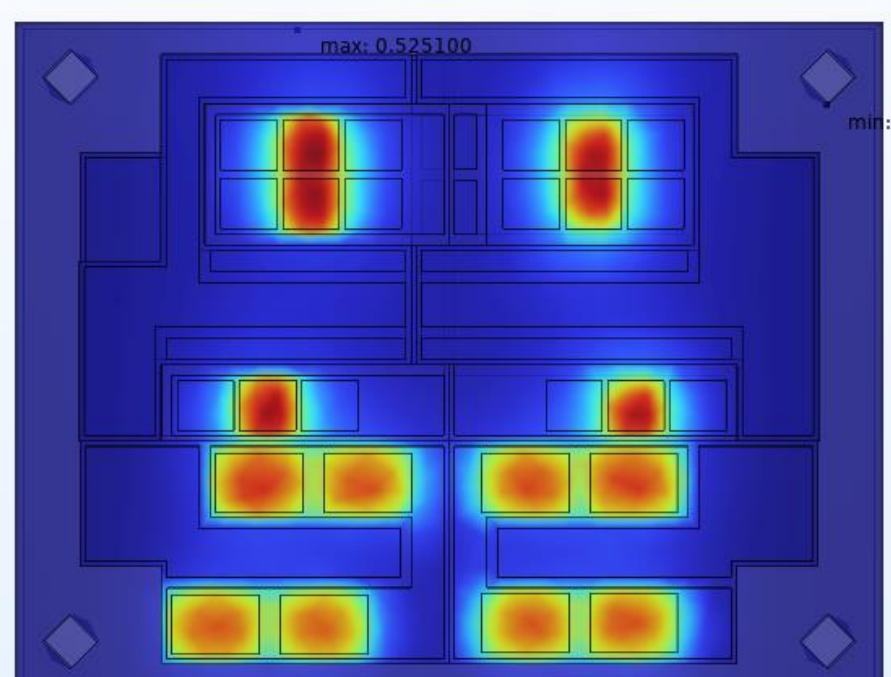


Fig. 4 Diagram of the packaged module and Fig. 5 steady-state thermal map

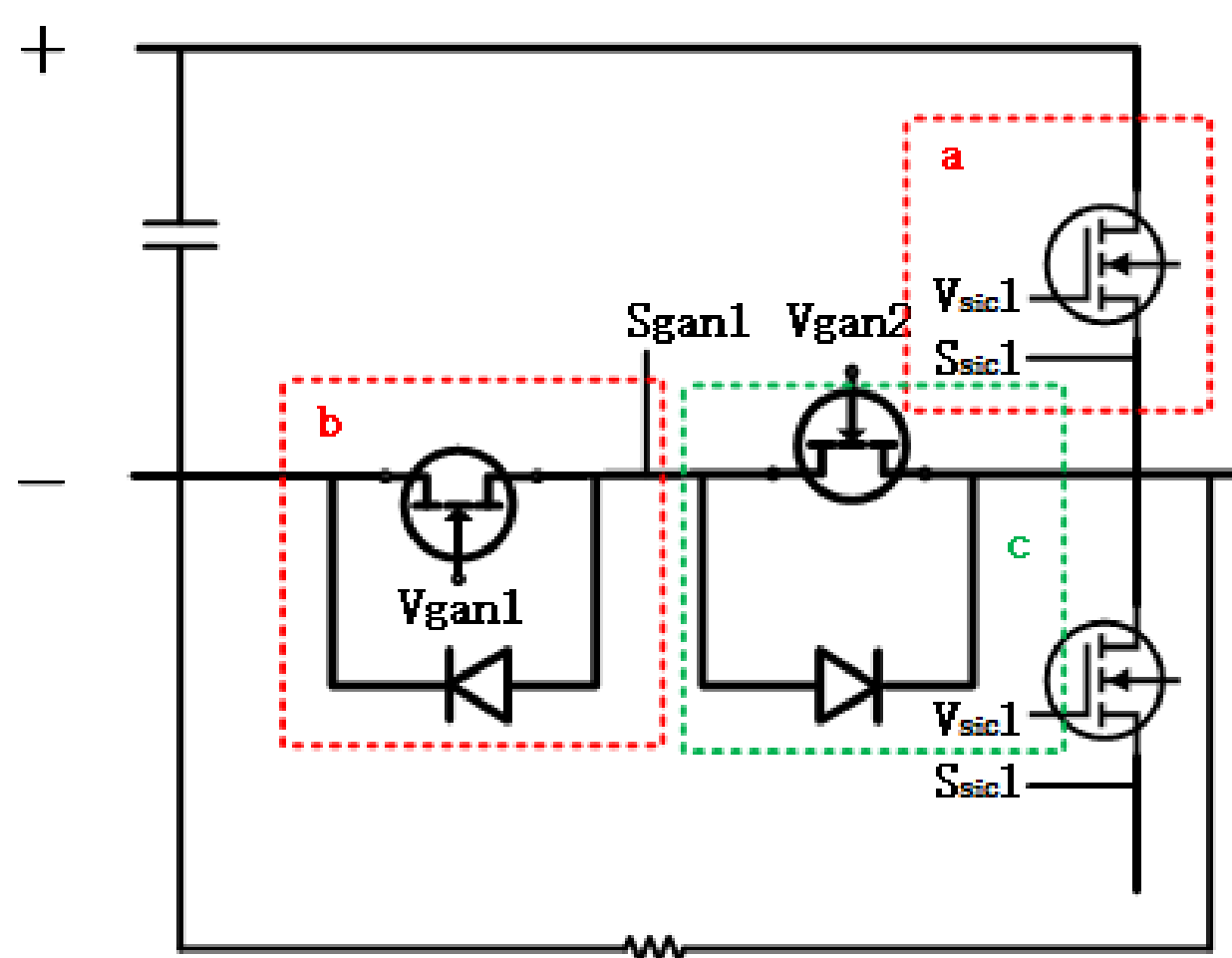
4. Thermal Simulation Analysis

3D steady-state thermal models are built in ANSYS Icepak matching the real laminated DBC packaging structure. Symmetric heat paths achieve uniform chip temperature distribution. GaN junction rise is 85°C, SiC reaches 92°C, both below 175°C limit. Extracted thermal resistance: 0.116 K/W for GaN, 0.17 K/W for SiC.

5. Experimental Verification

Double-pulse test (DPT) is adopted to characterize the dynamic switching performance of the T-type hybrid module under 400 V DC-link voltage and 140 A load current. A dedicated test circuit is constructed, where each bridge arm is measured separately with complementary devices serving as freewheeling branches to simulate real operating conditions.

The measured switching loss data are summarized as: Arm a (3.7 mJ Eon / 8.5 mJ Eoff), Arm b (5.3 mJ / 4.7 mJ), Arm c (4.2 mJ / 7.8 mJ), Arm d (3.8 mJ / 8.4 mJ). The GaN neutral clamping branch achieves the lowest turn-off loss owing to near-zero reverse recovery charge. All waveforms exhibit smooth switching without severe oscillation, proving the symmetric layout effectively balances parasitic parameters among parallel branches. The test results verify that the hybrid package combines SiC's high-voltage blocking capacity and GaN's high-frequency low-loss advantages.



Bridge arm	Test conditions	Turn-on loss Eon (mj)	Turn-off loss Eoff (mj)
a	VDC=400V ,Id=140A	3.7	8.5
b		5.3	4.7
c		4.2	7.8
d		3.8	8.4

Fig. 7 Schematic diagram of the double-pulse test circuit and Fig. 8 Measured switching waveforms of the four bridge arms

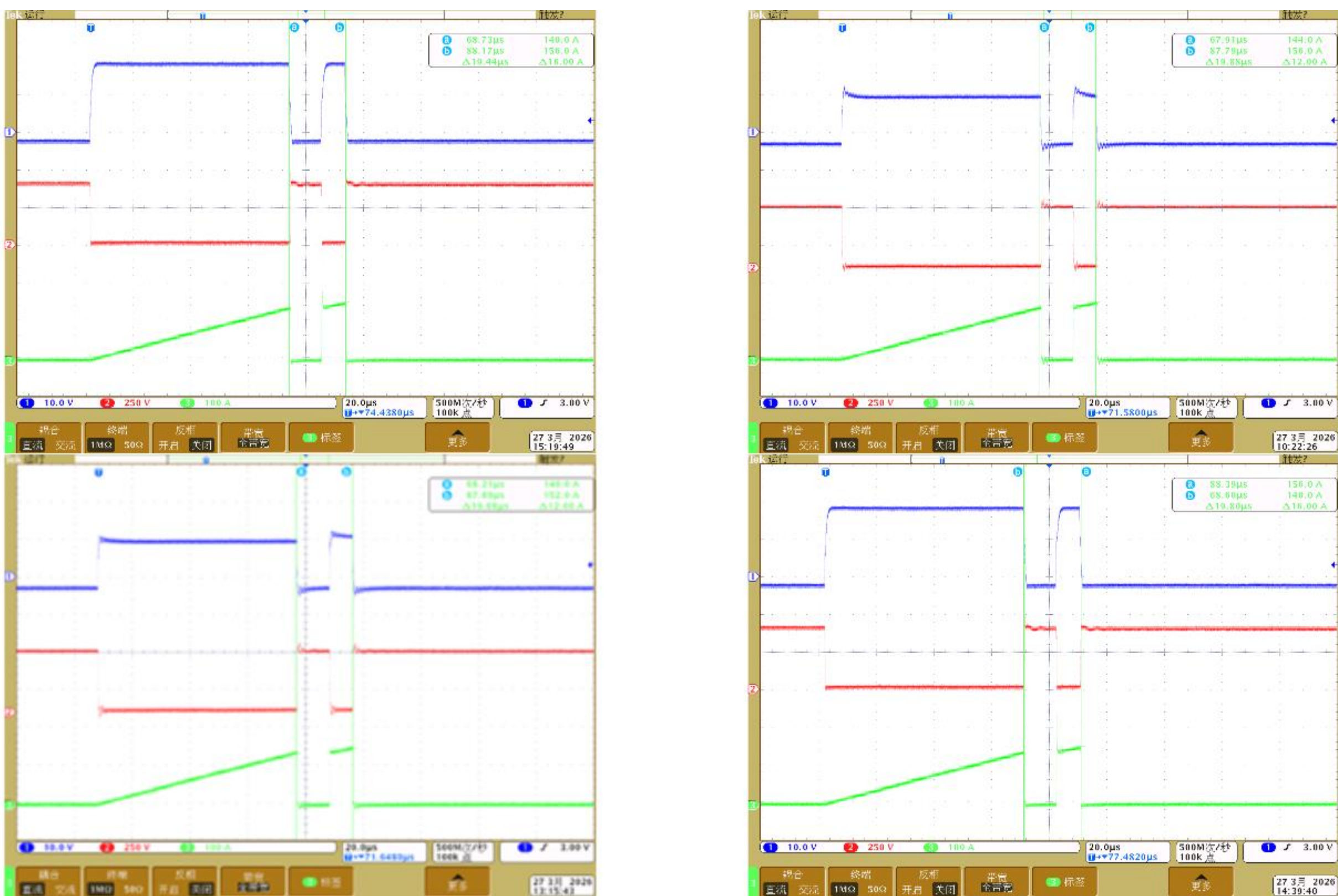


Fig. 9 Measured switching waveforms of bridge arms a-d at 400 V / 140 A

Conclusion

- A modular symmetric laminated DBC packaging is proposed for 800V EV T-type three-level GaN/SiC hybrid modules.
- Rational configuration of 1200V SiC MOSFETs and 650V GaN HEMTs achieves complementary device performance.
- Symmetrical layout and split substrate resolve four key challenges: multi-chip heterogeneous integration, dynamic current unbalance, parasitic inductance and insufficient heat dissipation.
- Thermal simulation and double-pulse experimental results fully verify the effectiveness of the proposed packaging design.
- This packaging scheme offers a practical technical route for high-voltage, high-frequency wide bandgap hybrid power converters.
- Future research will introduce AlN DBC, double-sided cooling structures and long-term power cycling reliability tests to promote industrial deployment.