

Development of a New Package Supporting Both Through-Hole and Surface-Mount Types for Fan Applications

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Introduction

- Market demand: smaller, lower-cost inverter PCBs
- Need for both surface-mount and through-hole IPM packages
- New SOIPM™/DIIPM™ achieves miniaturization while maintaining compatibility and thermal performance

Features of New SOIPM/DIIPM

The new SOIPM™/DIIPM™ integrates 6 RC-IGBTs, HVIC, and LVIC in a compact transfer-molded package. By adopting RC-IGBT technology, which combines IGBT and FWDi functions in a single chip, the chip mounting area can be reduced.

The package size is approximately **10% smaller than the conventional SOIPM** and approximately **45% smaller than SLIMDIP™**.

In addition, the same pin layout and pin pitch as the conventional SOIPM are maintained, which simplifies PCB routing. Both through-hole and surface-mount types are provided to support various assembly processes and application requirements.

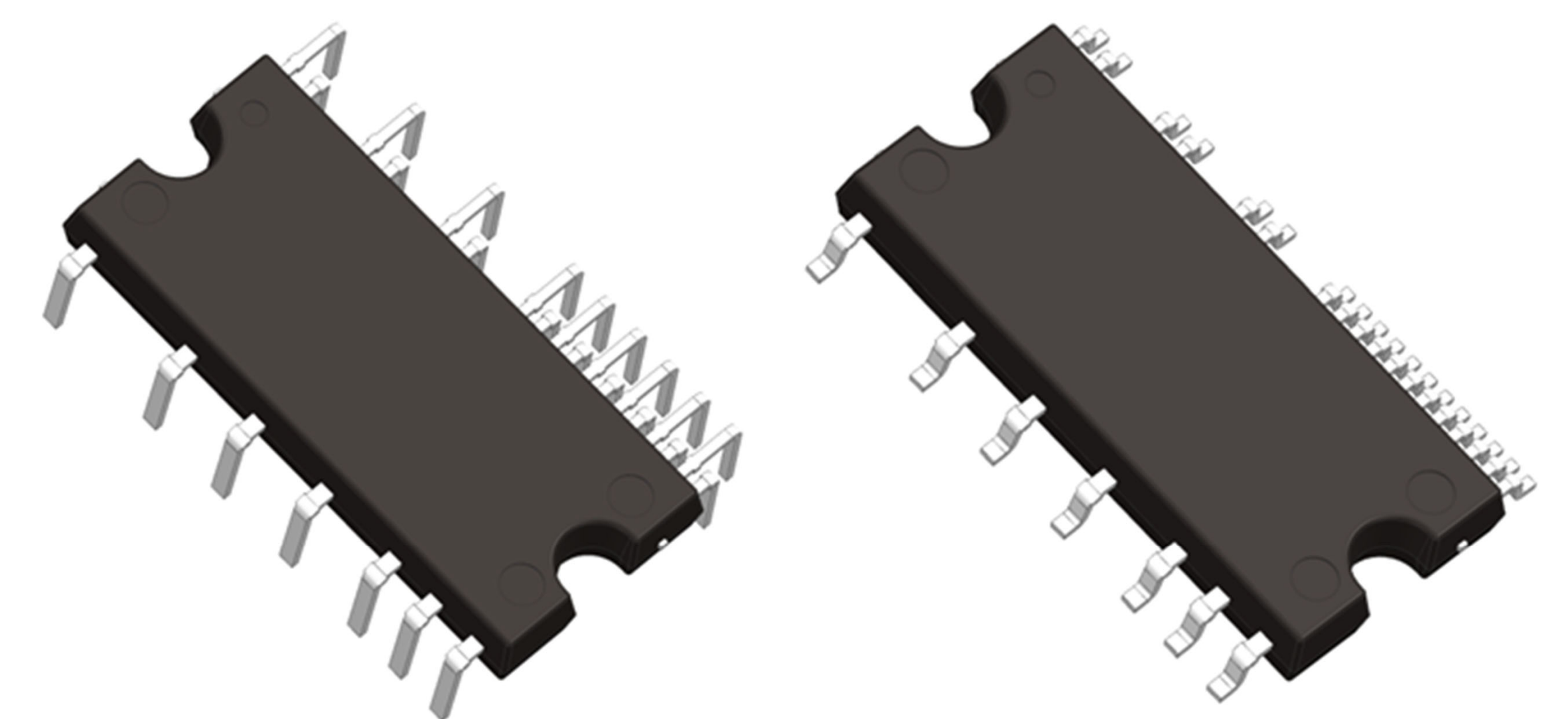


Fig. 1 Outline of New SOIPM/DIIPM

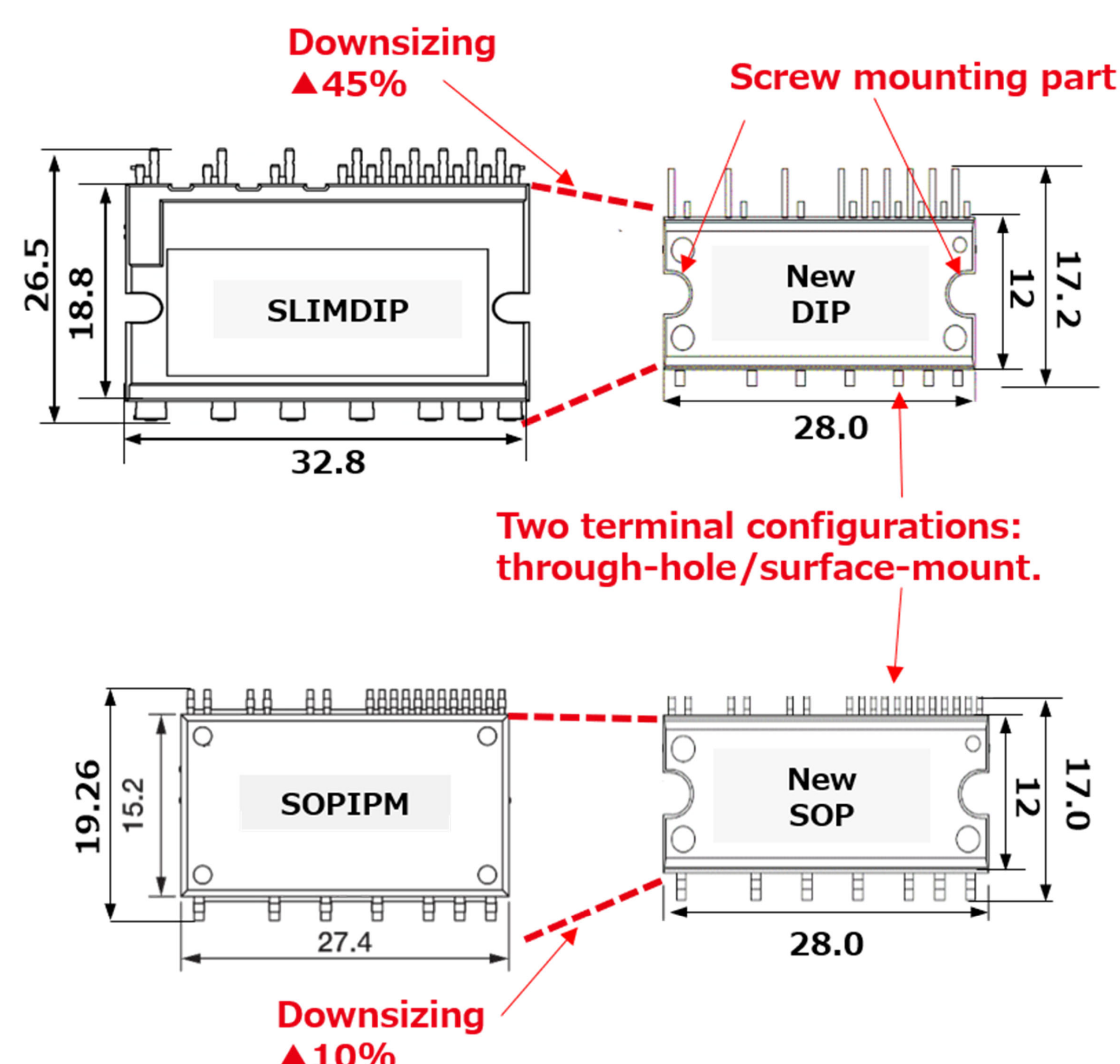


Fig. 2 Feature of New SOIPM/DIIPM Package

Melco New SOIPM	Competitor A	Competitor B

Fig. 3 Terminal layout comparison

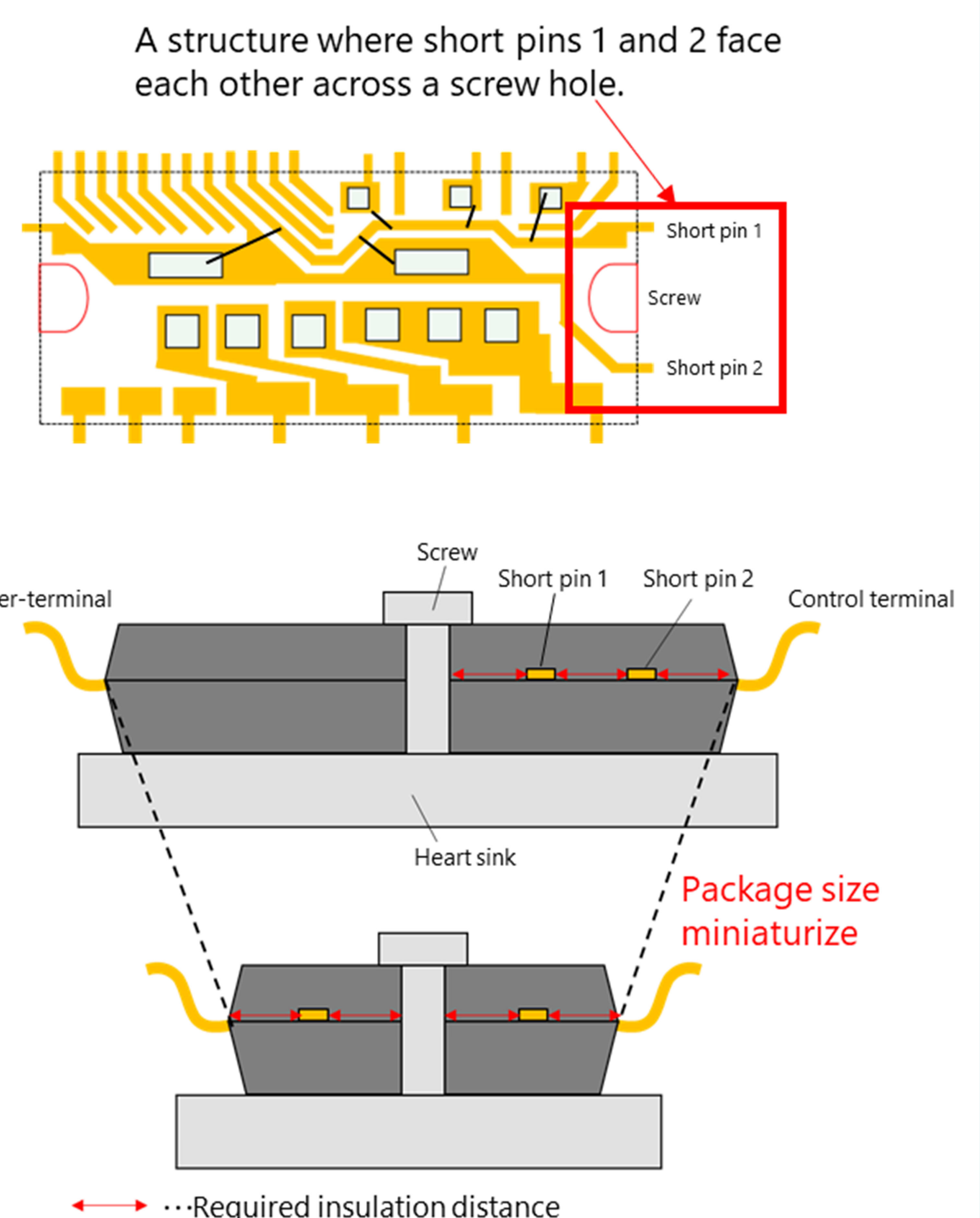


Fig. 4 Patent Pending for New SOIPM/DIIPM

Thermal Evaluation

Thermal performance was evaluated to confirm the applicability of the miniaturized package to fin-less small-capacity fan inverter systems. Since no heat sink is used in such applications, junction-to-ambient thermal resistance is an important index. The evaluation was conducted under still-air natural convection conditions using an acrylic chamber based on JEDEC standards. At $I_o = 0.3$ Arms, the 2 A-rated new SOIPM/DIIPM **showed only about a 5% increase in temperature rise despite approximately 10% package downsizing**. At $I_o = 1.0$ Arms, the 3 A-rated product reduced power loss by approximately 13% and improved temperature rise by approximately 8%.

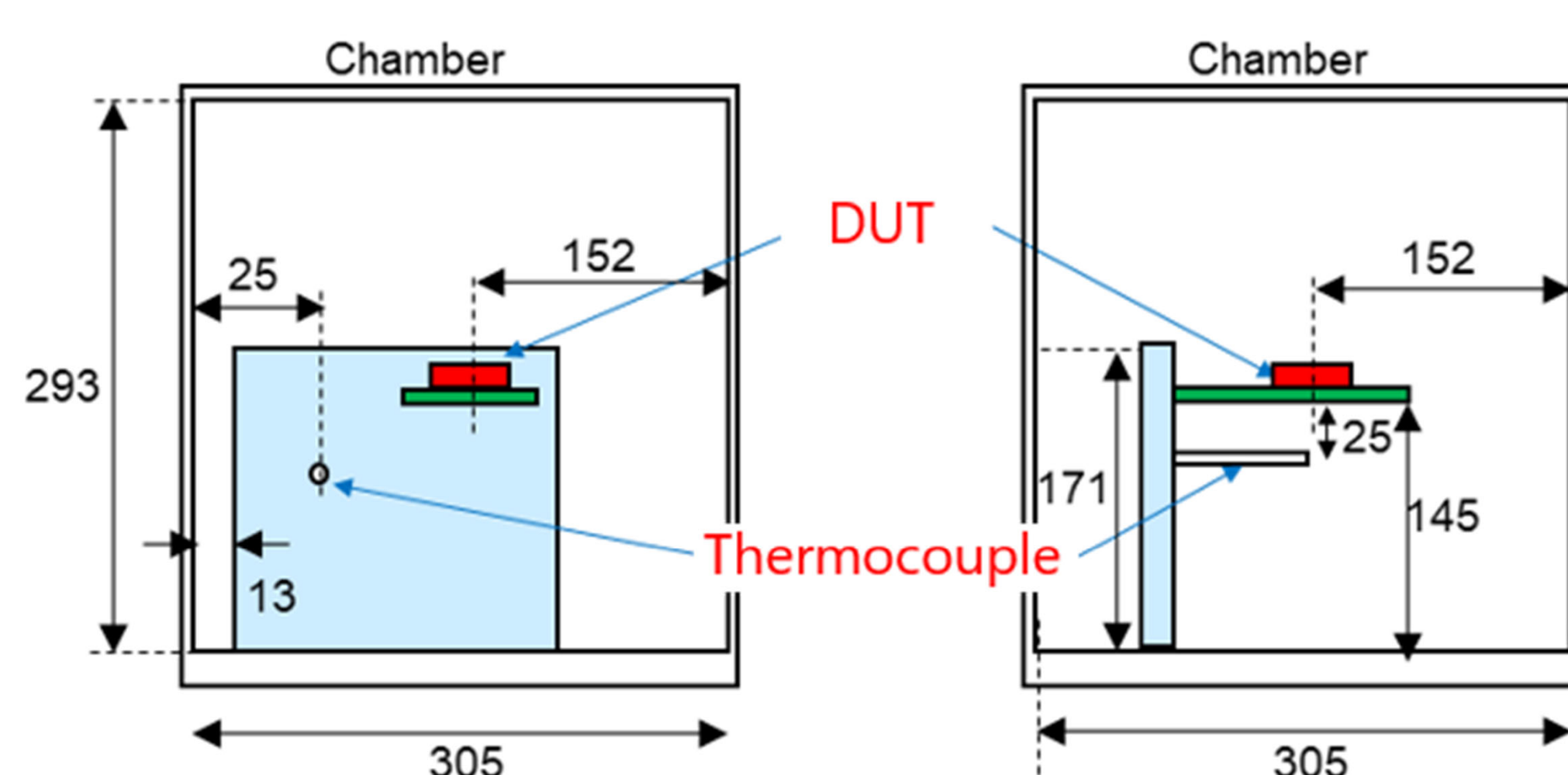


Fig. 5 Thermal evaluation chamber

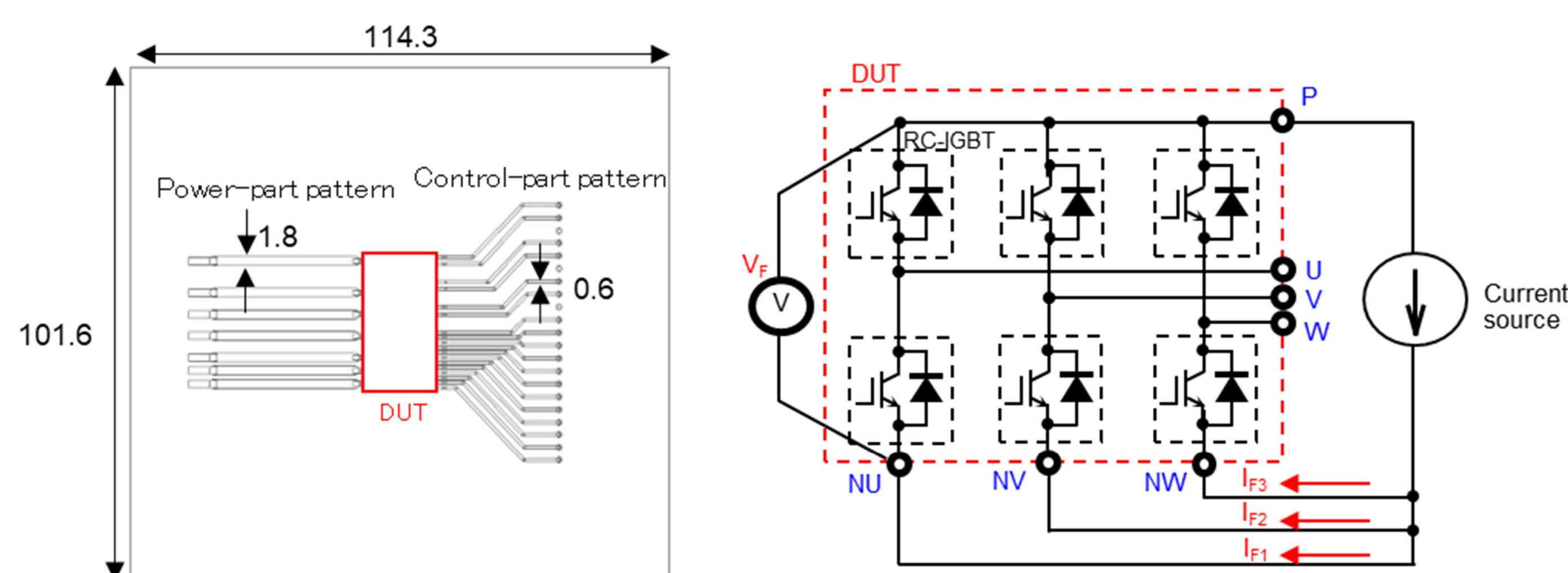


Fig. 6 Thermal evaluation board and circuit diagram

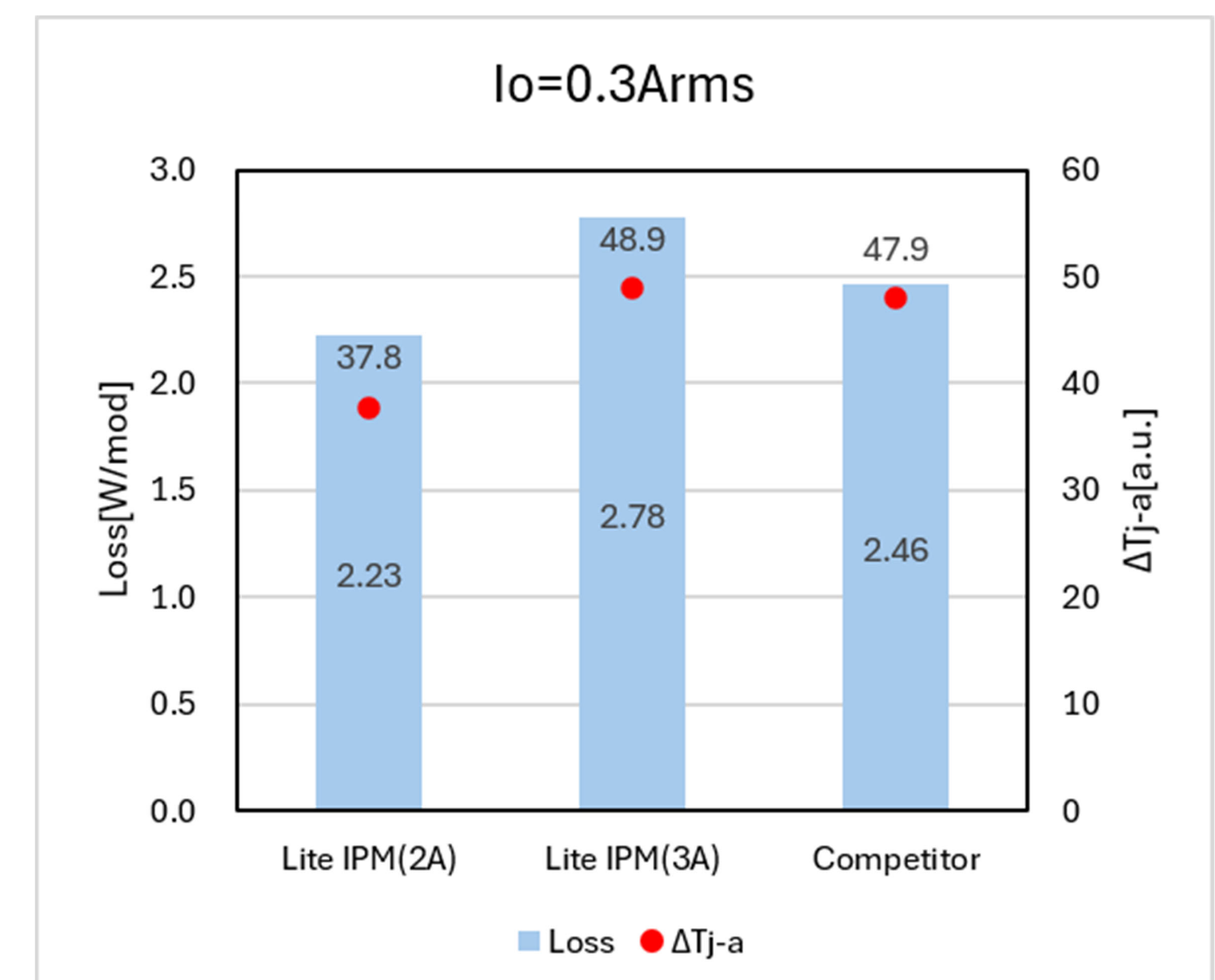


Fig. 7 Loss and temperature rising result ($I_o=0.3$ Arms)

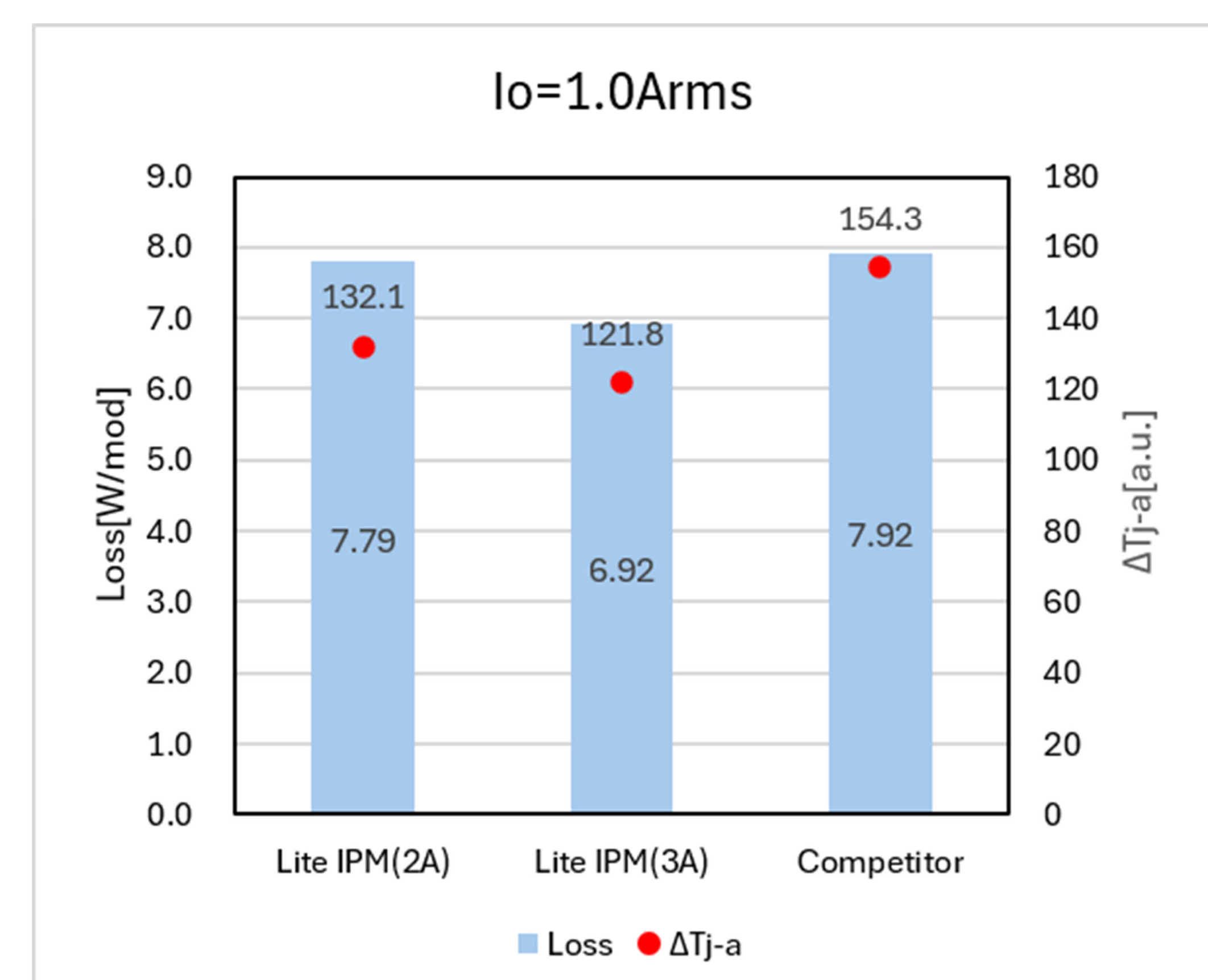


Fig. 8 Loss and temperature rising result ($I_o=1.0$ Arms)

Chip Layout Optimization

To suppress temperature rise caused by package miniaturization, the internal chip layout was optimized. In the conventional package, heat generation was concentrated on one side due to the arrangement of the power chips, which limited the effective heat dissipation area. In the new SOIPM/DIIPM, the chip placement was redesigned so that the maximum case temperature appears near the center of the package. This layout enables the entire package area to contribute more effectively to heat dissipation. As a result, **thermal concentration is reduced, temperature distribution becomes more uniform, and sufficient thermal performance is maintained even with a smaller package size**.

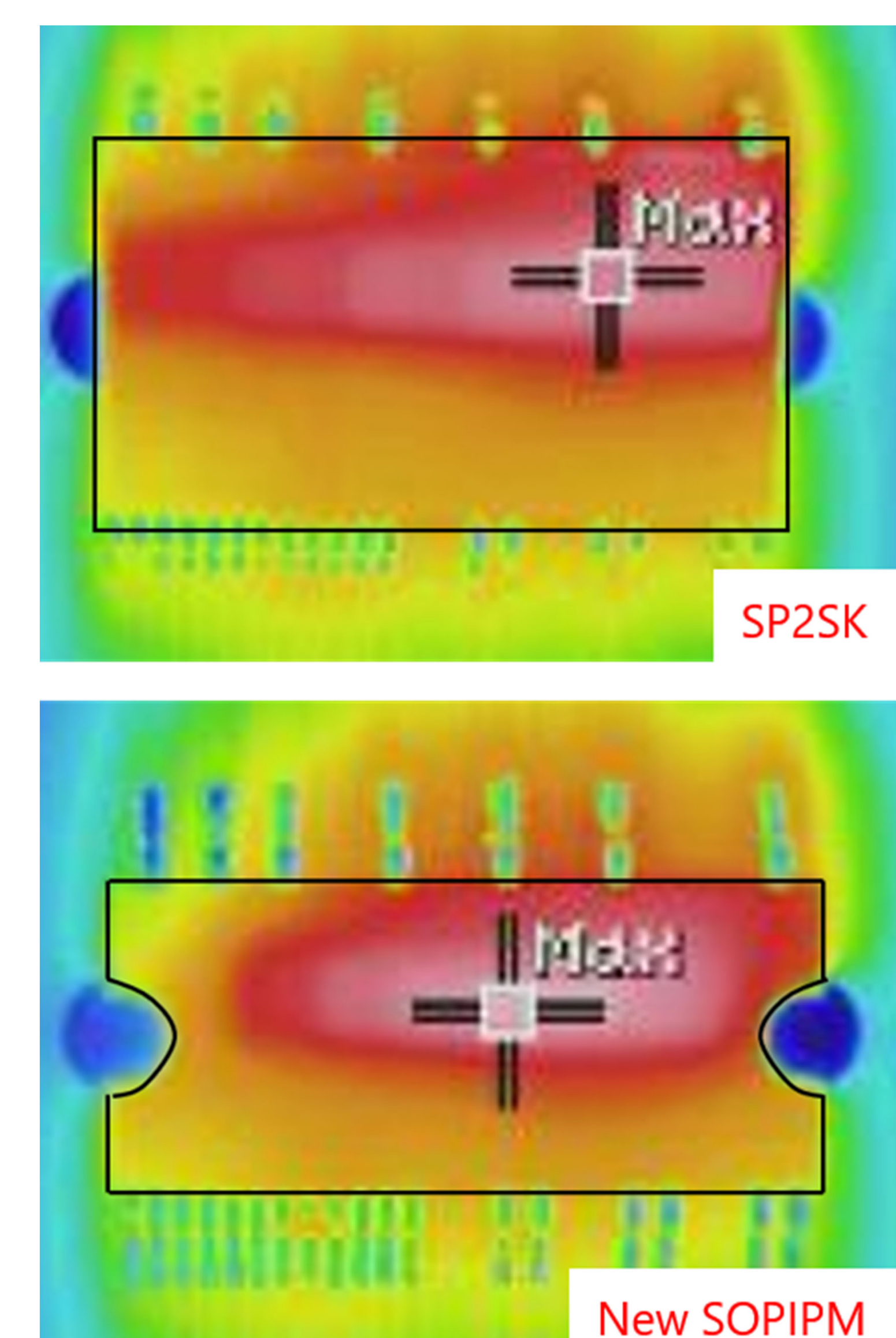


Fig. 9 Temperature distribution of the conventional SP2SK and New SOIPM

Conclusion

- The new SOIPM/DIIPM package was developed for small-capacity fan inverter applications, supporting both through-hole and surface-mount assembly.
- The package achieves approximately 10% size reduction compared with the conventional SOIPM, while maintaining the same pin layout and pitch for PCB compatibility.
- Thermal performance was maintained or improved through optimized chip selection and chip layout, enabling effective operation in both low- and high-current ranges.