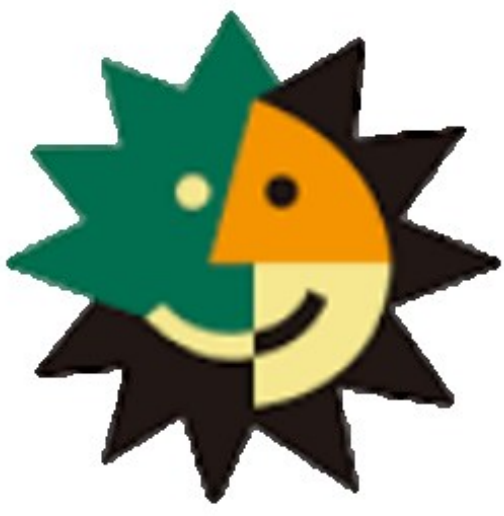




Advanced Thermal Management Solutions for Enhanced Com-compact 3D Power SiP Technologies

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Introduction

- In this work, a three-dimensional system-in-package (3D-SiP) power IC packaging approach is presented, achieving a 20% reduction in the x-y footprint while maintaining good electrical and thermal performance. By leveraging vertical component stacking, the proposed module enables a higher level of system integration within a compact form factor.
- Fig. 1(a) illustrates a conventional double-sided ball-grid-array (BGA) module, whose overall footprint is primarily determined by the PMIC die size and the number of BGA interconnects. In contrast,
- Fig. 1(b) depicts a compact 3D-SiP architecture, which consists of two substrates interconnected through a vertical interconnection scheme, enabling a higher degree of integration within a reduced package footprint.
- Fig. 1(c) illustrates the proposed enhance 3D-SiP structure, in which copper pins are incorporated to improve thermal management and support high-density I/O interconnects with reduced DC resistance.

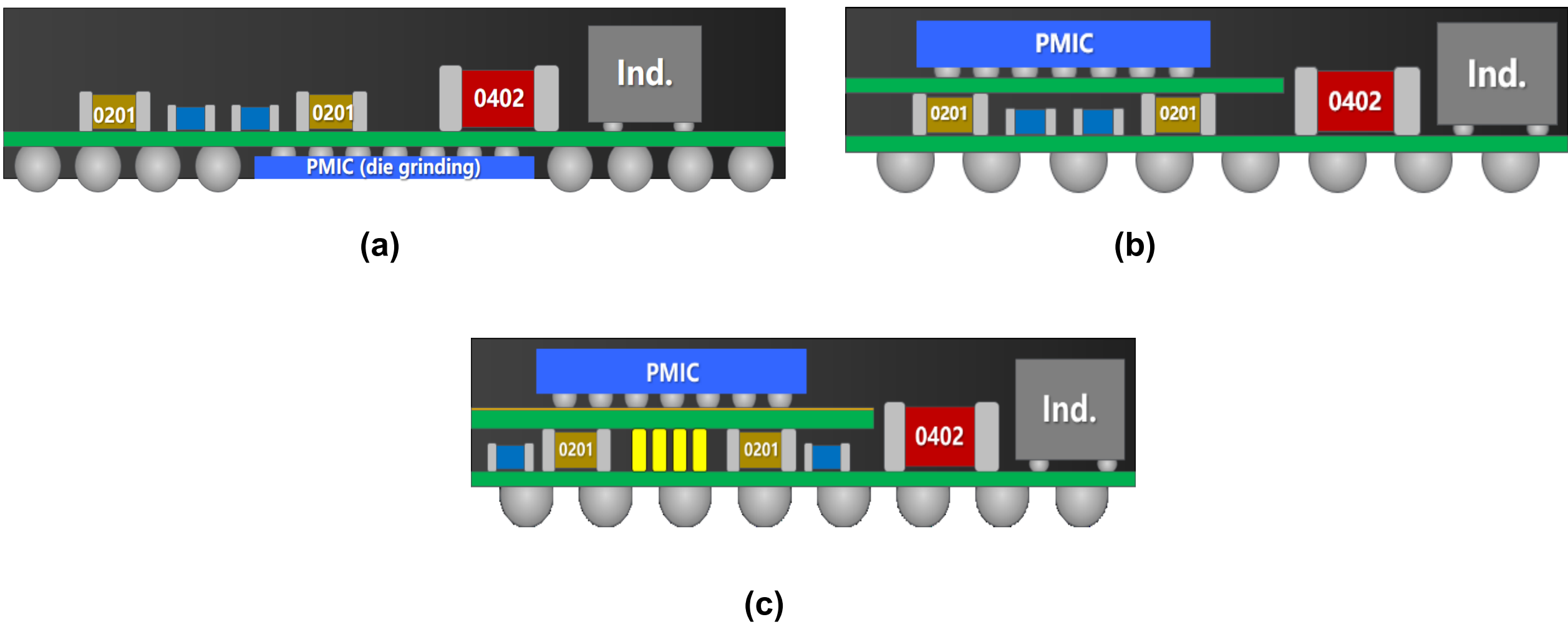


Fig. 1 PMIC Packaging (a) Conventional double-sided BGA module (b) 3D-SiP structure (c) 3D-SiP structure with copper pin interconnects

Process Flow

- The proposed 3D-SiP structure consists of two substrates, referred to as the upper PCB_A and lower PCB_B. Vertical interconnections between the two substrates are realized through a high-density integration of MLCCs and copper pins. The copper pins employed in the vertical interconnect structures have a height of 0.3 mm, a diameter of 0.09, enabling compact vertical integration while maintaining sufficient electrical and thermal connectivity between the stacked substrates.
- The total package measures 6.2 mm × 5.0 mm × 1.01 mm and incorporates a central interposer region accommodating the tallest passives (up to 0.35 mm). A 168-ball grid array with 0.4 mm pitch and 0.25 mm ball diameter ensures external connectivity. Z-axis optimization is achieved through strategic internal component layout, centered around a 2520-type power inductor (0.8 mm height), co-packaged side-by-side with the PMIC.
- An overview of the fabrication process flow and vertical integration strategy is illustrated in Fig. 3. For the upper substrate (PCB_A), the vertical interconnect components, including MLCCs and copper pins, are first mounted using standard surface-mount technology (SMT). On the lower substrate (PCB_B), the remaining passive components, including resistors, capacitors, and inductors, are assembled by SMT process.

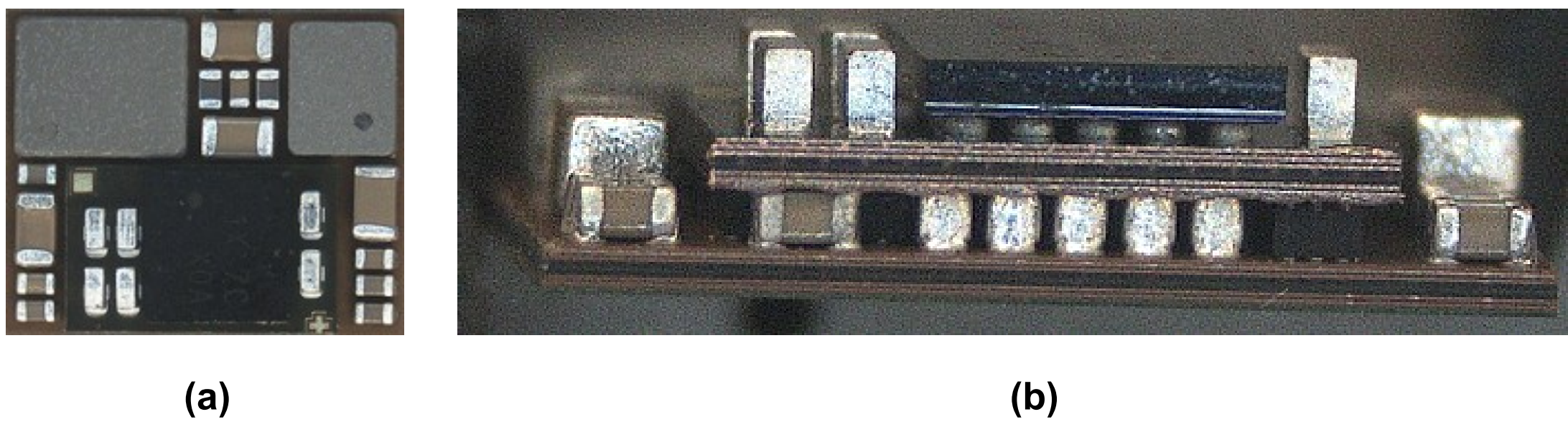


Fig. 2 (a) OM image of a 3D-SiP (b) Cross-sectional view of overall module

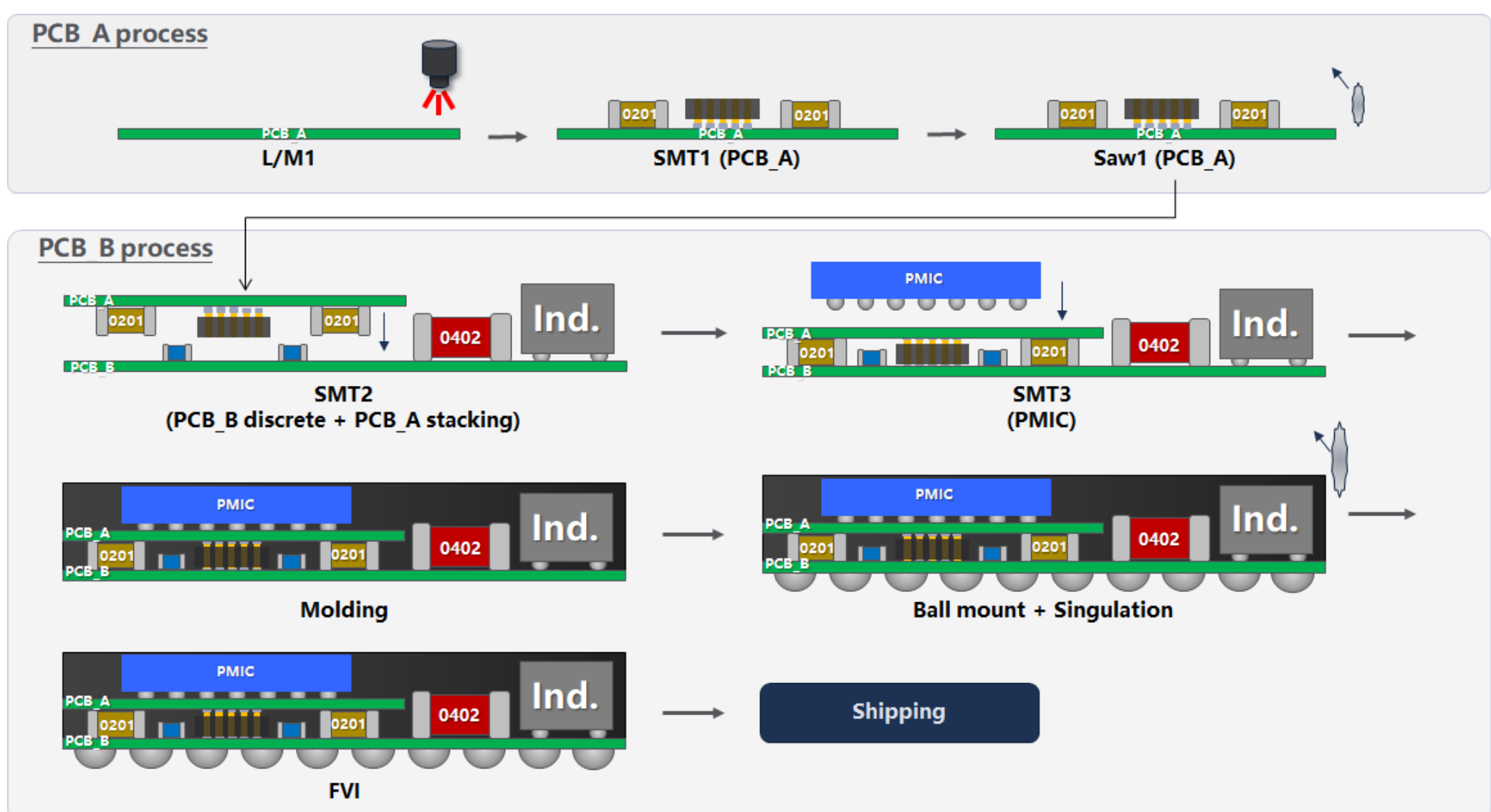
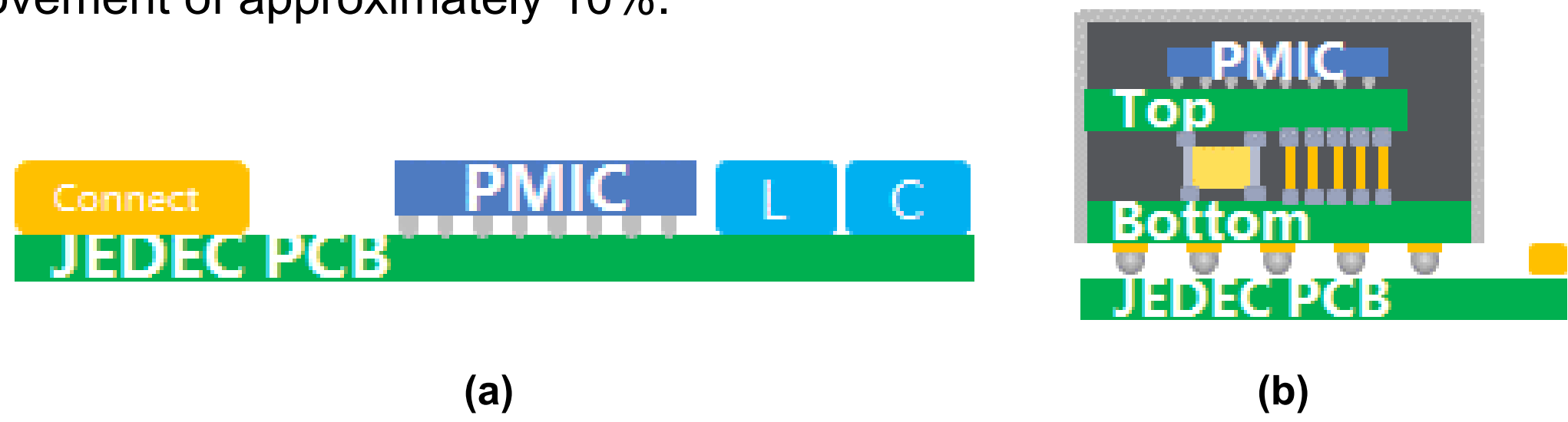


Fig. 3 Process flow of proposed 3D-SiP structure with copper pins

Thermal Performance

- In addition to electrical performance, thermal management is a critical consideration for the proposed 3D-SiP architecture due to its in-creased power density and limited heat dissipation capability. To address these challenges, optimized thermal management solutions were implemented, including optimized thermal vias and the strategic placement of copper pins to facilitate heat transfer within the package.
- To evaluate the thermal performance of the proposed design, junction-to-board thermal characterization parameter (Ψ_{JB}) simulations and measurements were conducted in accordance with the JEDEC JESD-51 standard using a JEDEC 2S2P test board. As shown in Fig. 4, two package configurations were investigated for comparison. Fig. 4(a) represents a conventional system-on-board (SoB) implementation, consisting of a WLCSP-packaged PMIC and discrete passive components mounted on the PCB without package-level integration or encapsulation. In contrast, Fig. 4(b) illustrates the proposed 3D-SiP architecture, which incorporates vertically integrated interconnect structures and dual-substrate packaging to achieve a more compact and highly integrated solution.
- Table 1 summarizes the simulated and measured Ψ_{JB} results. The measurements were conducted in accordance with the JEDEC JESD-51 standard using a Simcenter T3STER thermal characterization system. The baseline system-on-board configuration exhibited a measured Ψ_{JB} of 29.18 °C/W, whereas the pro-posed 3D-SiP architecture with thermal enhancement features achieved a measured Ψ_{JB} of 26.25 °C/W, corresponding to an improvement of approximately 10%.



		Simulation	Measurement
SoB	Ψ_{JB} (°C/W)	24.81	29.18
3D-SiP	Ψ_{JB} (°C/W)	22.42	26.25

Table 1 Thermal resistance simulation and measurement

Electrical Performance

- The proposed 3D-SiP power module employs a low-power power management integrated circuit (PMIC) that integrates one buck converter, one boost converter, and four low-dropout (LDO) regulators. The buck converter supports an input voltage range of 2.5 to 5.5 V, with an adjustable output voltage from 0.6 to 3.3 V and a maximum continuous load current of 1.2 A. The boost converter operates with an input voltage range of 2.5 to 4.4 V, provides an output voltage of 4.5 to 5.5 V, and supports a maximum continuous load current of 1.0 A. Each of the four LDO channels accepts input voltages from 1.9 to 5.5 V, delivers output voltages ranging from 0.6 to 3.775 V, and supports a maximum continuous load current of 0.3 A.
- To evaluate the output voltage regulation and power conversion efficiency, the SoB, 3D-SiP, and 3D-SiP with copper pin structures were individually mounted on the test PCB shown as Fig. 6. The resistance of the test PCB was measured using an Resistance Meter. After compensating for the test PCB resistance, the actual output voltages (V_{out}) of the different package structures were obtained. Fig.8 presents the efficiency measurement results of the Buck and Boost converters, showing less than 1% difference compared to the PMIC.
- Table 2 lists the resistance values of each path, where the discrepancy between simulation and measurement is below 10%. Excluding the inductor's internal resistance, the packaging resistance of the 3D-SiP is less than 20 mΩ.

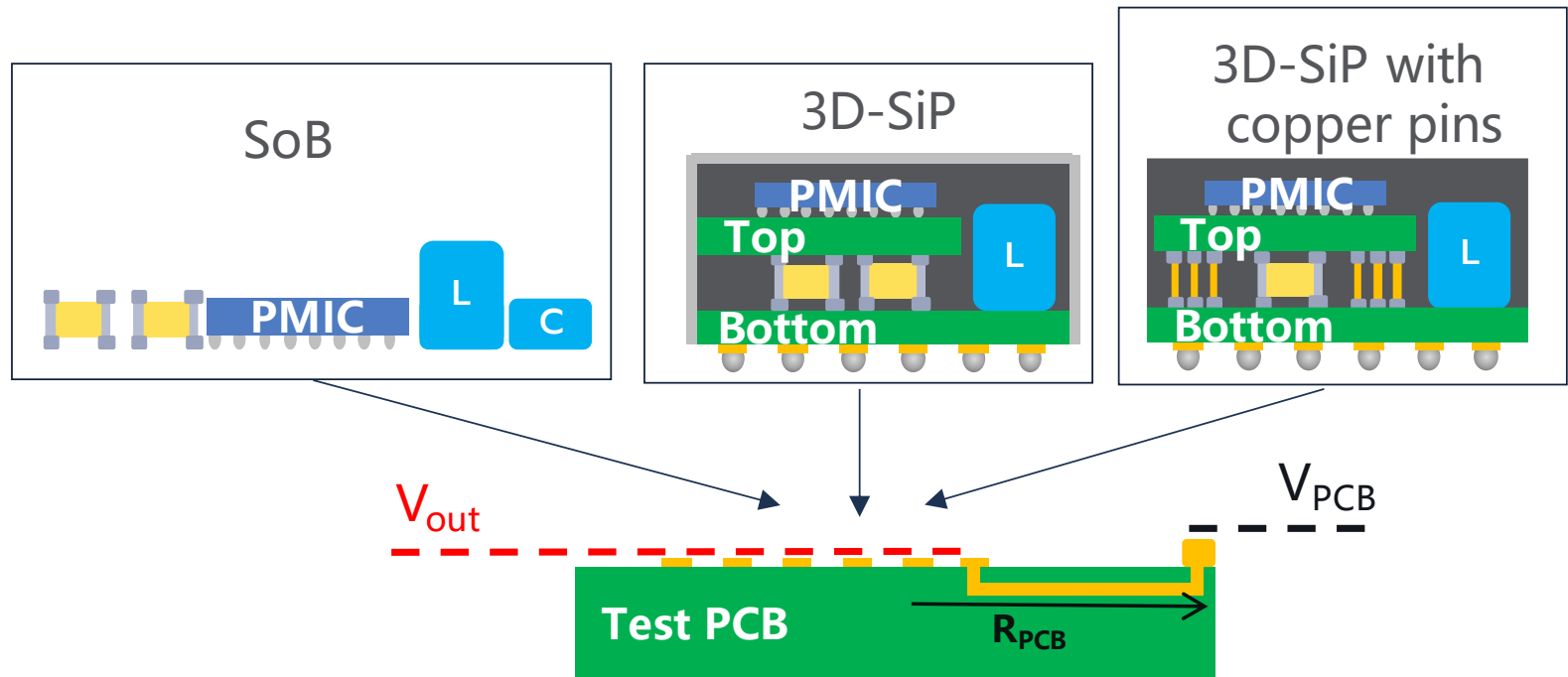


Fig. 6 Modules on test EVB illustration

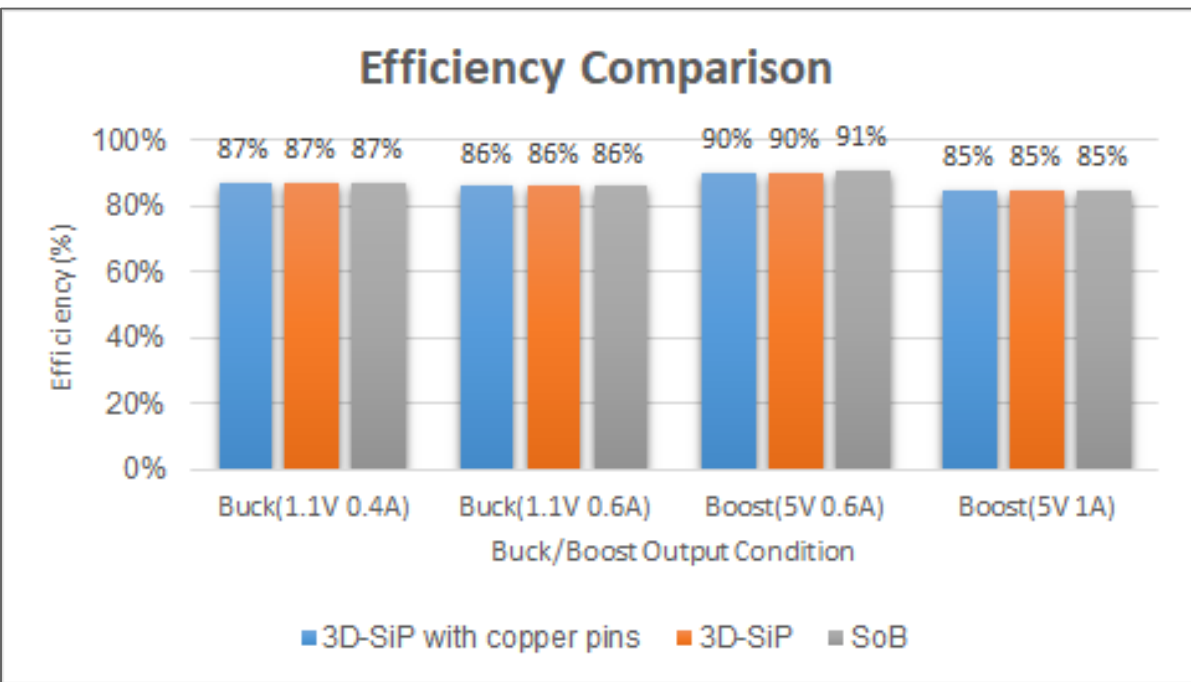


Fig. 8 Measured results of Buck/boost power conversion efficiency

	3D-SiP		3D-SiP with Copper Pins	
Net	Meas. (mΩ)	Sim. (mΩ)	Meas. (mΩ)	Sim. (mΩ)
Buck	9.02+R _L	10.33+R _L	5.01+R _L	4.89+R _L
BST	11.41	10.27	11.52	10.79
LDO1	14.07	12.7	10.01	10.83
LDO2	12.95	11.7	6.11	6.2
LDO3	12.53	11.79	8.97	7.76
LDO4	16.98	15.48	10.66	9.84

Table 2 Simulated and measured 3D-SiP packaging DC resistance