

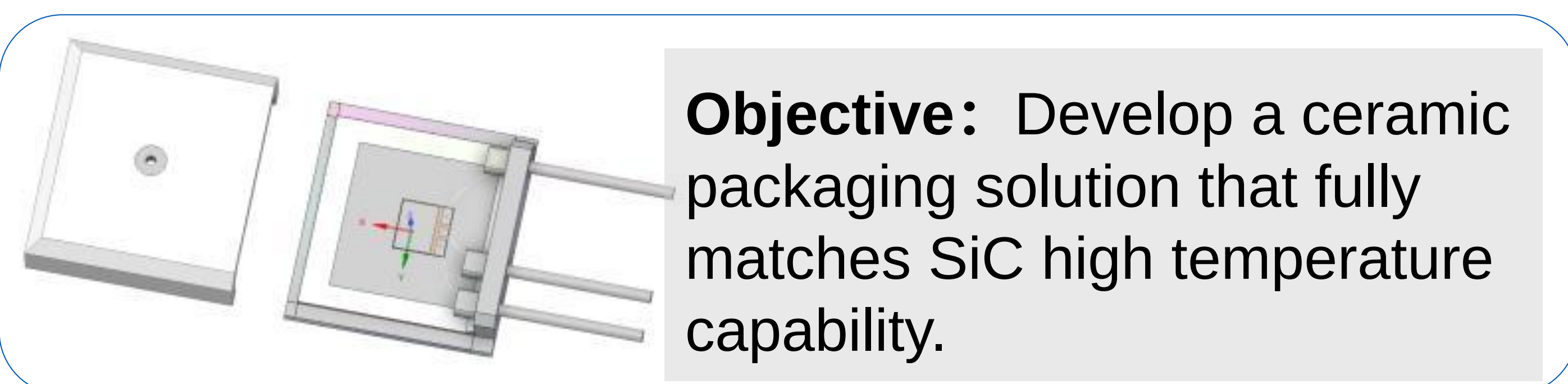
Ceramic Packaging Technology for 250°C Medium/High-Voltage Silicon Carbide Power Electronic Devices

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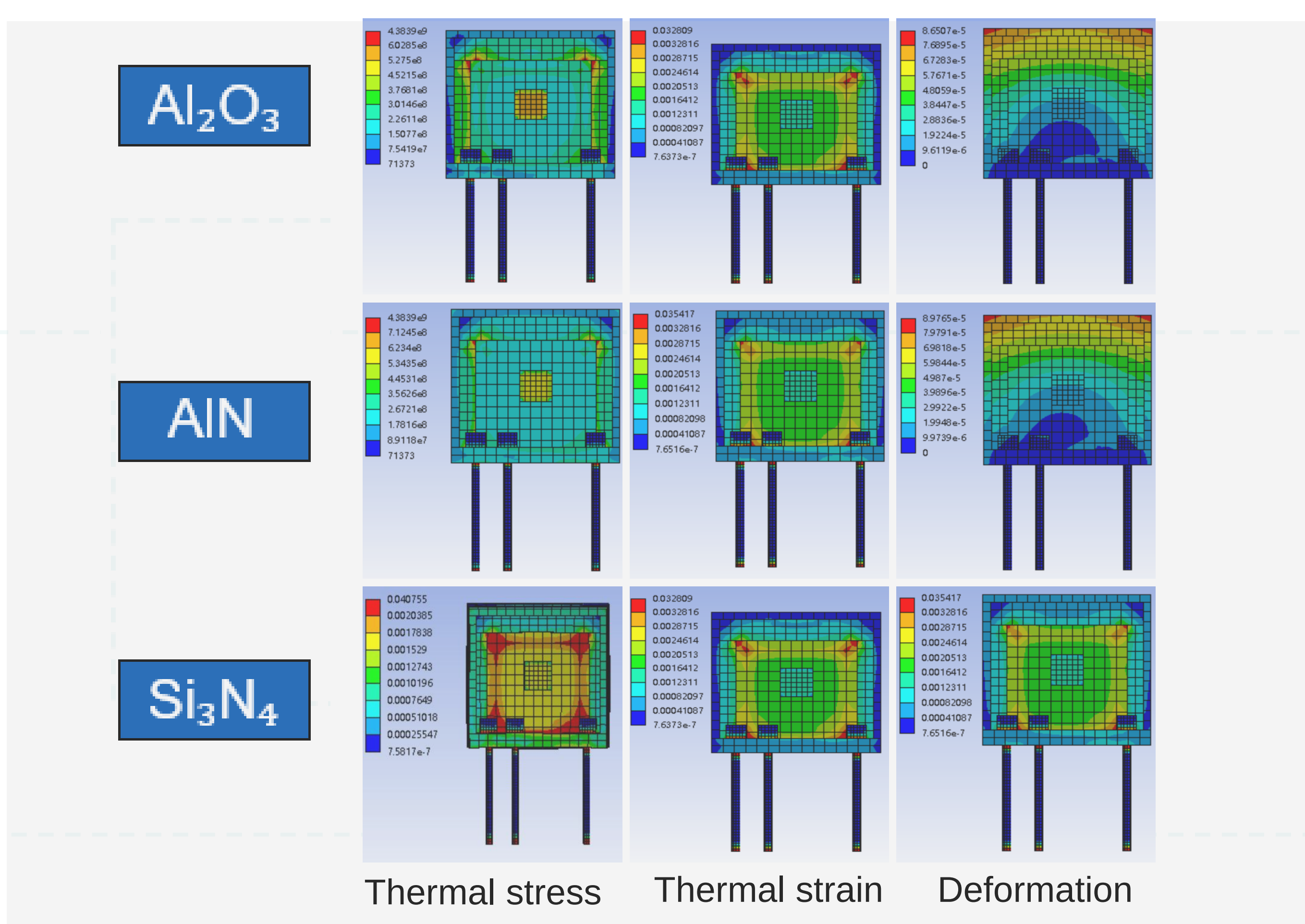
Introduction

Silicon carbide (SiC) power devices are constrained by conventional silicon packaging technologies rated below 175 °C, limiting their high-temperature capabilities. This work develops a high-temperature ceramic packaging solution through systematic electro-thermo-mechanical simulation, which identifies Si₃N₄ as the optimal housing material due to its excellent coefficient of thermal expansion match with SiC. A prototype is fabricated using nano-silver sintering for die attachment, and experimental validation confirms stable operation at 250 °C. This solution effectively unlocks the full high-temperature and high-voltage potential of SiC technology, providing a viable pathway for next-generation wide-bandgap power modules.

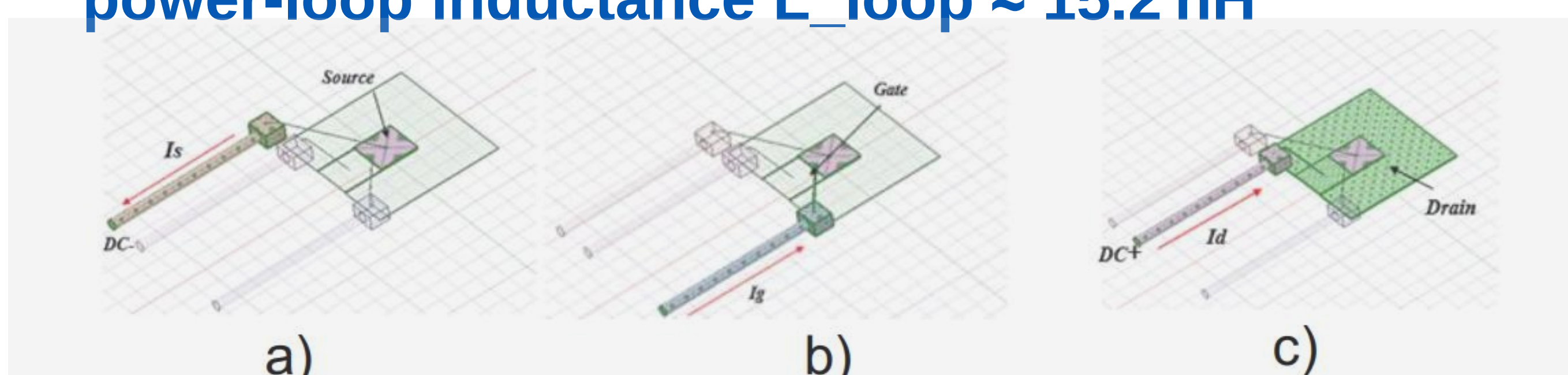
Simulation-driven method



Material Selection via Thermo-Mechanical Simulation



Parasitic extraction: ANSYS Q3D Extractor – total power-loop inductance L_{loop} ≈ 15.2 nH

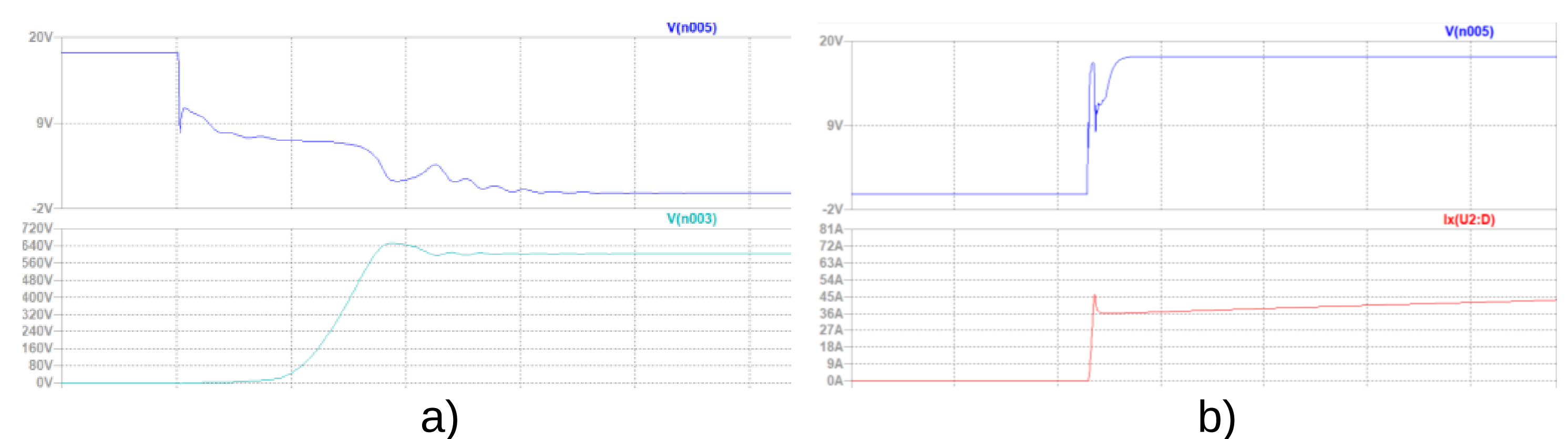


Parasitic inductance extraction using ANSYS Q3D. a) source, b) gate, and c) drain current paths

Conclusion

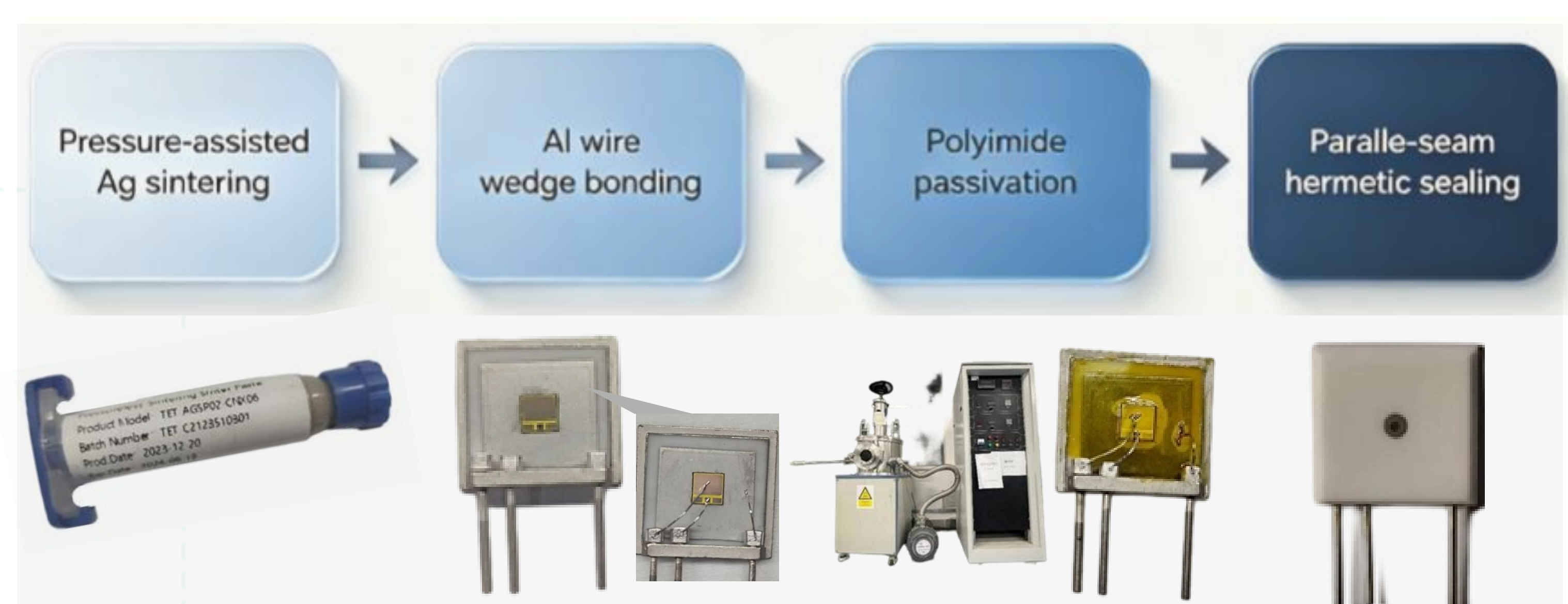
- Si₃N₄ ceramic provides the best CTE match ($\Delta\alpha \approx 1.4$ ppm/K) and highest strength, reducing interface stress by 38 %.
- The prototype operates continuously at 250 °C with no degradation – fully unlocks SiC's high-temperature potential.

Dynamic simulation: LTspice double-pulse test (DPT) at 600 V / 20 A.



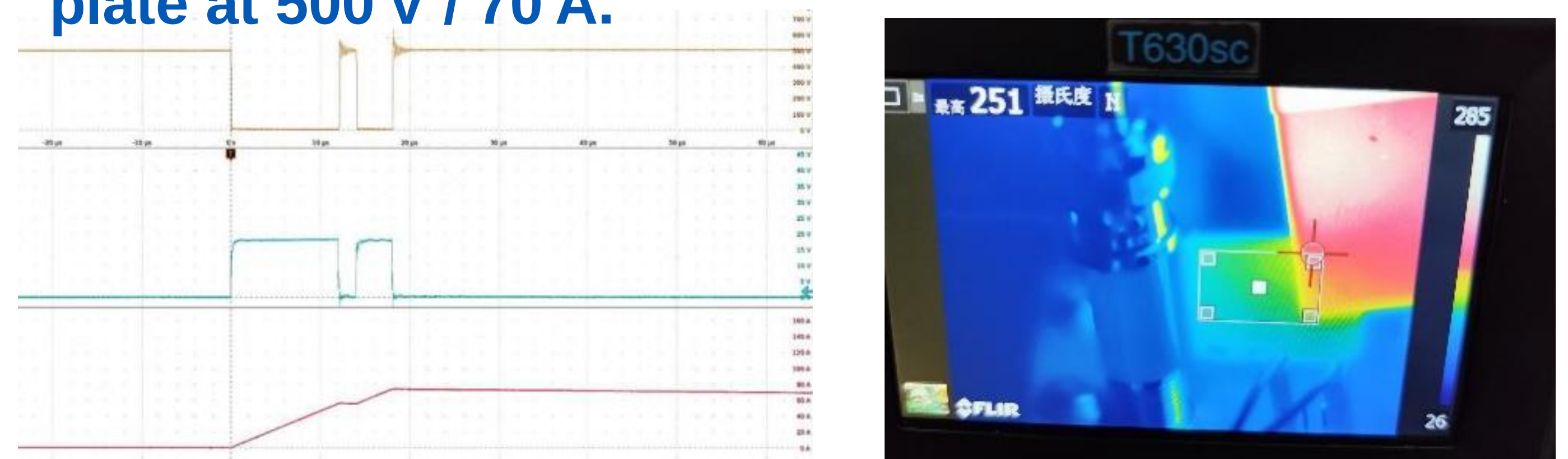
LTspice simulation results of double-pulse test. a) turn-off voltage spike, b) turn-on current spike

Fabrication



Result

High-temperature DPT: Tested on a 250 °C hot plate at 500 V / 70 A.



Turn-off overshoot only **80.2 V**; extracted loop inductance **16.2 nH** (excellent match with simulation)