

Abstract:

To meet high-power-density inverter demands, this paper presents an electro-thermal co-design of a 1200V 6-in-1 SiC module from NEXIC. We combine experiments and simulations to extract parasitic parameters, build a thermal network, and perform coupling analysis. This determines continuous current capability and safe operating temperature. Based on measured data, we develop a lifetime prediction model under typical power cycling, yielding current-frequency-thermal resistance curves for engineering selection. Results confirm excellent dynamic current sharing and thermal management, meeting rigorous application requirements.

The 6-in-1 Power Module Characteristics:

1. Product Technical Overview

Application: BEV/HEV main inverters, 800–950 V.

Chip: Automotive-grade SiC, RDS(on) = 1.7 mΩ, AQG324.

Thermal: Pin-fin baseplate + NTC, T_{vj}(max) = 175°C.

Integration: Bolt/weld options, standardized pinout.

Outcome: High power density and reliability for next-gen e-drives.

2. Static Behavior

SiC MOSFET static characteristics: RDS(on) exhibits a strong positive temperature coefficient, roughly doubling at 175°C, and increases slightly with drain current. Output characteristics show reduced current capability at high temperature, while a higher V_{gs} (e.g., 18 V) effectively lowers RDS(on). Transfer characteristics have a negative transconductance temperature coefficient, reducing current drive at elevated temperatures. The body diode's forward voltage decreases with temperature, lowering reverse conduction loss but demanding careful parallel design to prevent current hogging. These parameters are fundamental for power loss calculation, thermal design, and reliable operation.

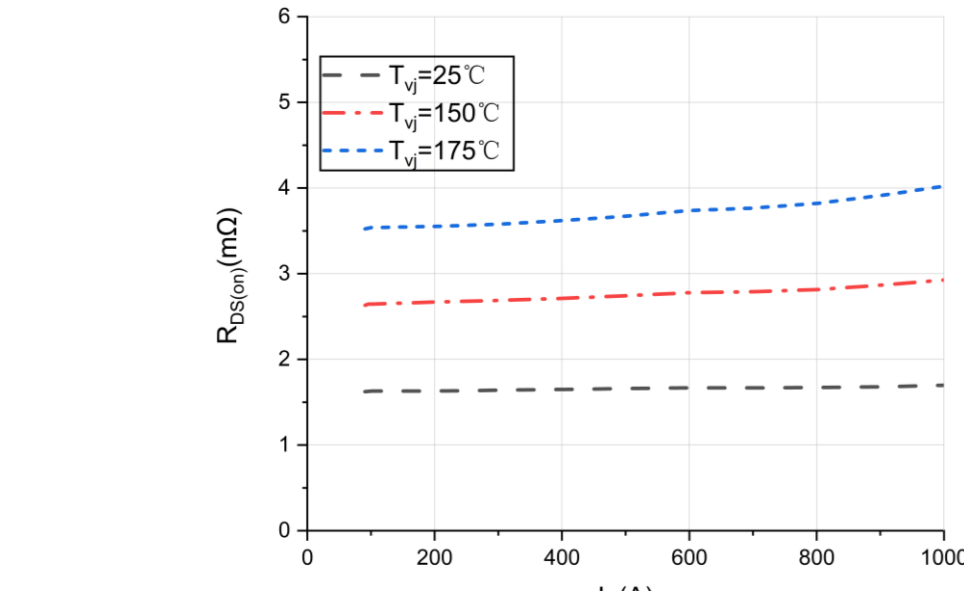


Fig.2 The influence of T_j and I_D on RDS(on)

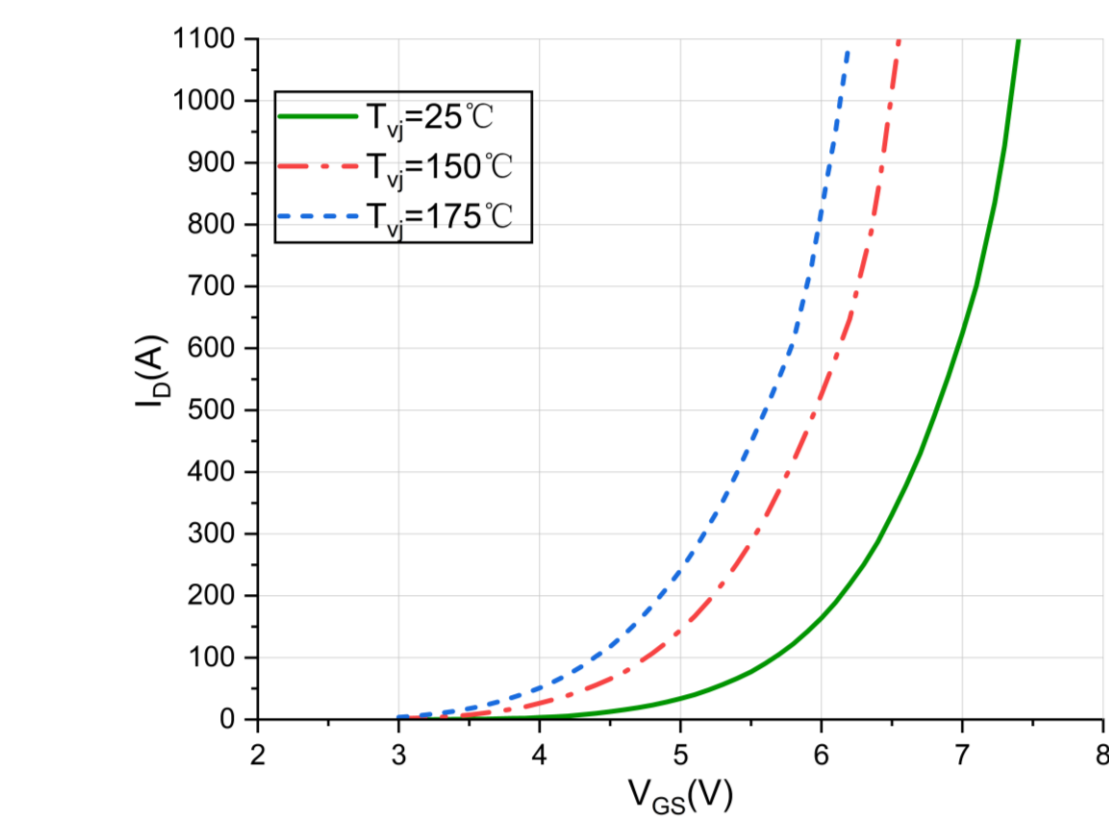


Fig.4 MOSFETs' transfer characteristics

3. Dynamic Behavior

A double-pulse test platform with a thermal chamber, inductive load, and high-bandwidth probes precisely captures switching transients at 25°C and 175°C. The DUT is thermally soaked to ensure accurate junction temperature, gate drive voltage is tightly regulated, and commutation-loop parasitic inductance is minimized for high-fidelity, reproducible measurements. The captured waveforms are then analyzed to extract switching energy and evaluate its strong temperature dependence.

MOSFET switching losses—turn-on (E_{on}), turn-off (E_{off}), and body-diode reverse recovery (E_{rec})—all increase with voltage and load current and exhibit strong temperature dependence. E_{on} at 175°C can be 30–50% higher than at 25°C, driven by a reduced threshold voltage that shifts the Miller plateau. E_{off} rises moderately at high temperature, while E_{rec} is substantially larger. Consequently, total switching loss must be evaluated at maximum junction temperature to ensure accurate calculation and reliable thermal design, especially in hard-switching bridge circuits.

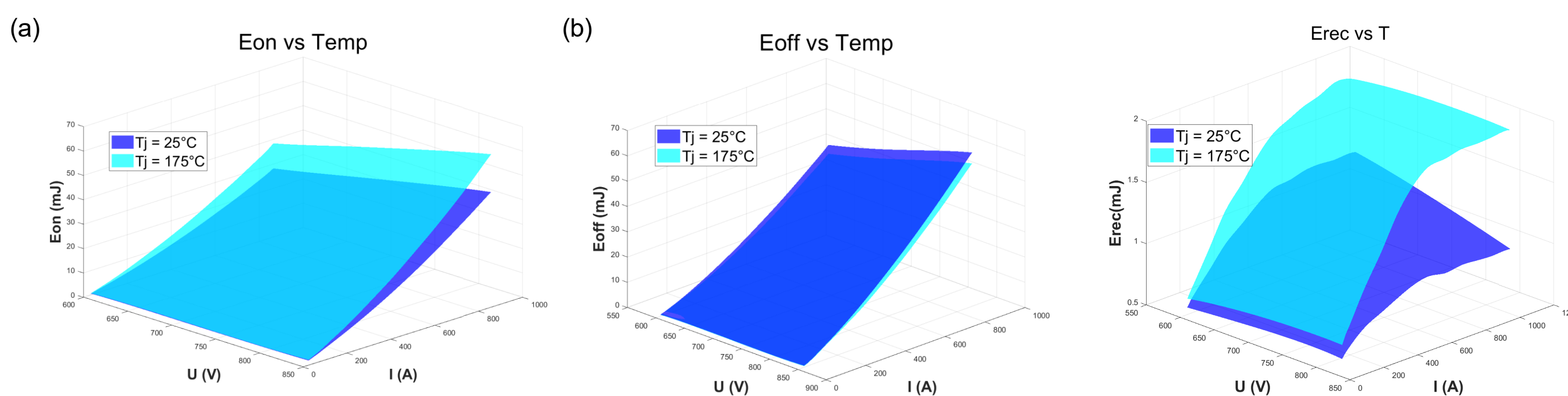


Fig.7 Switch Characteristics of NXHP

Fig.1 6-in-1 NXHP



Fig.3 MOSFETs' output characteristics

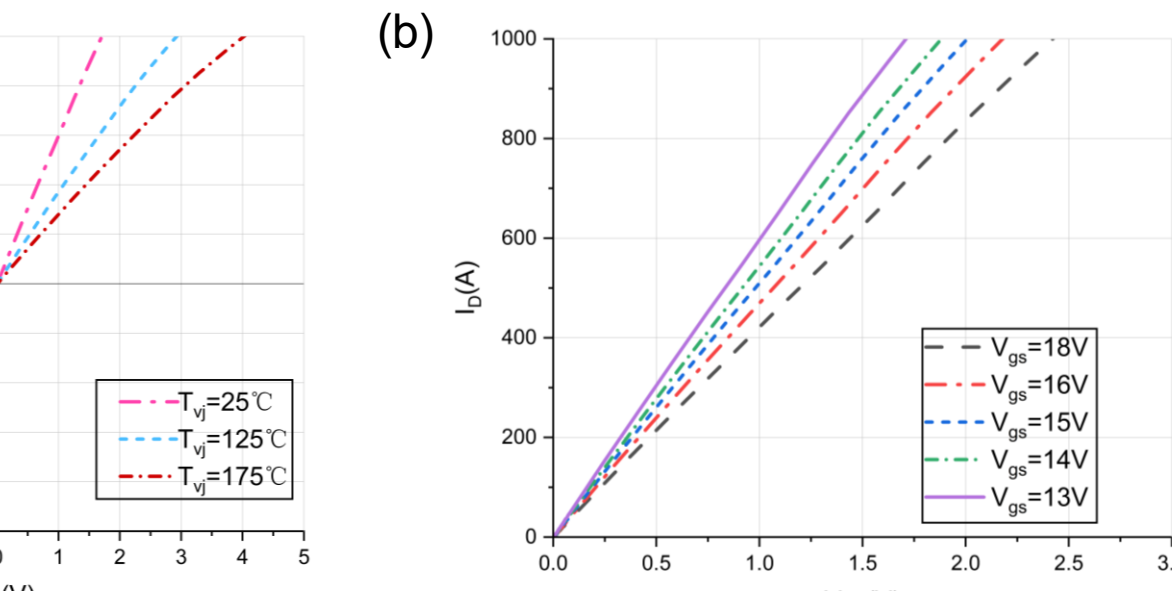


Fig.3 MOSFETs' output characteristics

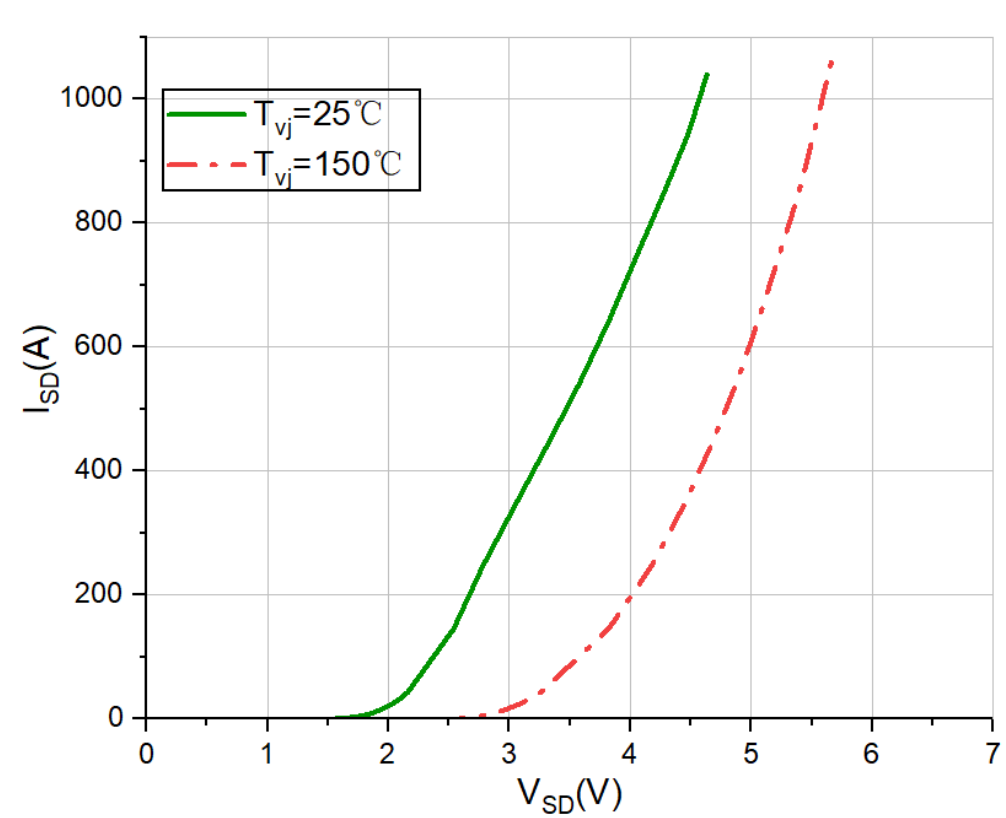


Fig.5 Body diodes' Forward characteristics

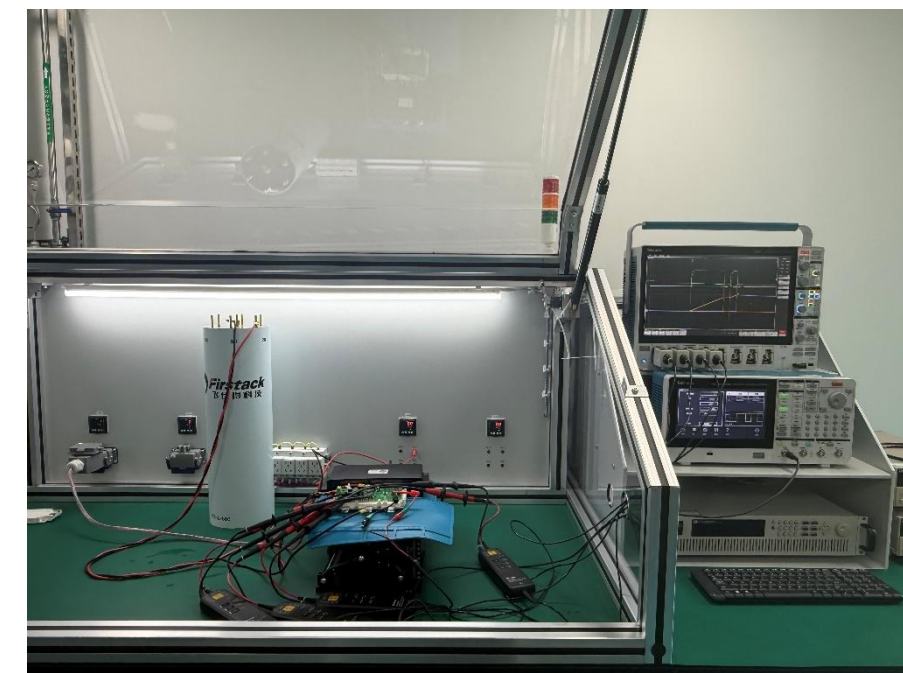


Fig.6 Experimental Test Platform

Fig.8 Erec Characteristics

4. Current Sharing Capability

Paralleling chips increases current rating, but parasitic variations cause current imbalance, degrading reliability.

$$\alpha = \frac{\sqrt{I_{d1} - \left(\sum_{i=1}^n \frac{I_{di}}{n}\right)^2} + \sqrt{I_{d2} - \left(\sum_{i=1}^n \frac{I_{di}}{n}\right)^2} + \dots + \sqrt{I_{dn} - \left(\sum_{i=1}^n \frac{I_{di}}{n}\right)^2}}{\sum_{i=1}^n \frac{I_{di}}{n}}$$

Six parallel MOSFETs show a turn-on current imbalance of 7.8%, attributed to threshold voltage variation causing turn-on timing dispersion, and transconductance or parasitic asymmetry causing di/dt differences. During turn-off, a 5.8% imbalance results from slight desynchronization and instantaneous current divergence. A symmetrical low-inductance layout enables this effective dynamic current sharing, maximizing current utilization and reliability.

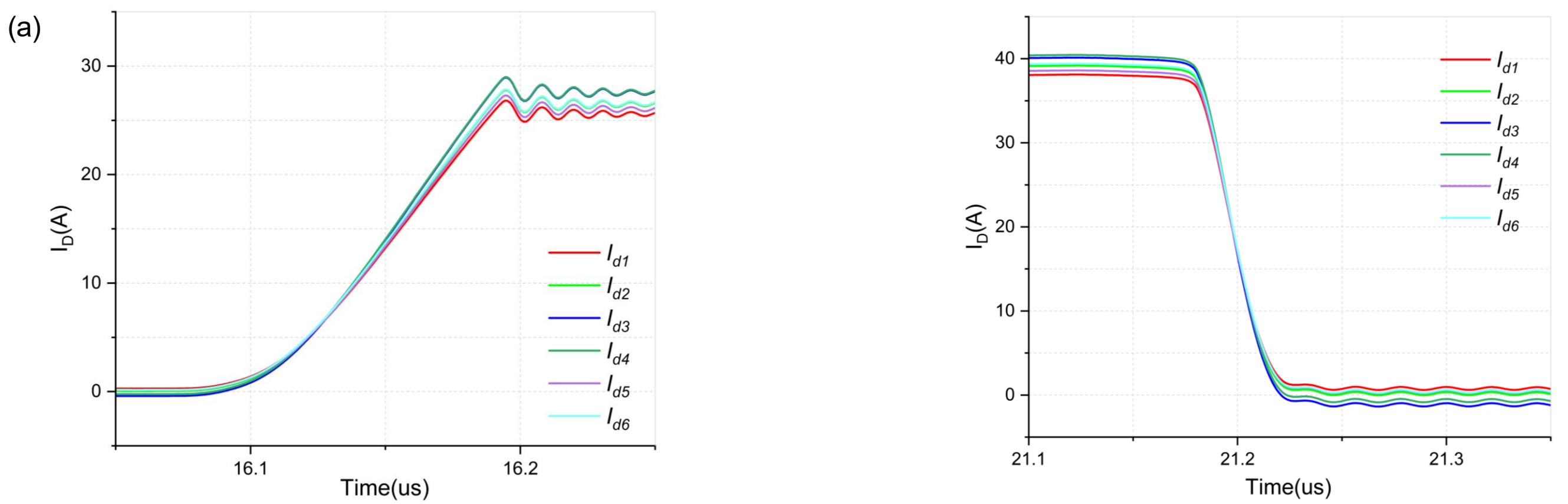


Fig.9 Current sharing characteristics of the MOSFETs

5. Thermal Performance

Isothermal surfaces serve as nodes to build Caue or Foster thermal models. In the Caue model, R_{th} is proportional to layer thickness, and both R_{th} and C_{th} are derived from the material's thermal properties. Flow rate dominates cooling system R_{th}, which drops significantly with higher flow, while it rises moderately with coolant temperature. At the typical 65°C, 10 L/min condition, R_{th}≈0.1 K/W, keeping junction temperature within safe limits.

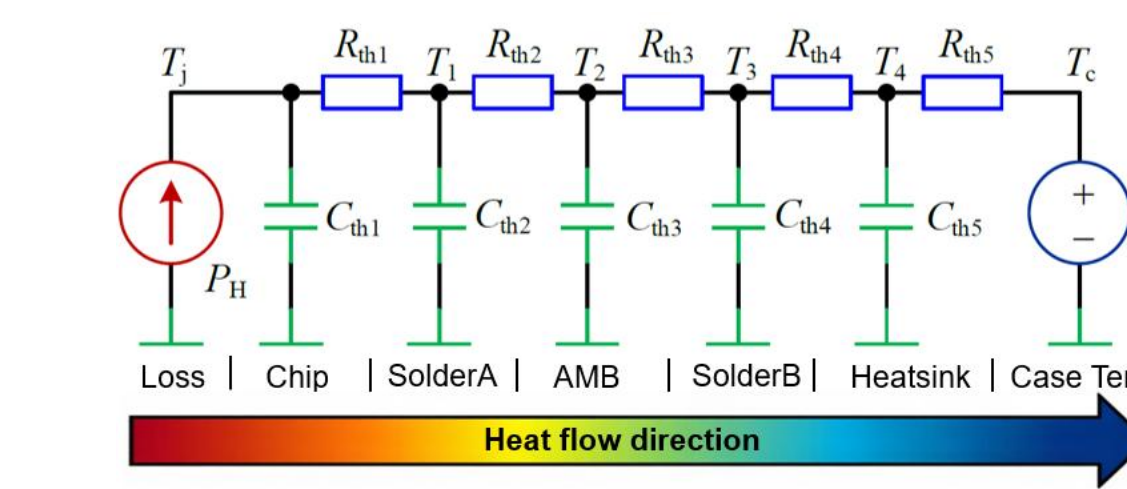


Fig.10 Caue Model

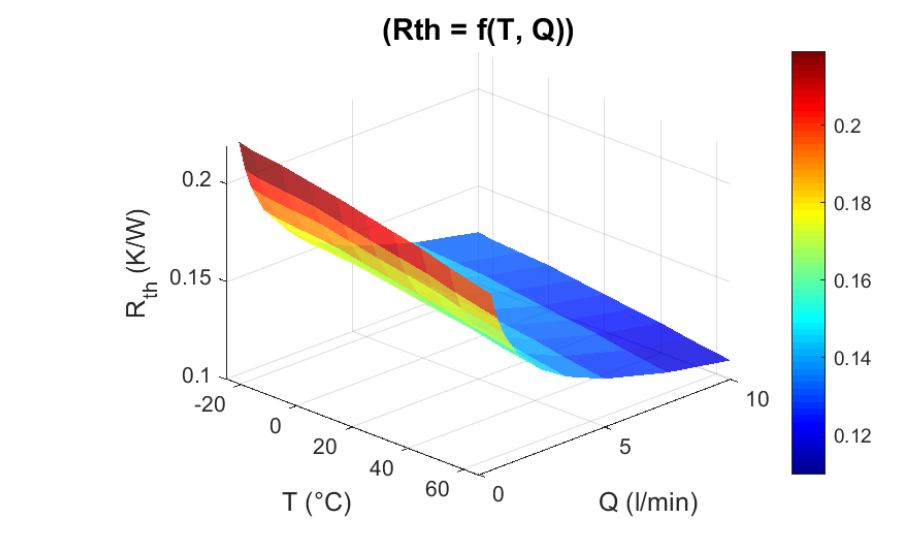


Fig.11 3D Thermal resistance contour

6. Dynamic Junction Temperature Calculation

The electro-thermal model couples instantaneous loss calculation with a thermal network: electrical losses heat the chip, and the resulting dynamic junction temperature (T_j) is fed back in real time to update the losses. Contour maps reveal that at a high DC-link voltage, the output current is the dominant factor driving the T_j rise, while the voltage and switching frequency exhibit a synergistic effect, together defining the Safe Operating Area (SOA). Under the following conditions—coolant inlet temperature of 65 °C, flow rate of 10 L/min, switching frequency of 10 kHz, DC-link voltage of 800 V, and T_j limit of 175°C, the module delivers a continuous output current of 550 Arms, confirming its practical operating boundary.

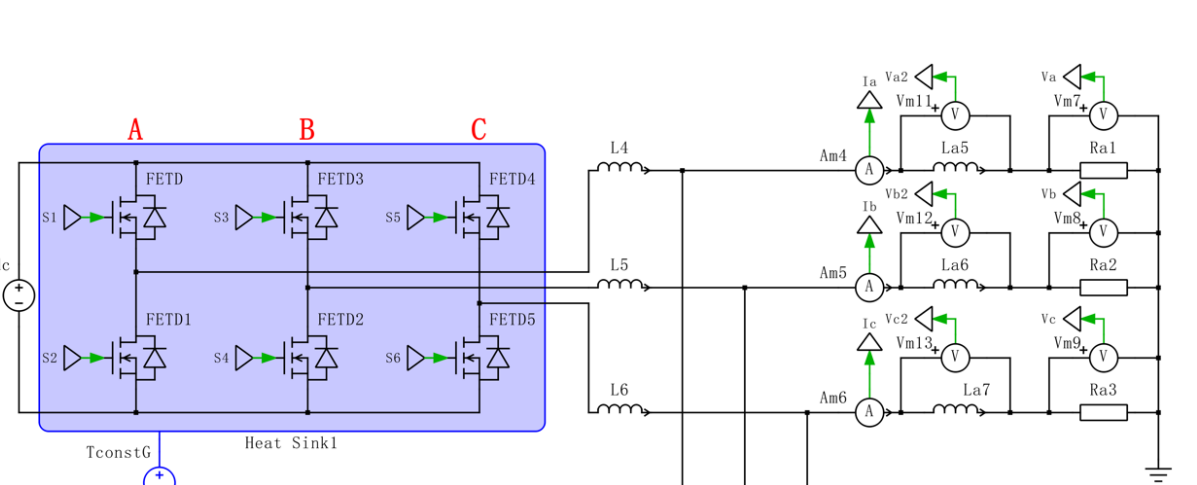


Fig.12 Electro-Thermal Model

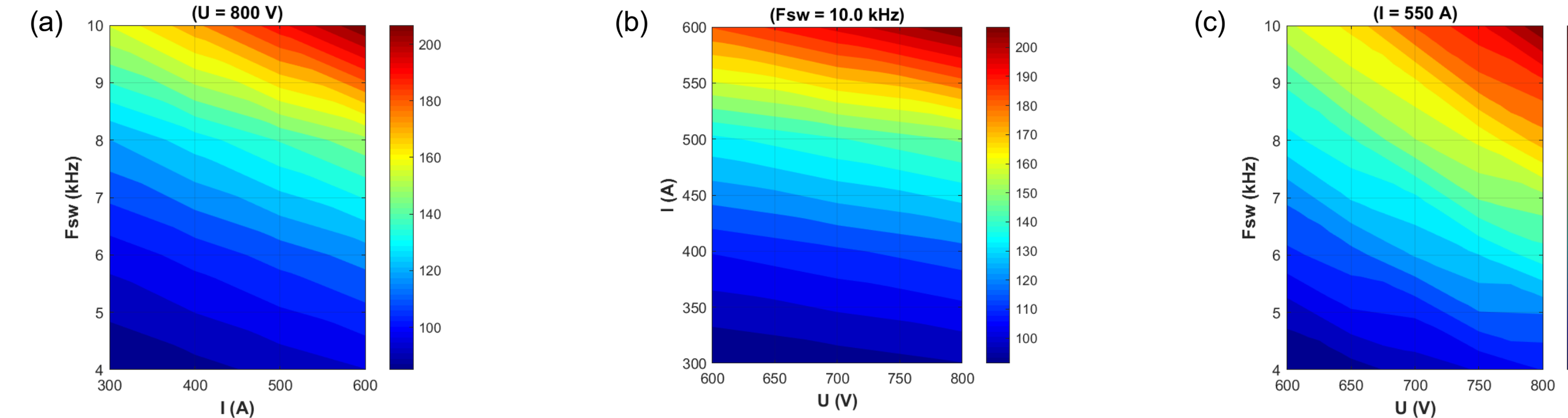


Fig.13 Contour map of junction temperature distribution

7. Lifetime Simulation

Based on power cycling (PC) data and the Coffin–Manson model, a thermal fatigue life model was established. Junction temperature profiles were obtained from an electro-thermal simulation under a realistic mission profile, and the rainflow counting method was applied to extract thermal cycles with different amplitudes (ΔT_j) and counts. Using Miner's linear cumulative damage rule, the cumulative damage index (CDI) was calculated. Under the evaluated condition (coolant 65°C, 10 L/min, 10 kHz, 800 V), the module's CDI over the 8000 h design life is approximately 17%, leaving an 83% life margin, which confirms an extremely high reliability margin and long-life capability.

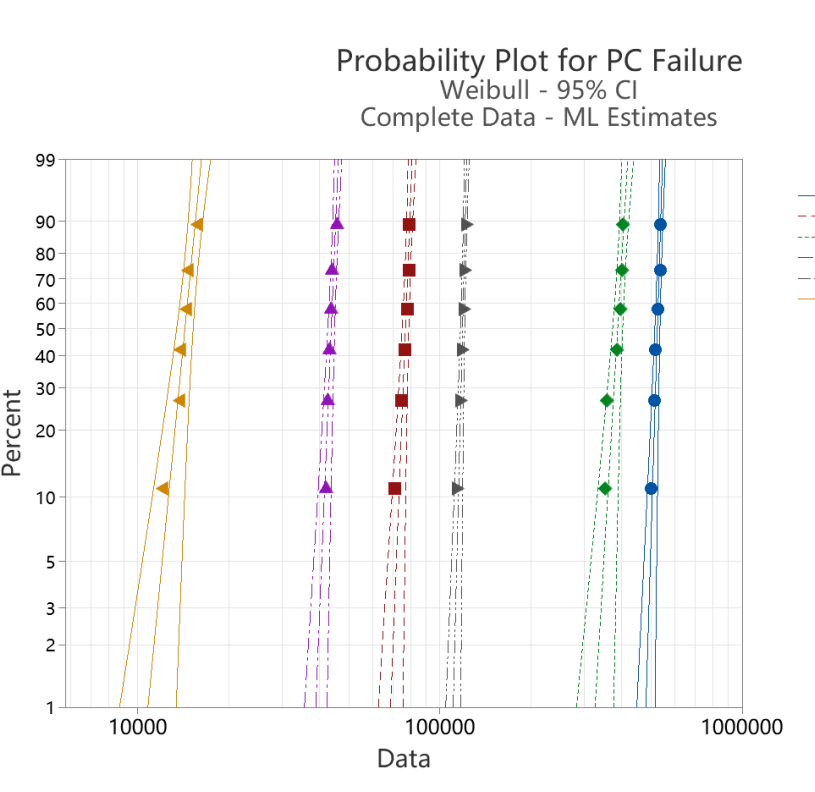


Fig.14 Probability Plot for PC Failure

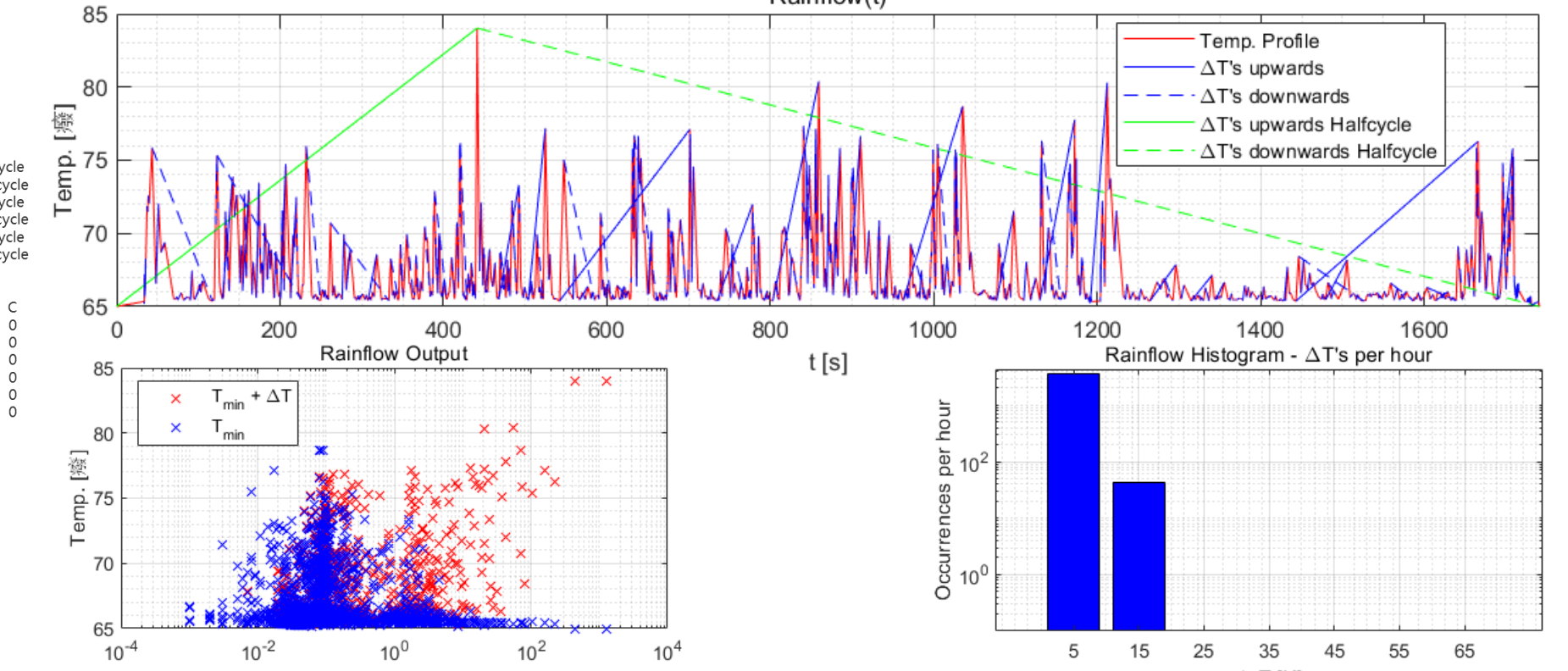


Fig.15 Rainflow Counting Analysis

CONCLUSION :

An electro-thermal-reliability co-design evaluation of a 1200 V 6-in-1 SiC power module for 800–950 V high-voltage platforms was conducted using combined experimental and simulation methods. The module demonstrates low RDS(on), excellent dynamic current sharing, a continuous output of 550 Arms under typical conditions, and CDI of approximately 17% under an automotive load profile based on the Coffin–Manson model, indicating a substantial reliability margin. These results confirm that the module meets high-end application requirements, and the multiphysics co-design methodology provides a valuable reference for high-power-density, high-reliability power module development.

References

- H. A. Mantooth, M. D. Glover, and P. A. Losee, "SiC Power Module Design: Challenges and Opportunities," in *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 1896–1907, March 2018.
- X. Perpina, M. Vellvehi, and J. M. Reynes, "Electro-thermal simulation of power modules: A review," in *Microelectronics Reliability*, vol. 54, no. 9–10, pp. 1509–1524, Sep-Oct 2014.
- R. Amro, J. Lutz, and A. Lindemann, "Power cycling capability of modules for traction applications," in *Microelectronics Reliability*, vol. 46, no. 9–11, pp. 1704–1709, Sep-Nov 2006.
- F. Yang, X. Du, and B. Ji, "Dynamic Current Sharing Analysis and Improvement for Paralleled SiC MOSFETs," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 10, pp. 7561–7571, Oct. 2019.
- M. Andresen, G. Buticchi, and M. Liserre, "A Thermal Analysis Method for Power Electronic Systems based on Caue and Foster Networks," in *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Vancouver, BC, Canada, 2016, pp. 1–8.
- U. Choi, F. Blaabjerg, and K. Ma, "Power Cycling Test Methods for Reliability Assessment of Power Device Modules in Respect to Temperature Stress," in *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2531–2551, March 2018.