

Overload Investigation of 3.3kV SiC-MOSFET Power Module for Medium-Power Applications

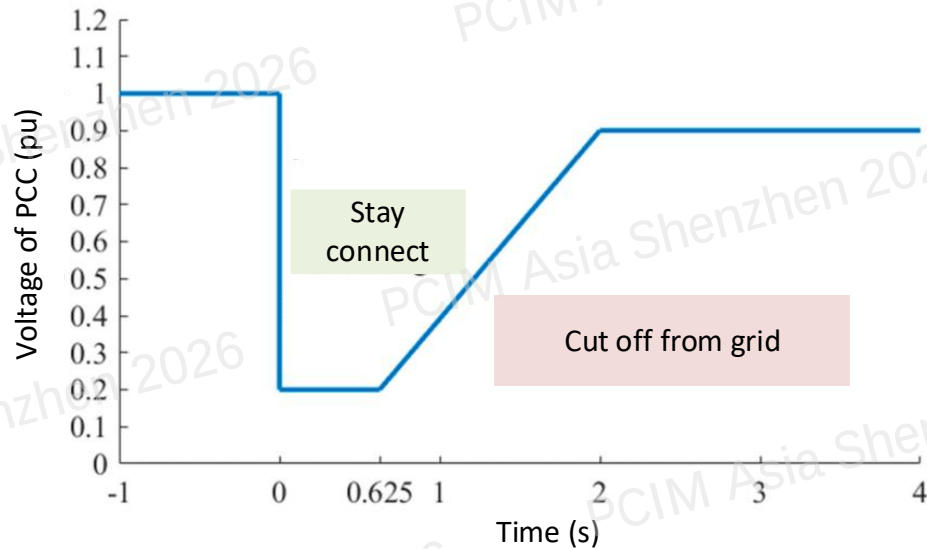
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- **Background**
- **Converter basics**
- **Losses and thermal calculation**
- **Results**
- **Conclusions**

Overload

Why overload matters?

- Over high current required for
 - Fault transients, e.g. LVRT
 - Grid service fulfilment, such as inertia support.



Low-voltage ride-through (LVRT) requirement

$$\rightarrow I = P/U$$

$\rightarrow$ current increase to keep power stable

- Why power module?
- Lowest time constant compared to remaining parts, such as transformer, reactor, etc.

$\rightarrow$ Fastest thermal failure for power module

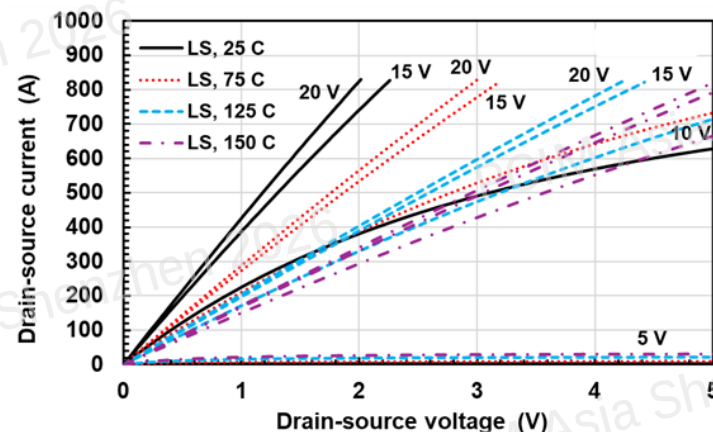
- Why SiC?
 - Higher thermal limit than Si-IGBT power module (normally 175 °C vs. 125 °C)
- **What is the impact on overload?**
- **Is SiC replacement also beneficial from overload perspective?**

Overload capability is a critical specification for system transients

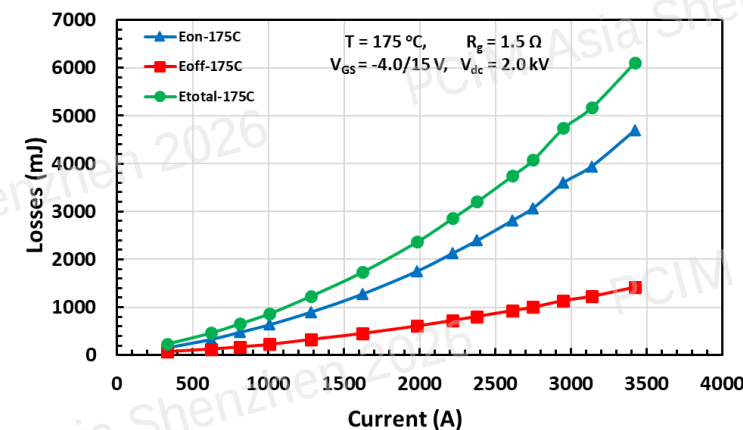
Overload

Device Characteristics

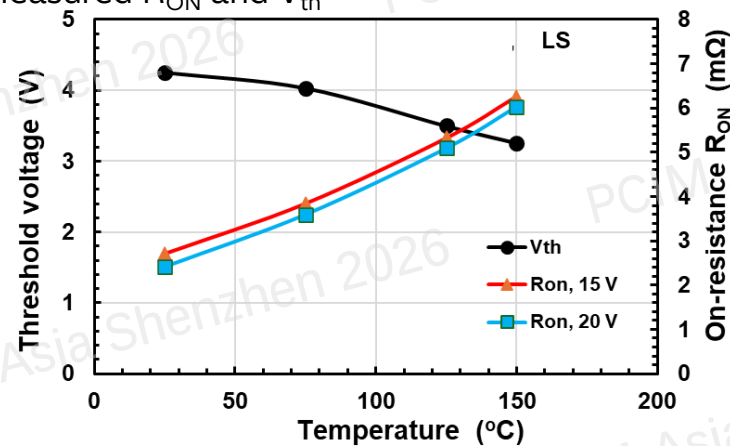
Measured I-V curves



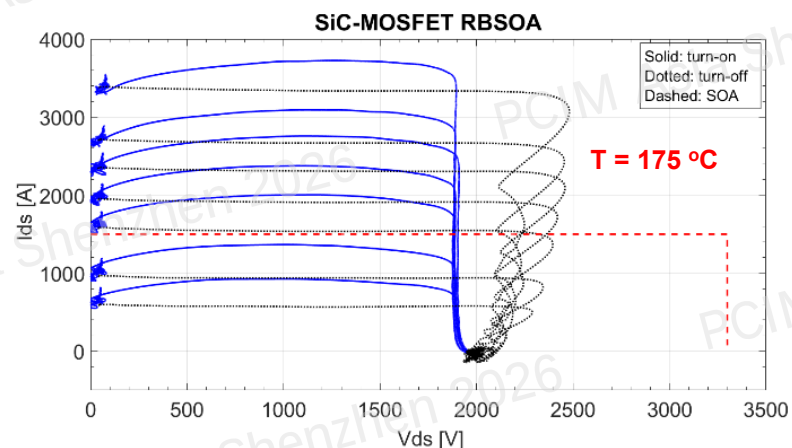
Measured E_{on}/E_{off} data with current up to 3500 A



Measured R_{ON} and V_{th}



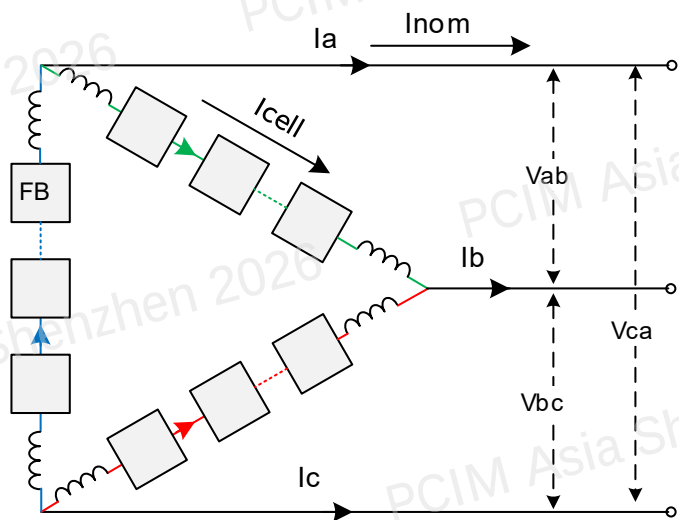
SOA tracing for turn-on (blue) and turn-off transients (black)



Static and dynamic tests to confirm health status and define overload limit @ 175 °C

Overload

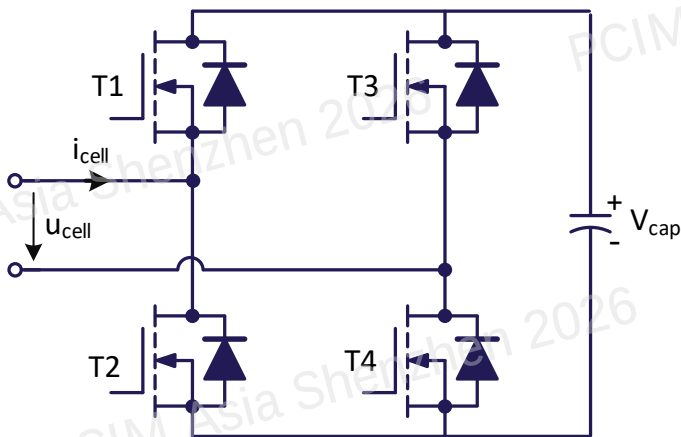
Converter Topology



Assumptions:

- Constant cell DC cap voltage
- One FB cell only operating in +V/-V/bypass mode
- MOSFET can conduct bidirectionally – no current flowing through the body diodes except commutation
- Current evenly flowing through 4 switching positions

3.3 kV SiC-MOSFET cell



Mode	Positive I	Capacitor
Insert $U_{cell} > 0$	SiC-MOSFET: T1, T4	Charge $i_{cell} > 0$ Discharge $i_{cell} < 0$
Insert $U_{cell} < 0$	SiC-MOSFET: T2, T3	Charge $i_{cell} < 0$ Discharge $i_{cell} > 0$
Bypass $U_{cell} = 0$	SiC-MOSFET: T1, T3 / T2, T4	Bypassed

Identical power losses for each switching position

Overload

Converter Parameters

– Parameters input

Specification	Parameter
Targeted grid-connected line voltage levels U_{ac}	35 kV
Targeted arm switching frequency $f_{sw,arm}$	6 kHz
Cell DC voltage V_{dc}	2 kV
Device case temperature T_c	50 °C, 80 °C.
Thermal limit $T_{j,SOA}$ (device failure criteria)	175 °C (present) and 250 °C (future) for 3.3 kV SiC-MOSFET module.



– Resultant scenarios

#	Voltage U_{ac} (kV)	Cell# per arm	Device switching frequency $f_{sw,d}$ (Hz)	Sweeping parameters:
1	35	26	57	$T_c = 50\text{ °C}, 80\text{ °C}.$ $T_{j,SOA} = 175\text{ °C}, 250\text{ °C}.$

Higher thermal limit expected for SiC module

Overload

Thermal Model & Loss Calc.

- Coupling relationship between power losses and junction temperature of power module
- Conduction losses

$$P_{cond} = R_{on}(T_j) \cdot I_{rms}^2$$

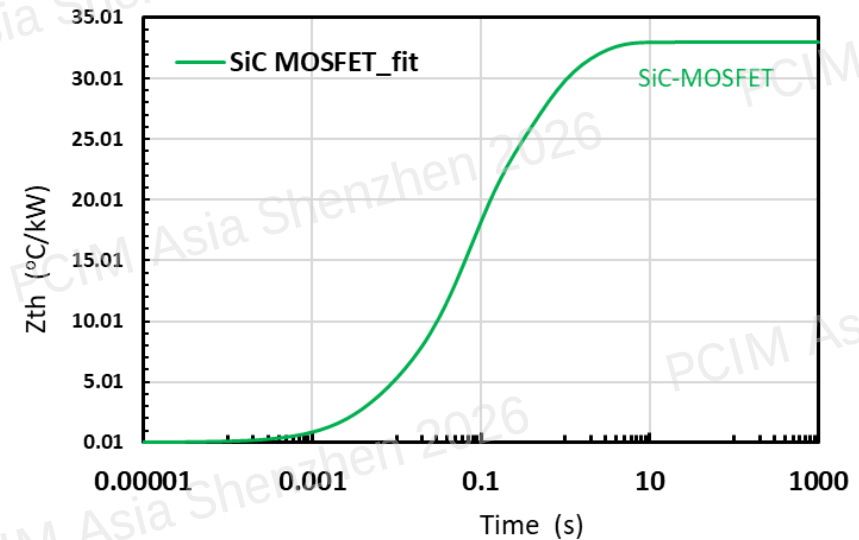
- Switching losses

$$P_{sw} = \frac{Nf_1 V_{dc} I_{avg}}{V_{ref} I_{ref}} \left[k_{on} \cdot (E_{on}(T_j) + E_{rec}(T_j)) + k_{off} \cdot E_{off}(T_j) \right]$$

Coupling P_{loss} and T_j

$$\begin{cases} \Delta T_{j,(n-1)} = P_{loss,(n-1)} \sum_{i=1}^3 R_i \left(1 - e^{-\frac{\Delta t}{\tau_i}} \right) \\ \Delta T_{j,n} = \Delta T_{j,(n-1)} \sum_{i=1}^3 R_i e^{-\frac{\Delta t}{\tau_i}} + P_{loss,n} \sum_{i=1}^3 R_i \left(1 - e^{-\frac{\Delta t}{\tau_i}} \right) \end{cases}$$

- Thermal impedance model
 - Assumed constant case temperature
 - $Z_{th,JC}$ from junction to case from datasheet applied



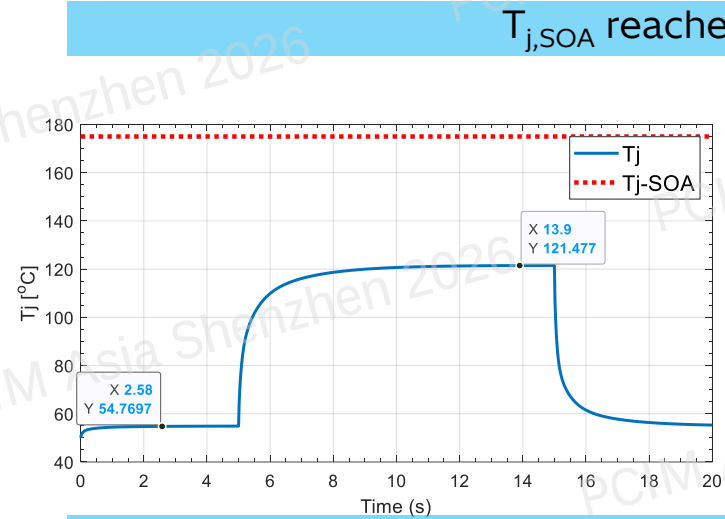
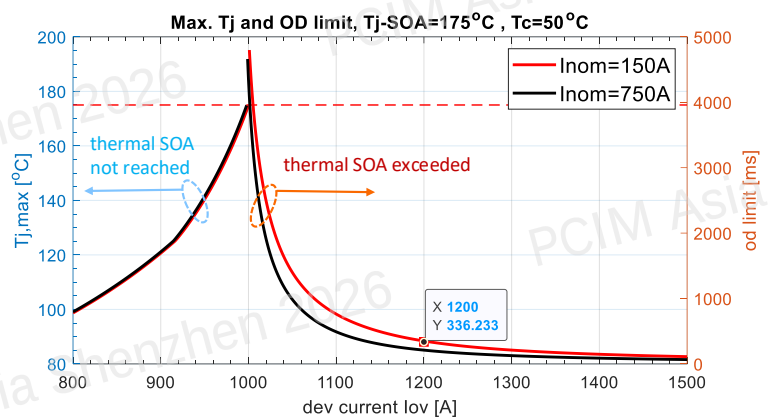
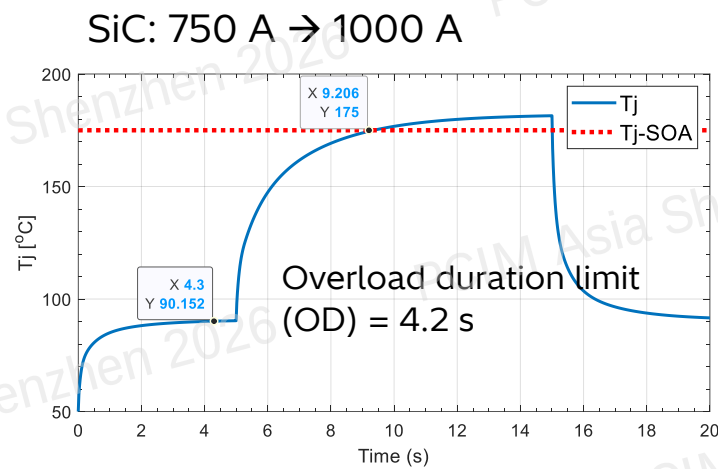
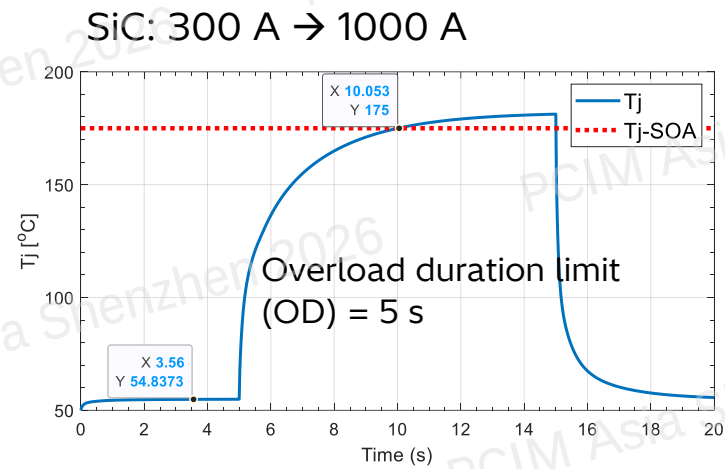
Iterative discrete calculation between power losses $P_{loss} = (P_{cond} + P_{sw})$ and junction temperature T_j

Overload

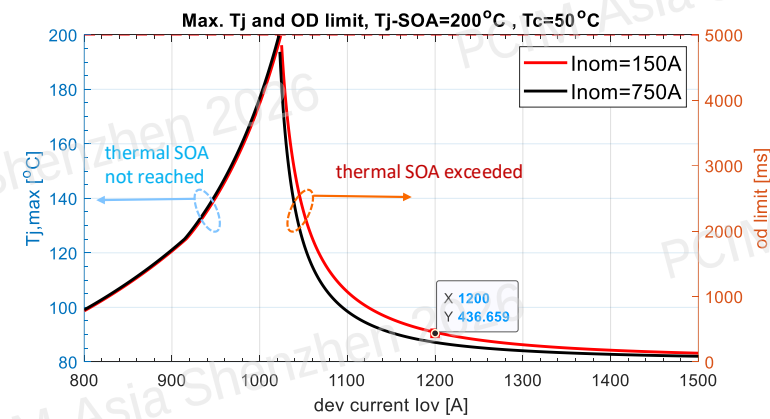
Results – device level

Individual operating point

Overload operation sweep



SiC: 300 A → 900 A
 $T_{j,\text{max, SiC}} = 121^{\circ}\text{C}$



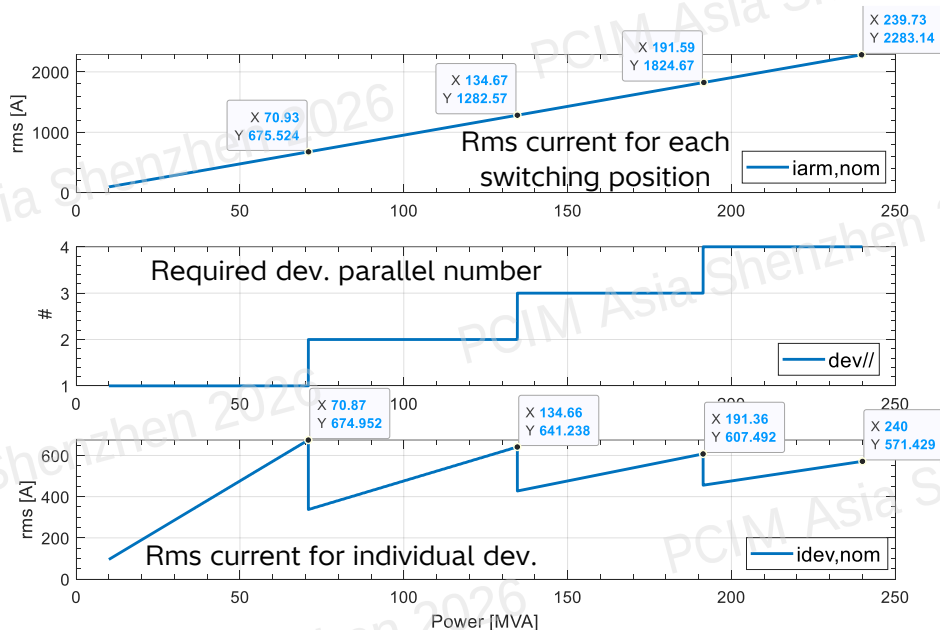
$T_{j,\text{SOA}}$ NOT reached → $T_{j,\text{max}}$ recorded

- Impacts of overload current (I_{ov}), normal operating current (I_{nom}) and thermal limit ($T_{j,\text{SOA}}$) on OD: $\uparrow I_{ov}$, $\uparrow I_{nom}$, $\downarrow T_{j,\text{SOA}}$ → $\downarrow \text{OD}$

Overload

Results (converter level) – $T_{j,SOA}$ reached

– Converter normal operating → determine device parallel



- Current derating due to SiC module parallel

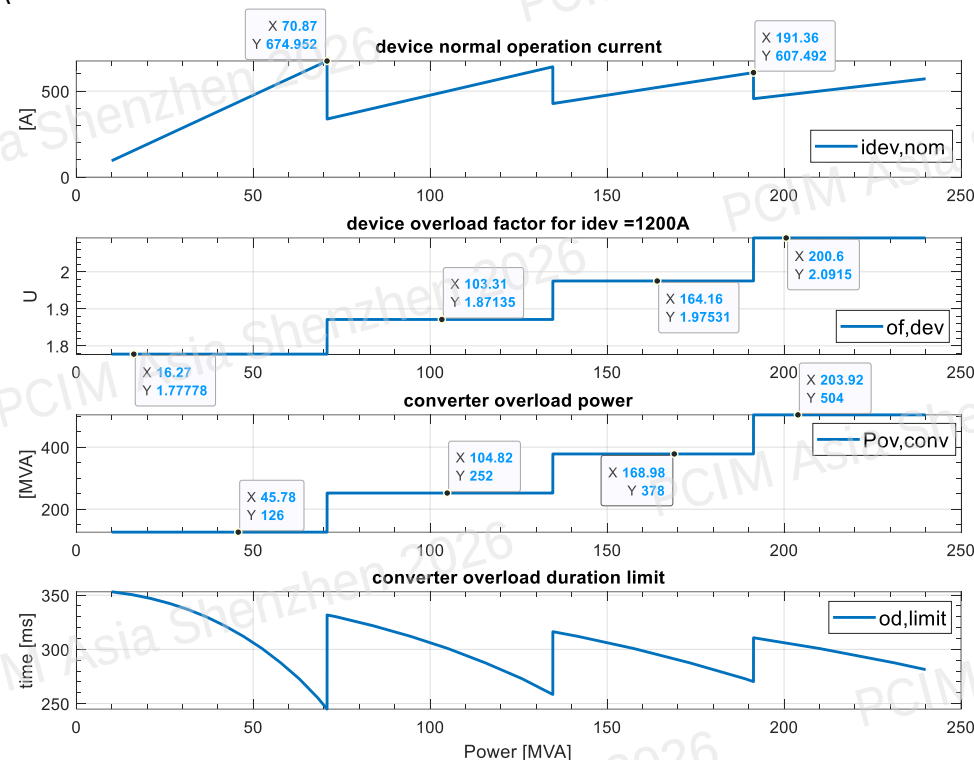
– Converter normal operating → overload operating
@ $T_c = 50\text{ }^{\circ}\text{C}$ $T_{j,SOA} = 175\text{ }^{\circ}\text{C}$

Normal operating rms current for each dev.

Calculated dev. overload factor for $I_{ov} = 1200\text{ A}$

Resultant converter overload power for $I_{ov} = 1200\text{ A}$

Resultant converter overload duration limit for $I_{ov} = 1200\text{ A}$

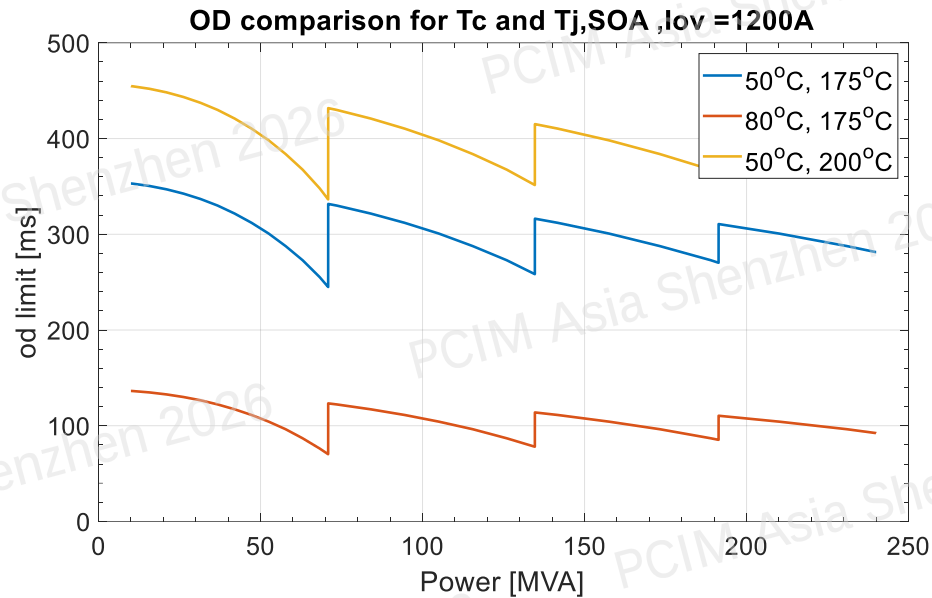


Lower dev. parallel number → higher OD range

Overload

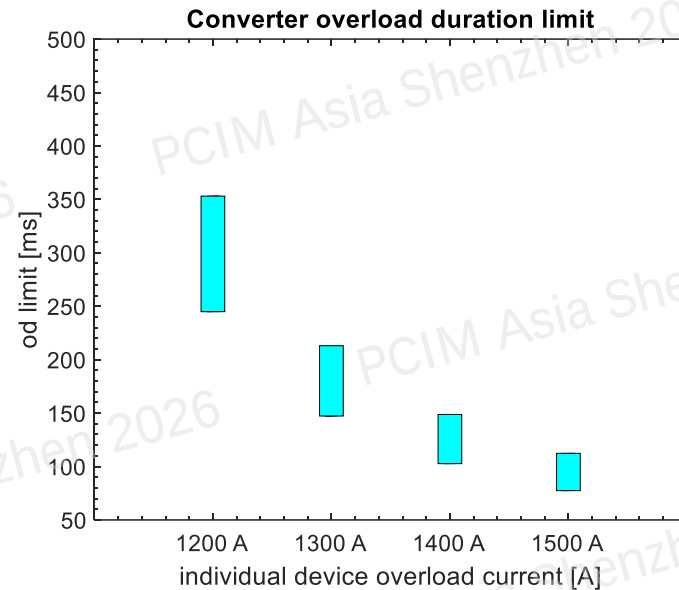
Results – converter level

- Converter overload duration along with rated power range @ different T_c $T_{j,SOA}$ and fixed $I_{ov} = 1200$ A

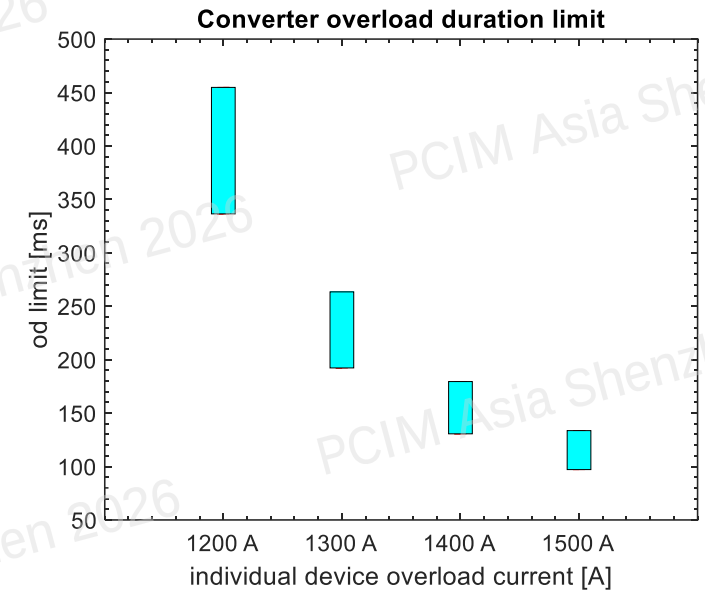


- Converter overload duration range along with overload current I_{ov}

@ $T_c = 50$ °C $T_{j,SOA} = 175$ °C



@ $T_c = 50$ °C $T_{j,SOA} = 200$ °C



Converter overload duration limit depends on overload current and temperature limits

Overload

Conclusions

- 3.3 kV SiC power module can operate at high overload current up to 3500 A at high temperature up to 175 °C.
- 3.3 kV SiC can benefit converter overload capability within 80 – 450 ms depending on overload conditions incl. overload current, temperature limit and device parallel.