

Performance of a New Power MOSFET Technology Designed to Serve the Requirements of Motor-Drive Applications

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Motor drives ask for a different device balance

- low $R_{DS(on)}$, high current capability and low reverse-recovery charge outweigh low gate- and gate-drain charge
- switching frequency typically stays near 10 kHz, but dv/dt needs to be limited to about 5 V/ns
- the V_{DS} overshoot must meet the derating limit, being typically 80 % of 100 V

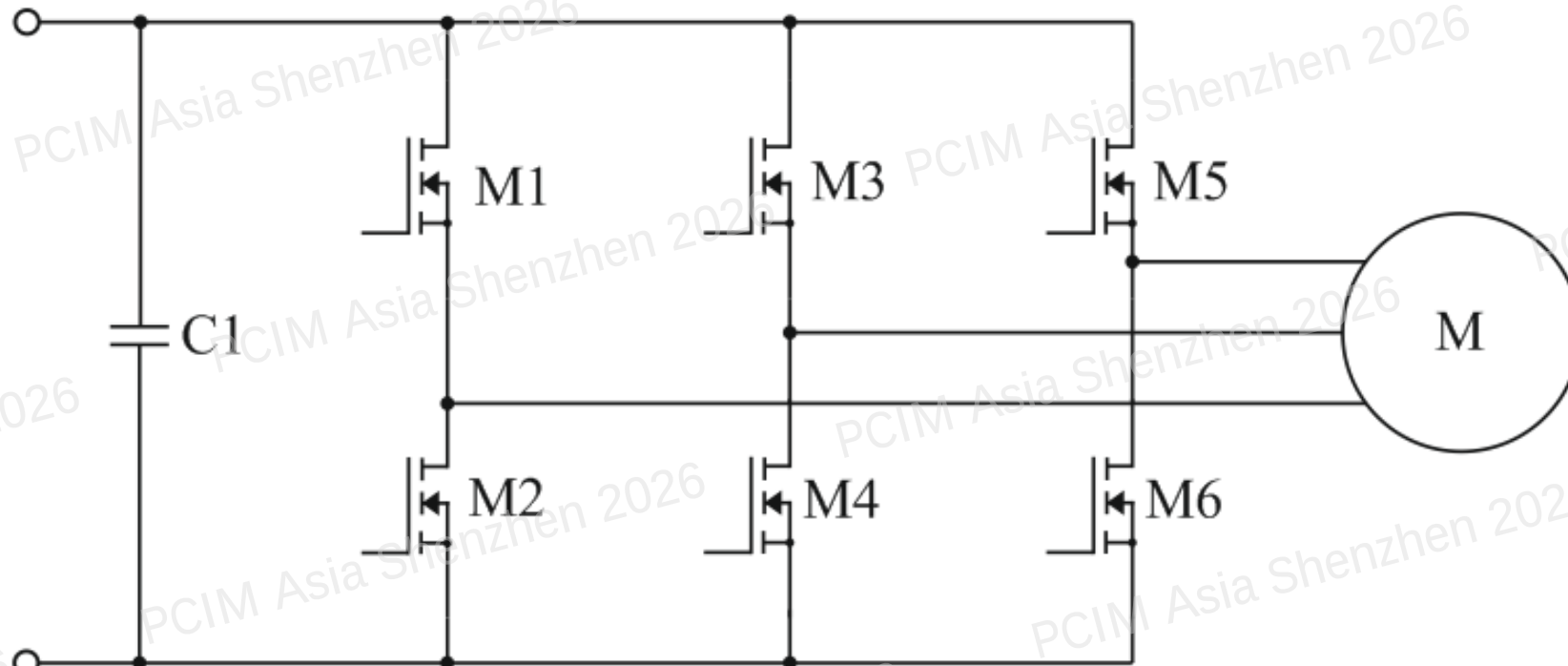


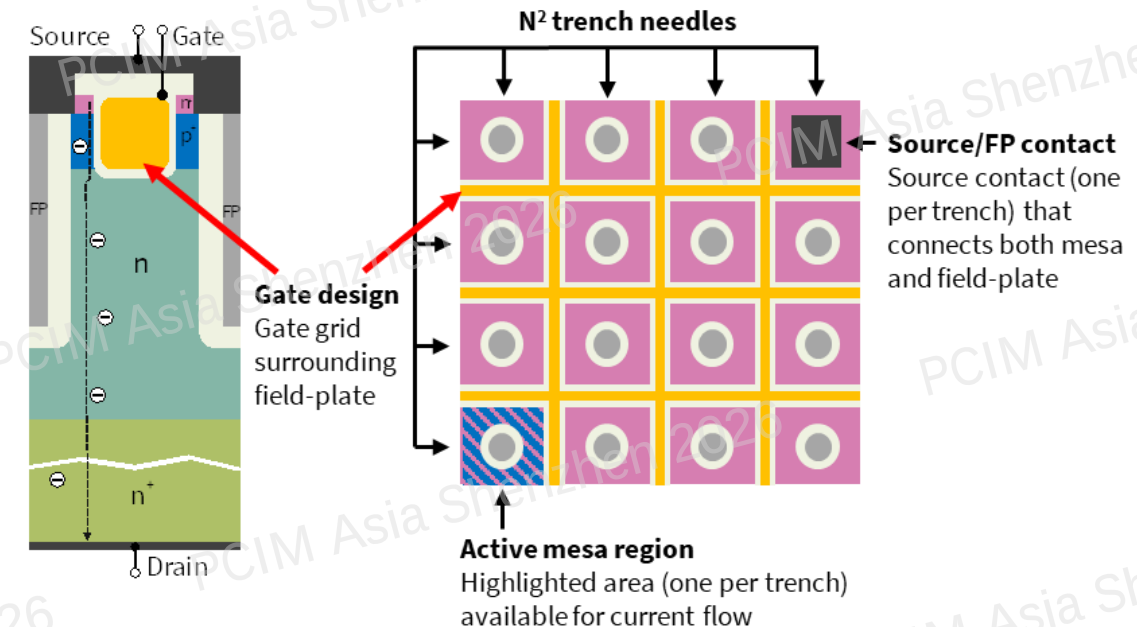
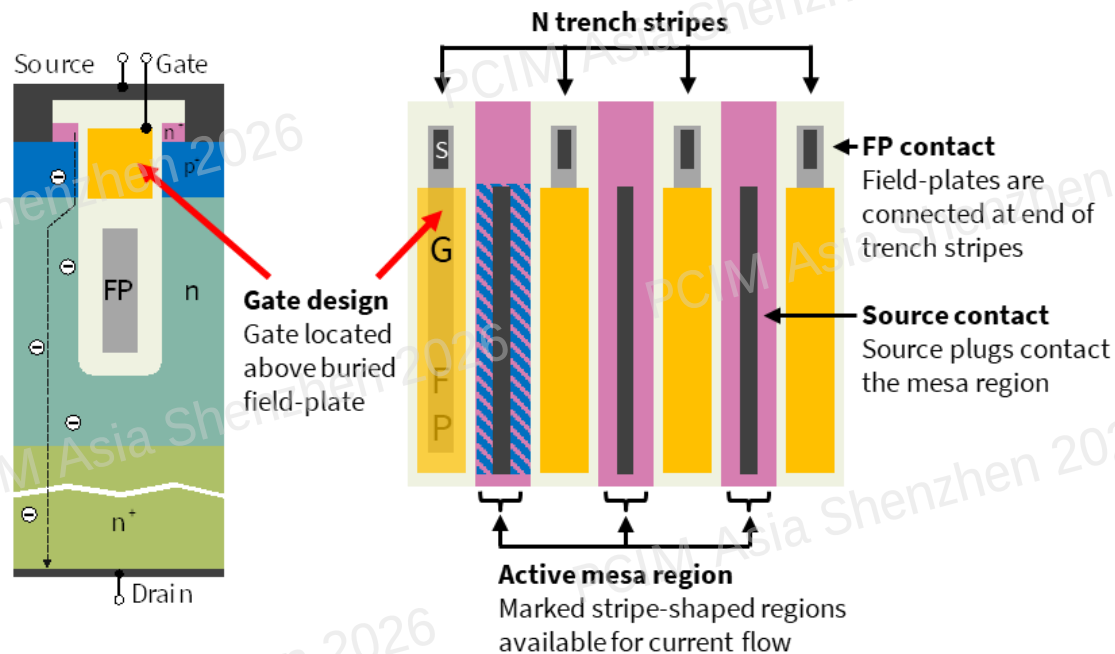
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Introduction of Device Concept

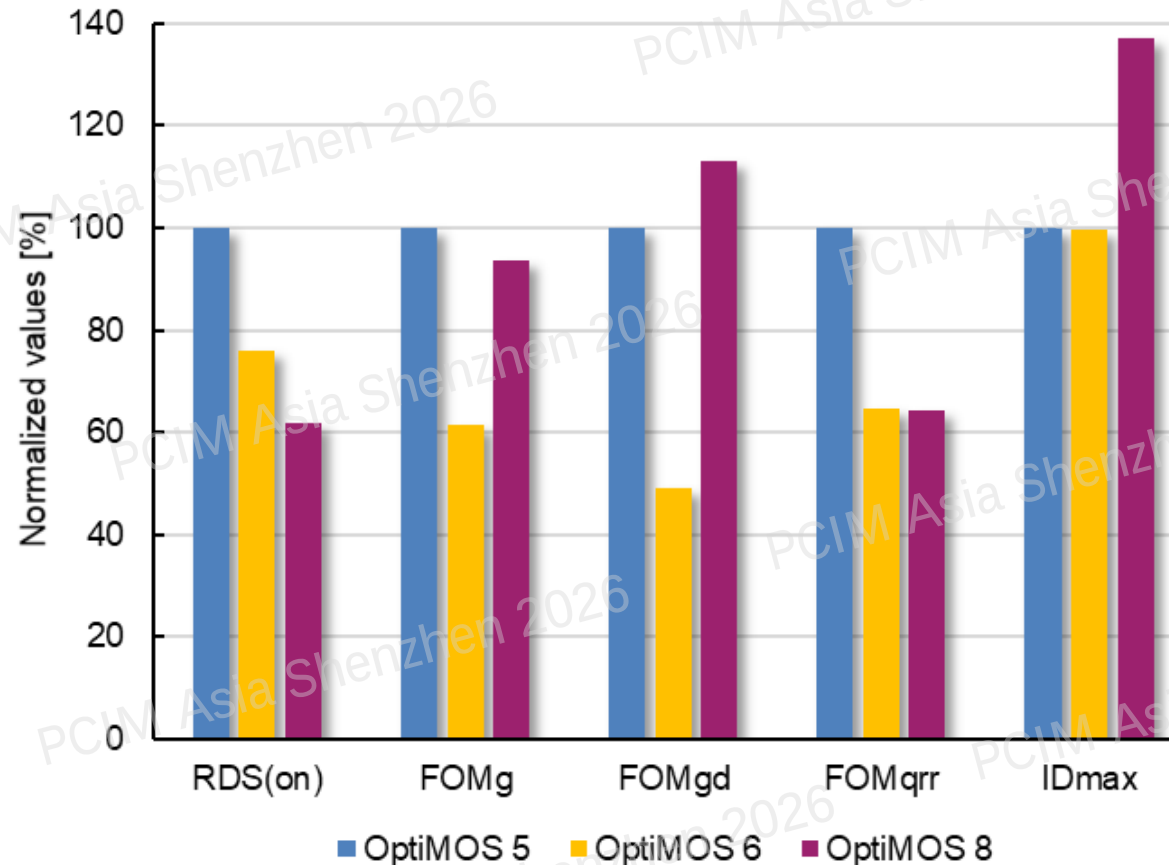
From stripe-cells to a grid-like needle layout

- lateral charge compensation by an insulated field-plate that is connected to source
- 2D stripe-shaped trench cells represent the industry standard
- 3D charge compensation due to needle trenches surrounded by a gate trench grid yield larger conduction area
- metal gate ensures a low, homogeneously distributed gate resistance
- direct field-plate connection eliminates almost any resistance delaying the charging of the output capacitance



Switching-optimized versus drive-optimized

- OptiMOS™ 5 represents the established stripe-cell technology reference
- OptiMOS™ 6 is switching-optimized: minimum FOM_G and FOM_{GD} for fast switching at several 100 kHz
- OptiMOS™ 8 is drive-optimized: lowest $R_{DS(on)}$, high current and low Q_{RR}



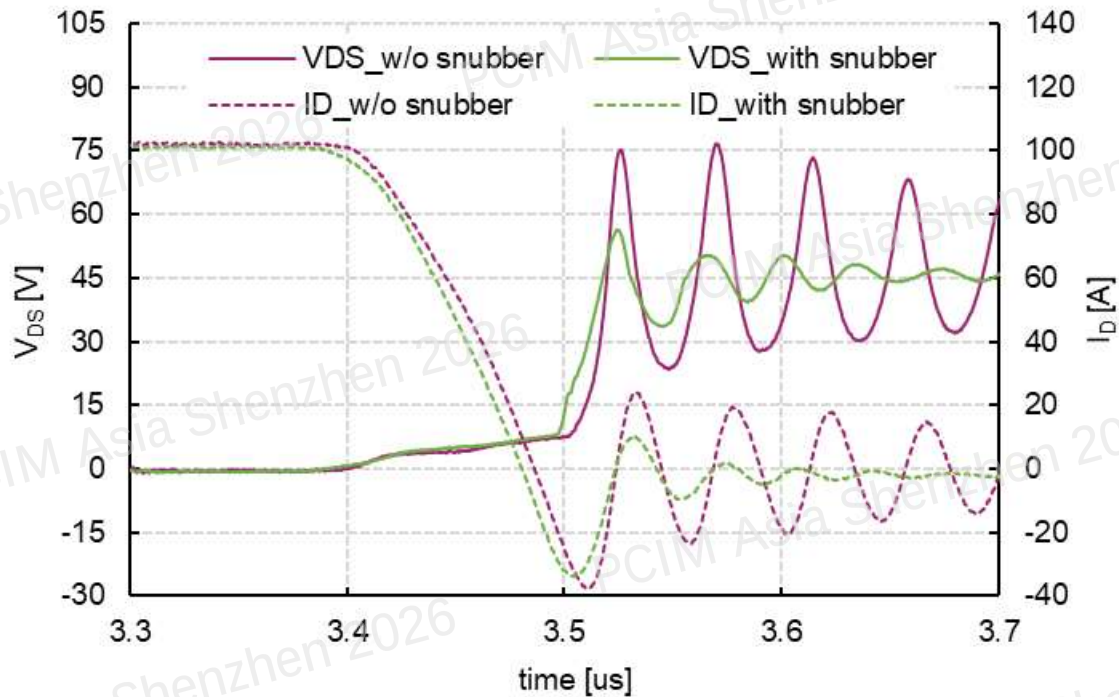


Integrated Nonlinear Snubber

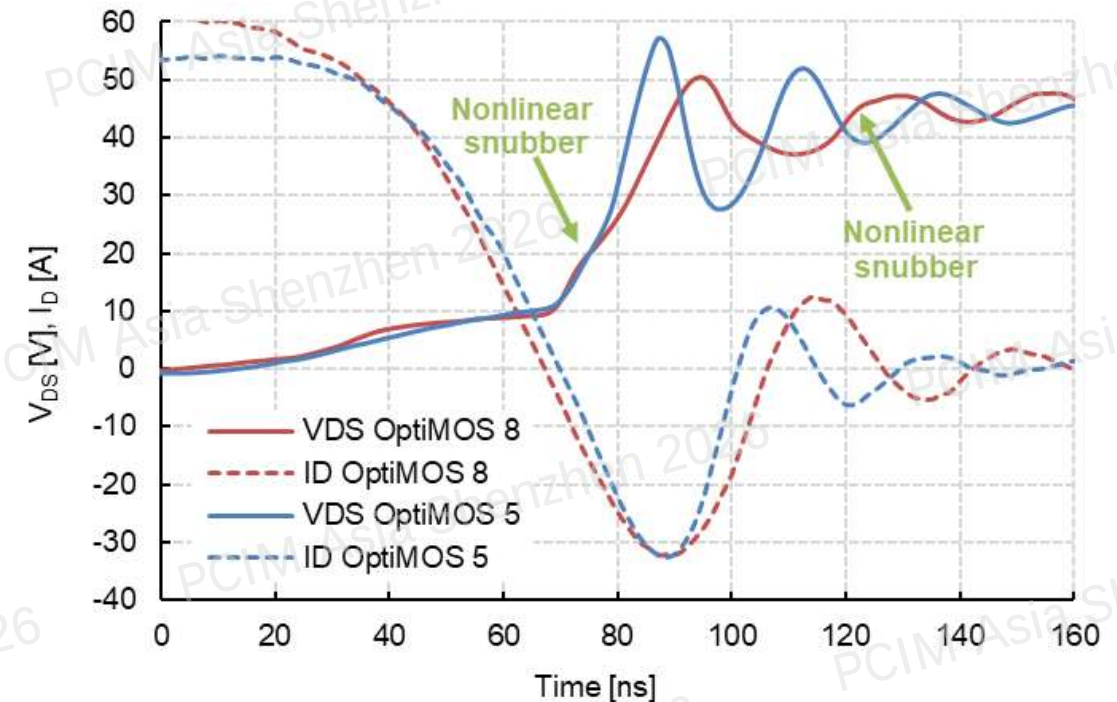
A nonlinear snubber integrated into the device

- the new device comes with an integrated snubber - no external RC or RCD network is required
- the new element limits the drain-source voltage overshoot, and damps the ringing
- V_{DS} slope changes (arrows) reflect the nonlinear snubber action

Same device with and w/o internal snubber

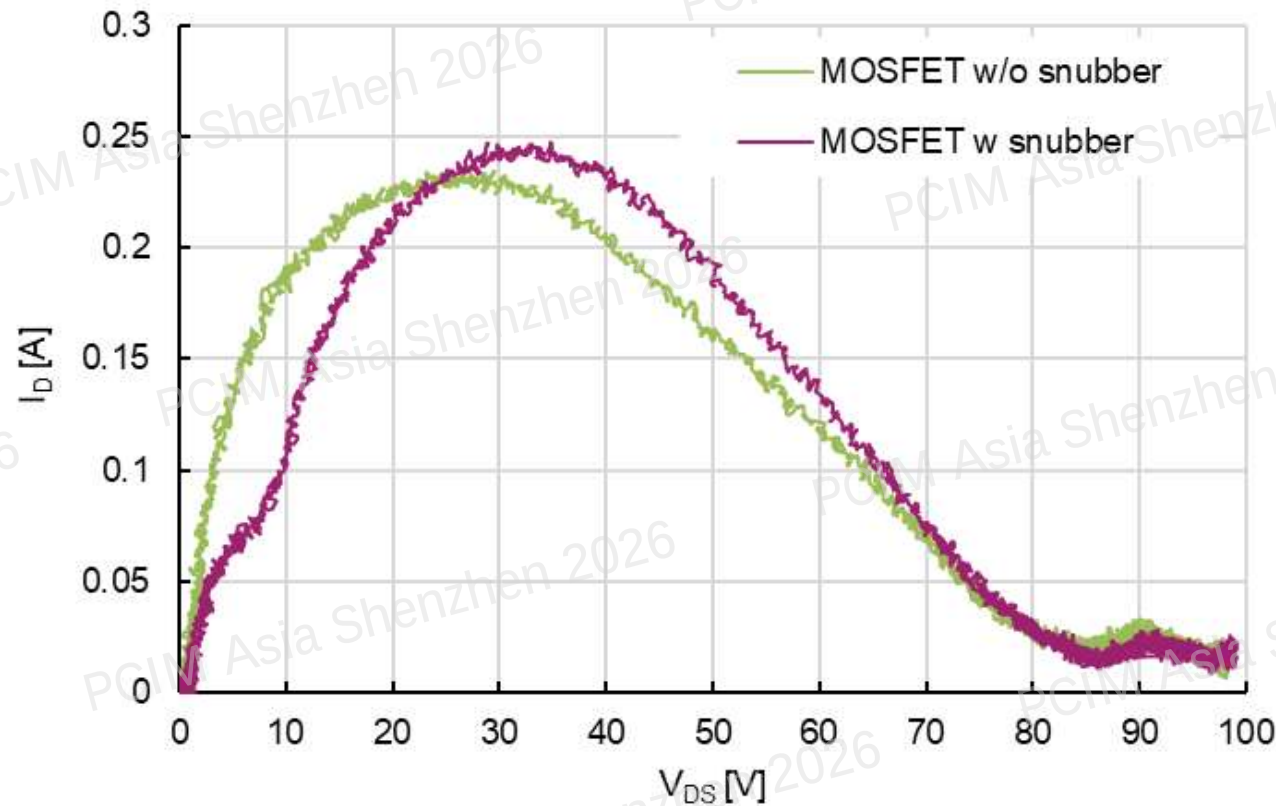


Comparison with stripe-cell device



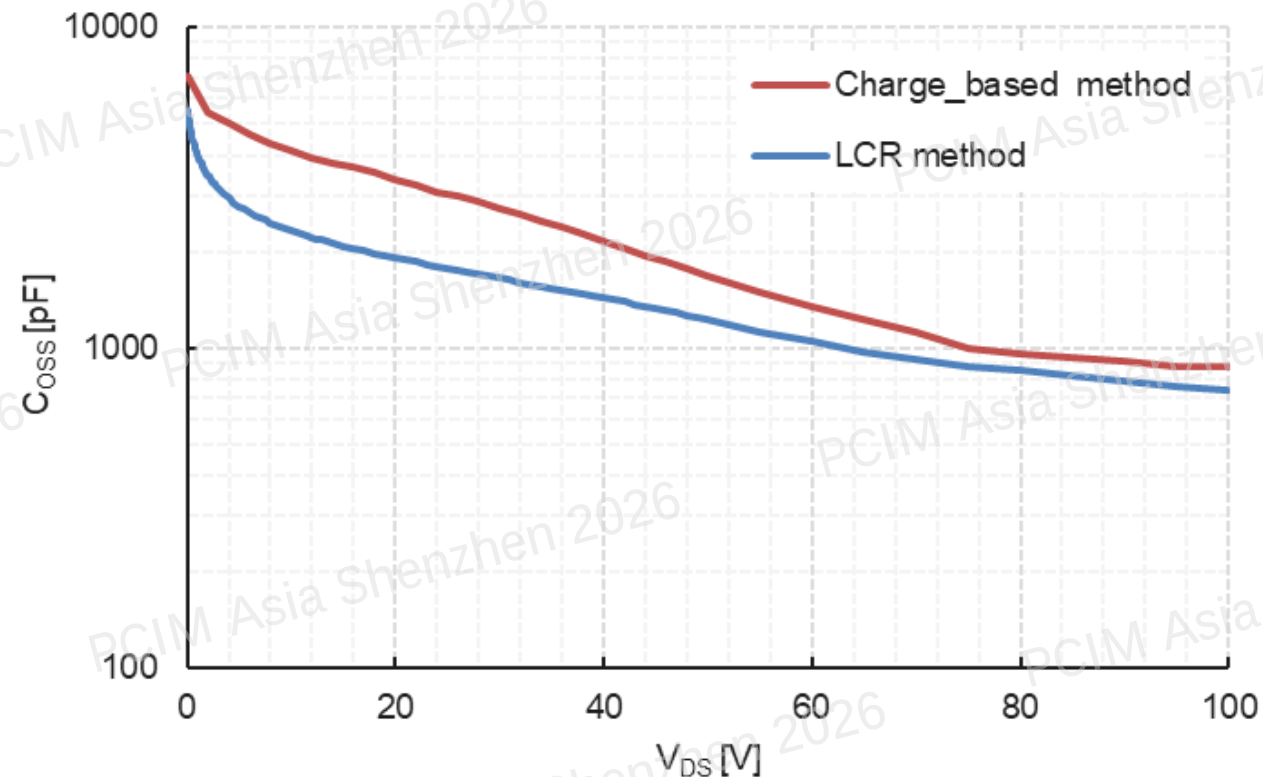
Impact on the output capacitance

- a pulse of $dv/dt = 120 \text{ V}/\mu\text{s}$ charges the output capacitance C_{OSS}
- the current follows the capacitance shape
- with added snubber element, the charging is delayed and C_{OSS} remains low up to about 10 V
- deviations from the ideal shape arise from parasitic inductance in the test circuit



How to correctly measure the output capacitance

- LCR meters use a small AC signal on a slow DC ramp and will report too low values due to the added snubber
- charge-based method: a constant current charges the output capacitance
- the capacitance can be calculated from the integration of the current over time and the drain voltage change
- only the charge-based result is correct



Device Performance in a Motor-Drive Application

pcim
ASIA SHENZHEN



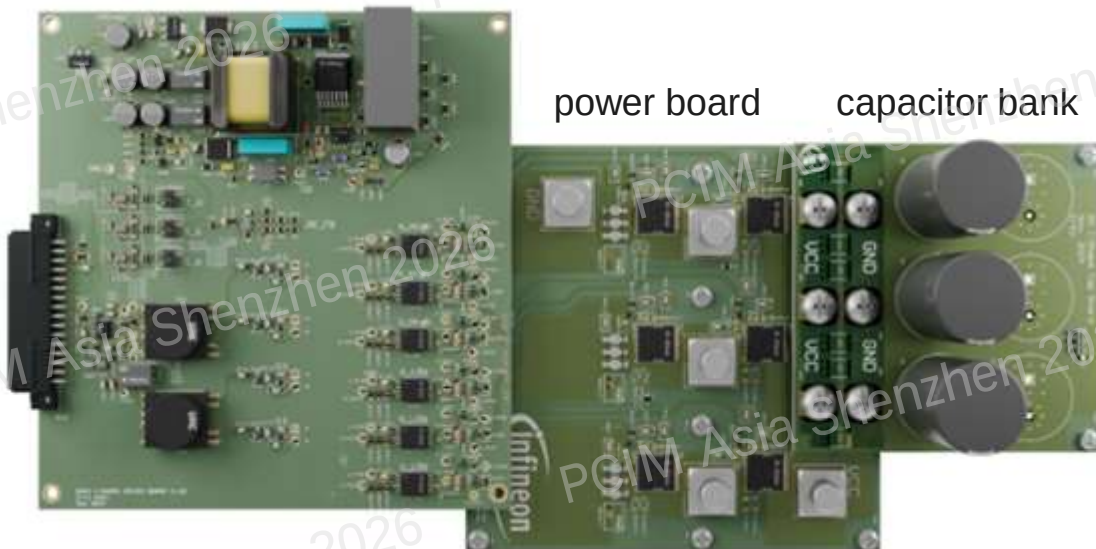
48 V / 4 kW three-phase inverter test platform

- B6 inverter, 48 V input, 82 Arms, 1EDI20H12AH drivers, TOLL or TDSON-8 packages can be used
- V/f control with seven-segment SVM: 520 mV/Hz, 2000 rpm, fsw = 10 kHz, 4 kW output power
- drives a three-phase induction motor coupled to a hysteresis break
- case temperature set to 100 °C
- dv/dt and di/dt matched via external gate resistors and capacitances in order to compare different devices

gate driver

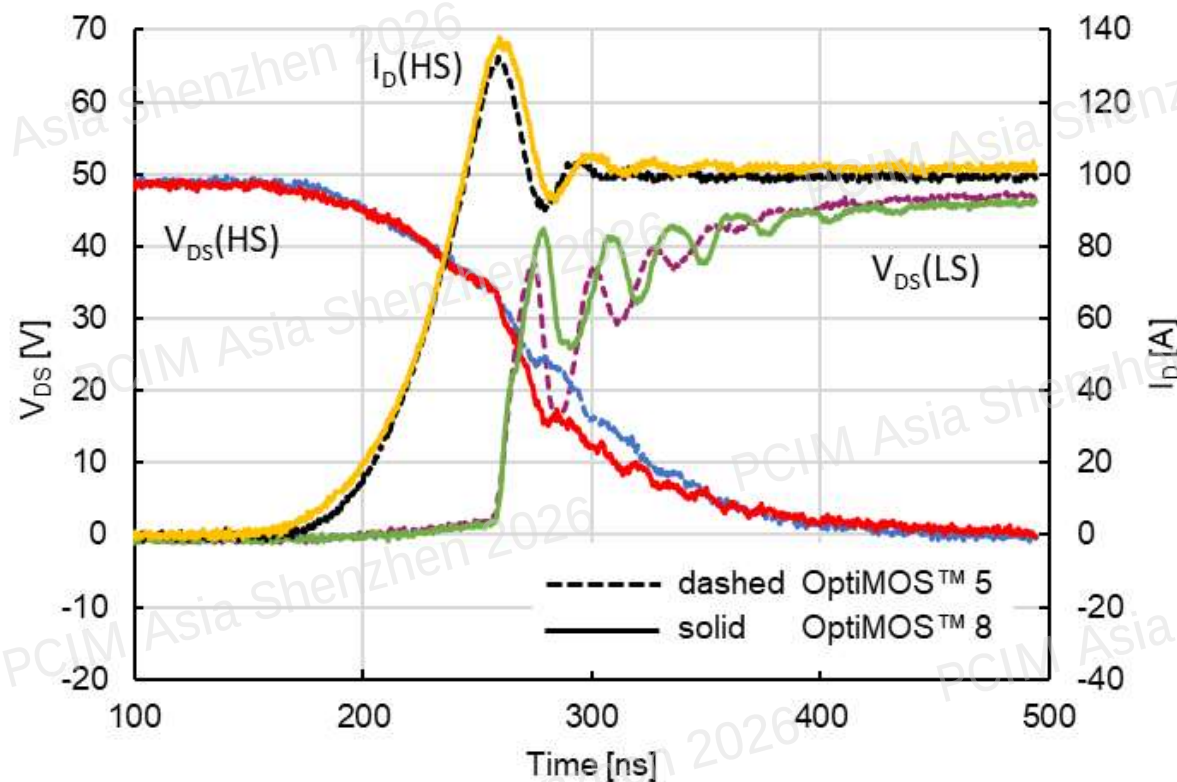
power board

capacitor bank



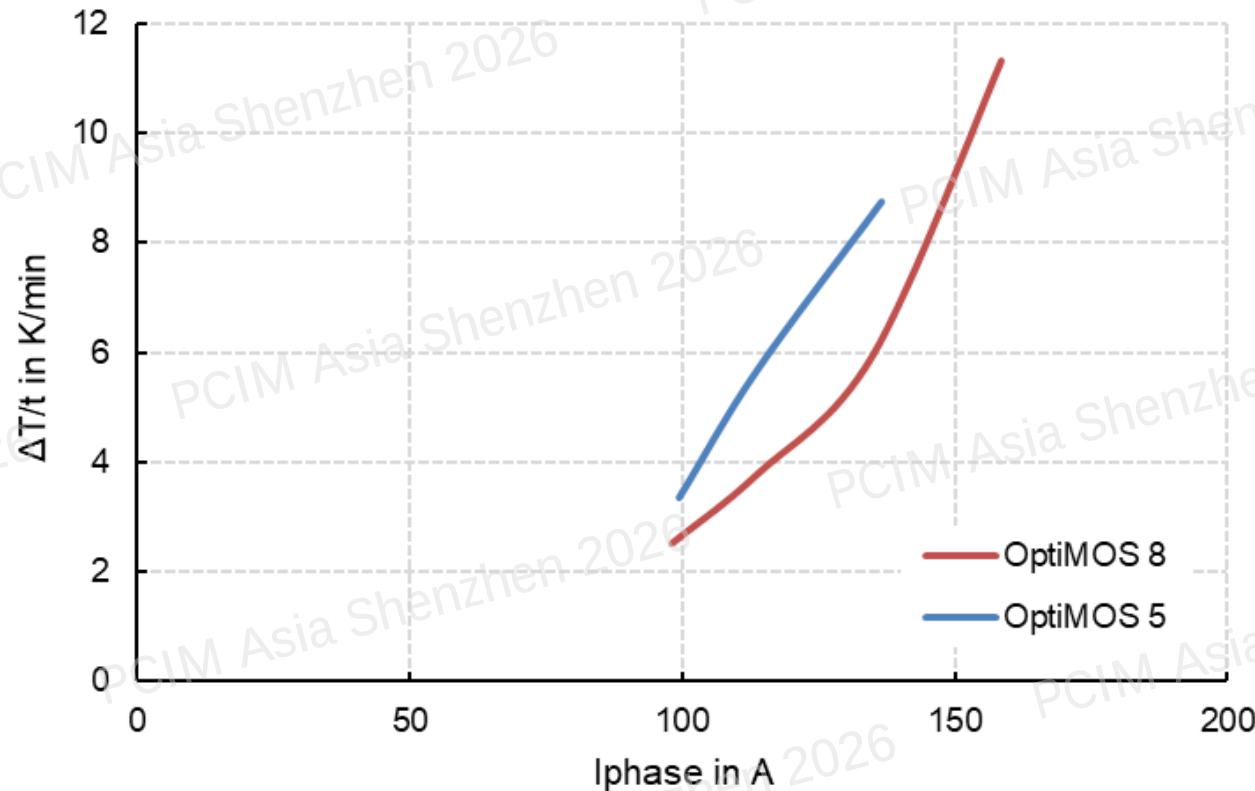
Switching behaviour versus the OptiMOS™ 5 predecessor

- best-in-class devices: IPT009N10NM8 (0.9 mΩ) against IPT015N10N5 (1.5 mΩ)
- first peak-to-valley voltage falls from about 15 V to about 10 V
- 8 % higher inverter output power at identical footprint and case temperature



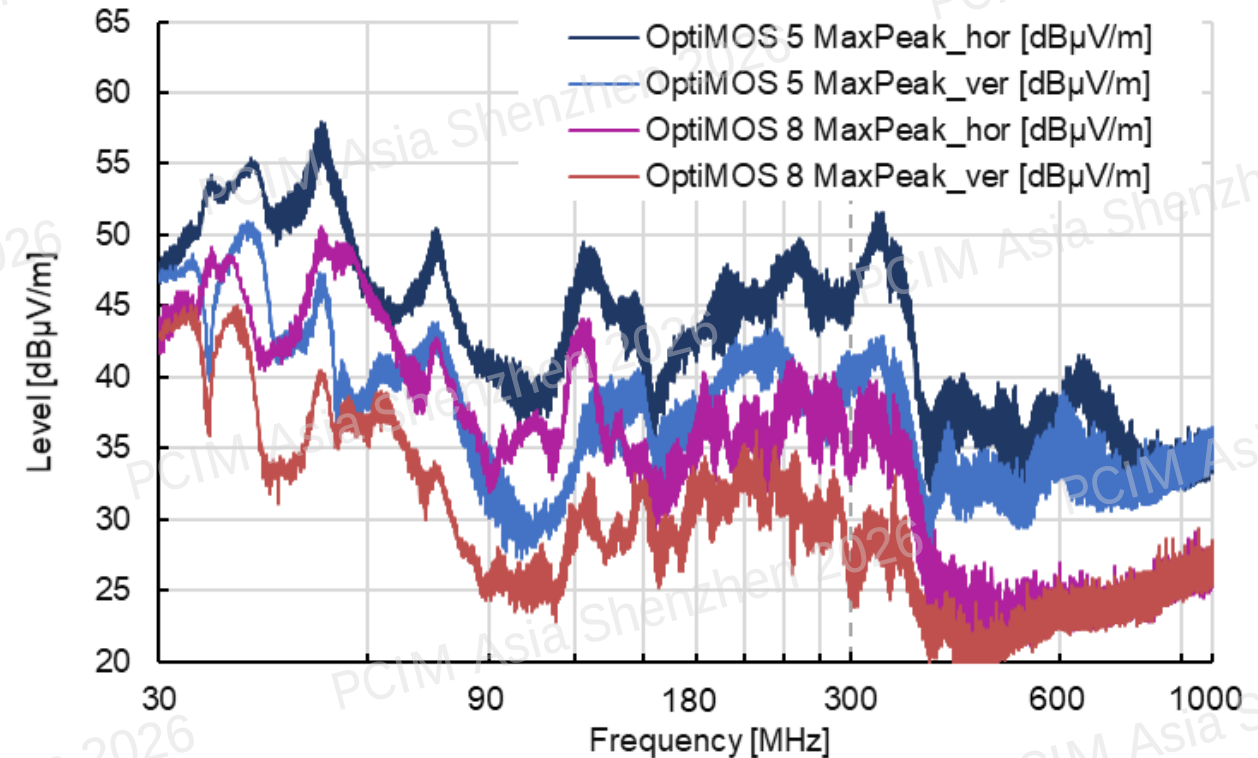
Overload handling capability

- robustness measured as temperature rise rate $\Delta T/\Delta t$ versus phase current
- motor accelerated to 2000 rpm, then mechanically loaded into overload condition
- about 16 % more overload current handled by the new device: 135 A instead of 114 A



Radiated emission according to EN 12895

- lowered emission due to smaller ringing amplitude, stronger damping and reduced dv/dt
- measurements confirm reduced radiated emission over the full test spectrum compared to predecessor device
- meeting the EMC limits gets easier without additional filtering effort

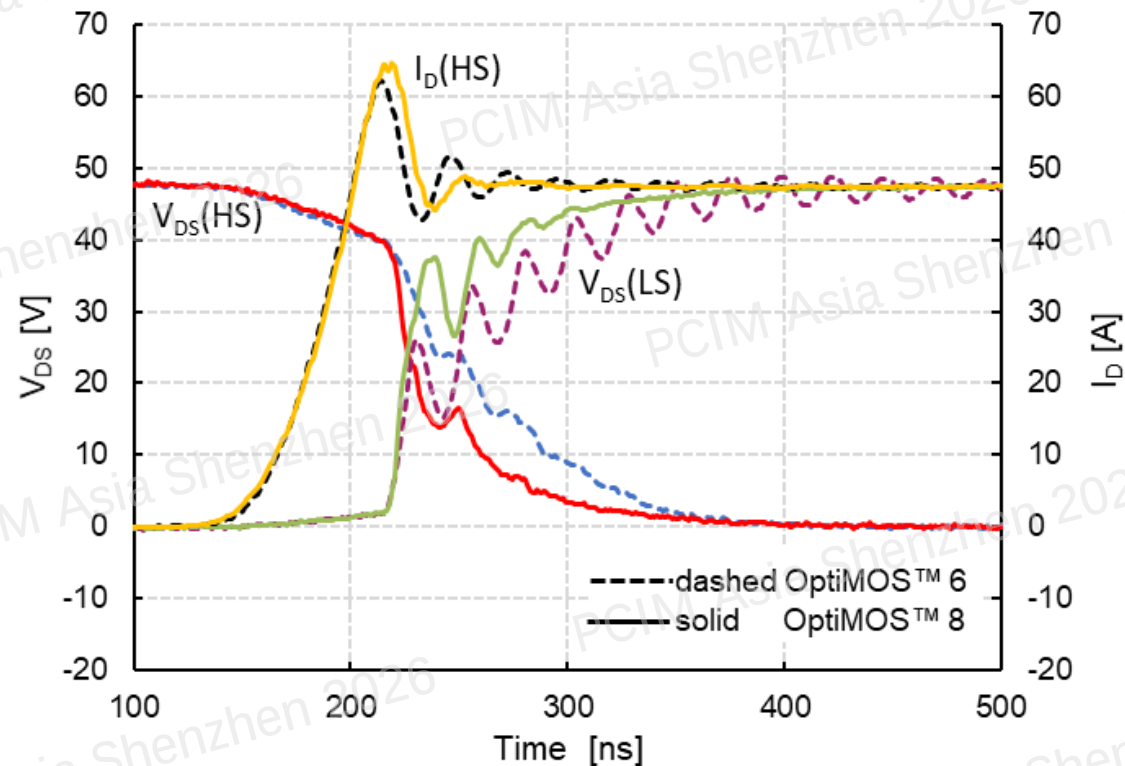


Comparison to a Switching-Optimized Technology

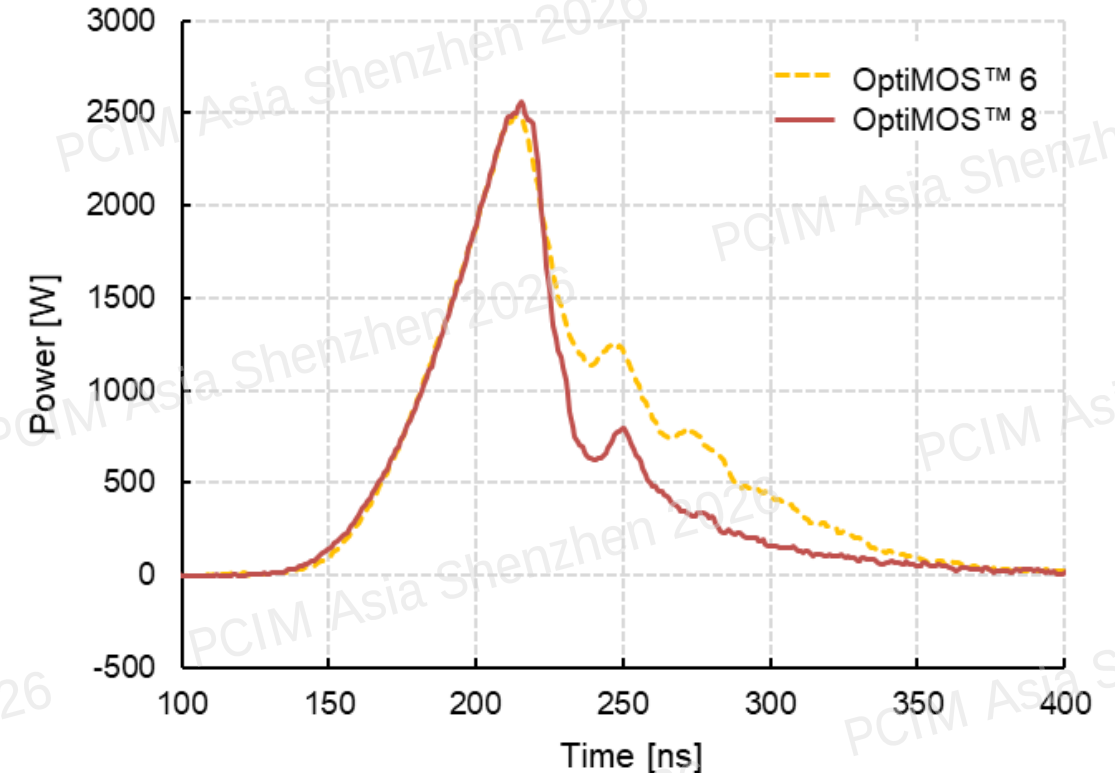
Turn-on: OptiMOS™ 8 vs. OptiMOS™ 6

- ISC019N10NM8 (1.9 mΩ) compared to ISC022N10NM6 (2.2 mΩ),
- dv/dt and di/dt matched
- $V_{DS(HS)}$ transition is faster for the drive-optimized device and the ringing is better damped
- turn-on losses are lower although $Q_{RR} + Q_{OSS}$ is slightly higher

waveforms



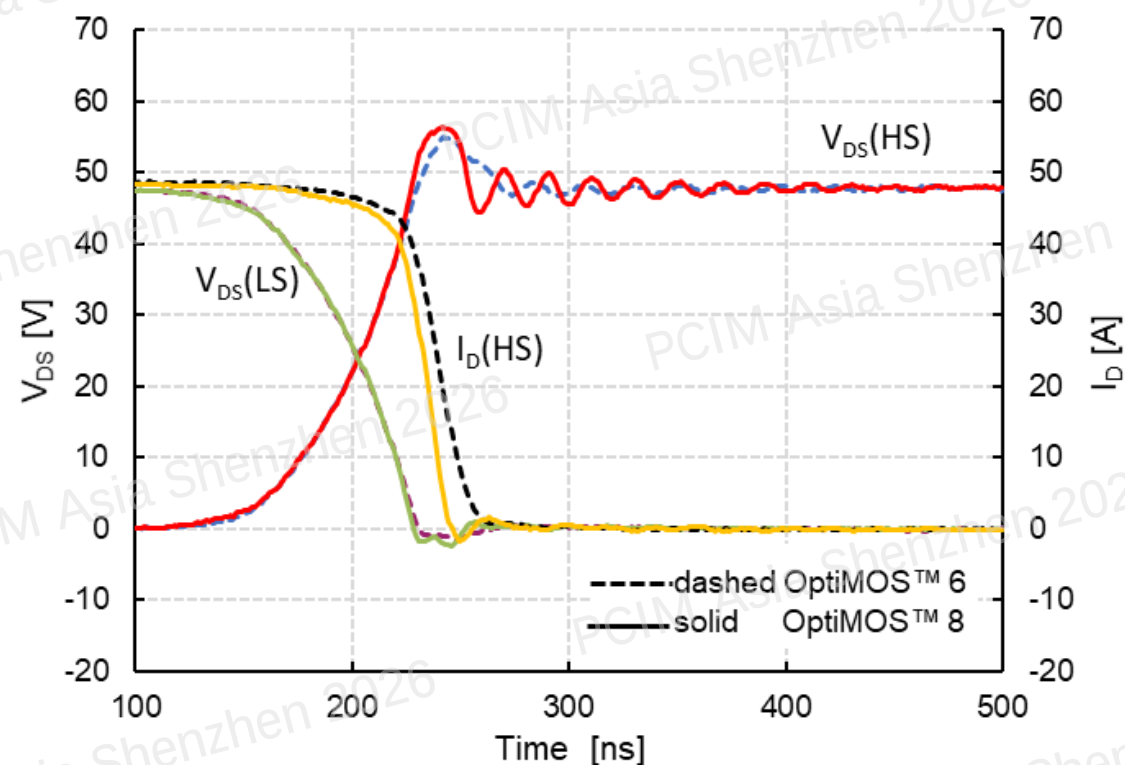
power losses



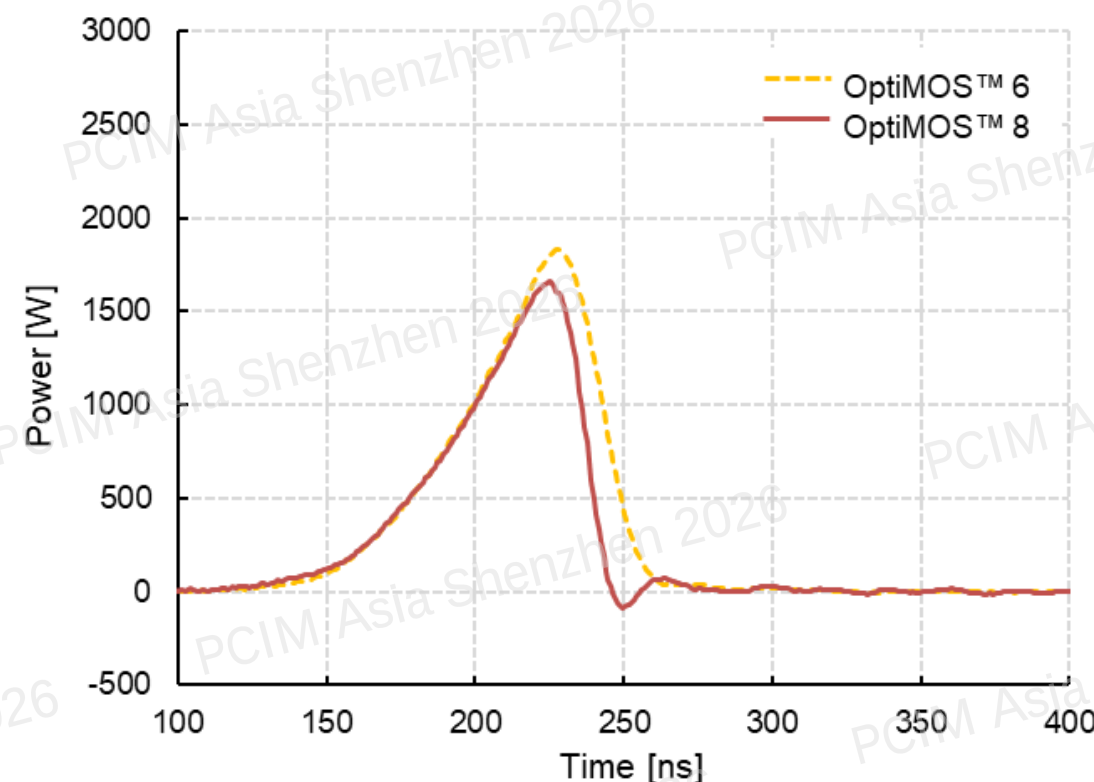
Turn-off: OptiMOS™ 8 against OptiMOS™ 6

- dv/dt of $V_{DS(LS)}$ matches well;
- di/dt of $I_{D(HS)}$ is higher for OptiMOS™ 8
- the higher di/dt causes a slightly larger $V_{DS(HS)}$ overshoot
- turn-off losses are lower for the drive-optimized device

waveforms



power losses



Summary



Summary

- OptiMOS™ 8 100 V integrates a nonlinear snubber into the MOSFET device
- the integrated snubber limits the V_{DS} overshoot and damps the ringing without external components
- avoids additional parasitics in the power loop, saves parts, requires less board area and reduces tuning efforts
- enables the use of smaller gate resistors, with the benefit of reduced the switching losses
- due to the snubber integration, the output capacitance has to be characterized with a charge-based method
- 48 V / 4 kW inverter: 8 % more output power and 16 % more overload current compared to predecessor device
- radiated emission reduced over the full spectrum, measured according to EN 12895

