

All-SiC Power Modules with 3rd-Generation Trench-Gate SiC-MOSFET

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Background & Objectives

- Accelerating SiC adoption in renewables, EVs, railways and AI data centers.
- Strict requirements for higher efficiency and greater power density in power conversion systems.
- **Conventional 2G:** Miniaturization causes electric field concentration on the gate oxide.



Objective:

Develop an **SBD-less All-SiC module** using 3rd-Gen trench-gate MOSFETs to maximize power density and minimize system losses.

Design of 3rd-Generation Trench-Gate SiC-MOSFET

Simplified Architecture:

Partial reduction of p-type diffusion layers to reduce cell pitch.

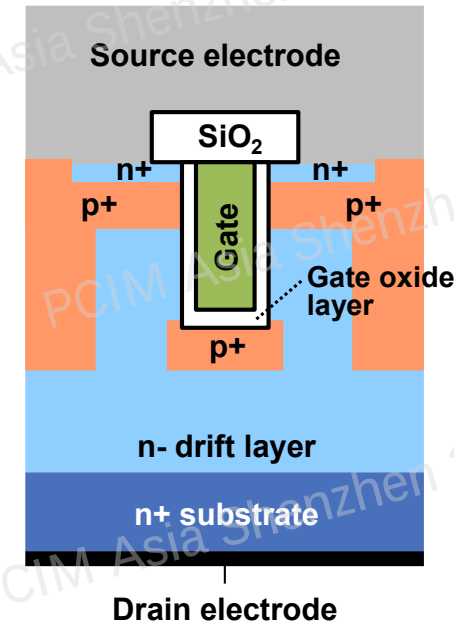
Enhanced Protection:

Optimized p+ layer at the trench bottom to ensure robust gate oxide protection under high-voltage conditions.

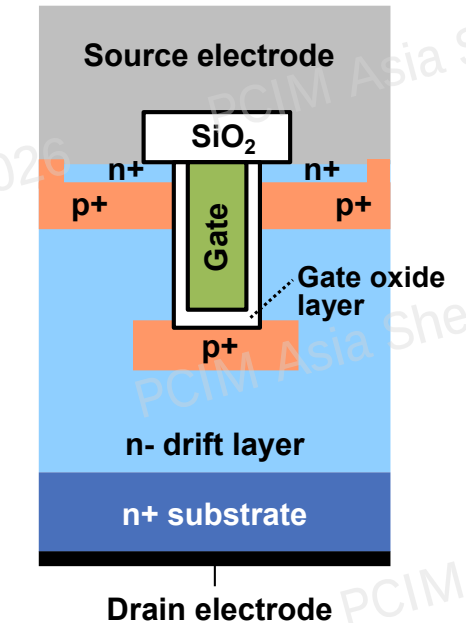
Densification:

Enables higher current capacity per unit area.

2G SiC-MOSFET



3G SiC-MOSFET



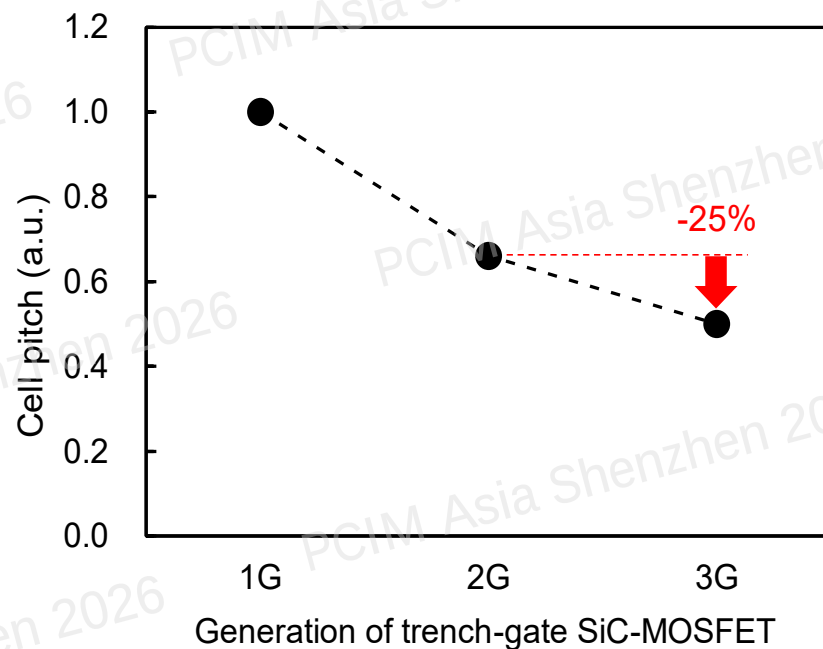
Reduction in On-Resistance

Shrank cell pitch:

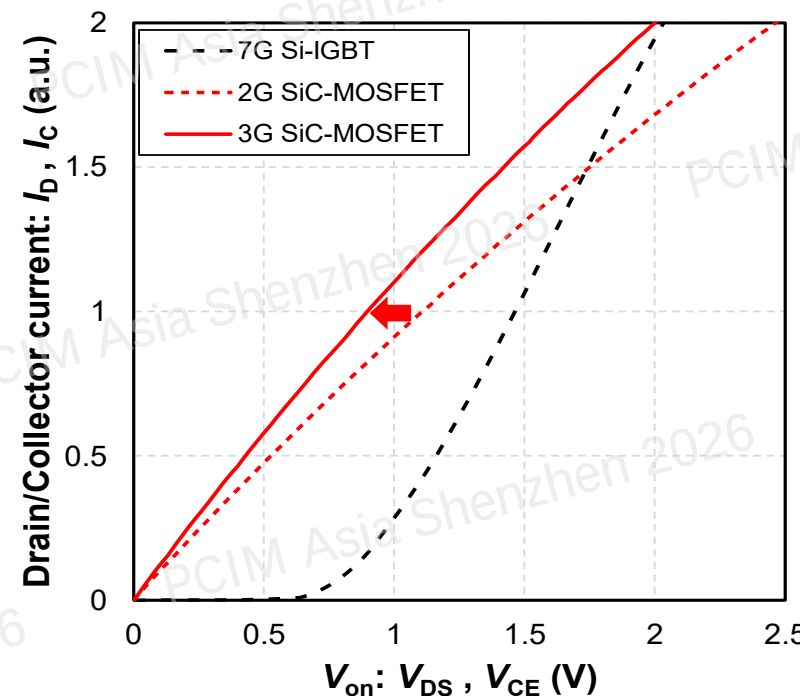
Approx. 25% to achieve higher cell densification.

✓ **23% reduction** in specific on-resistance (R_{onA}) compared to the 2G.

Comparison of cell-pitch size



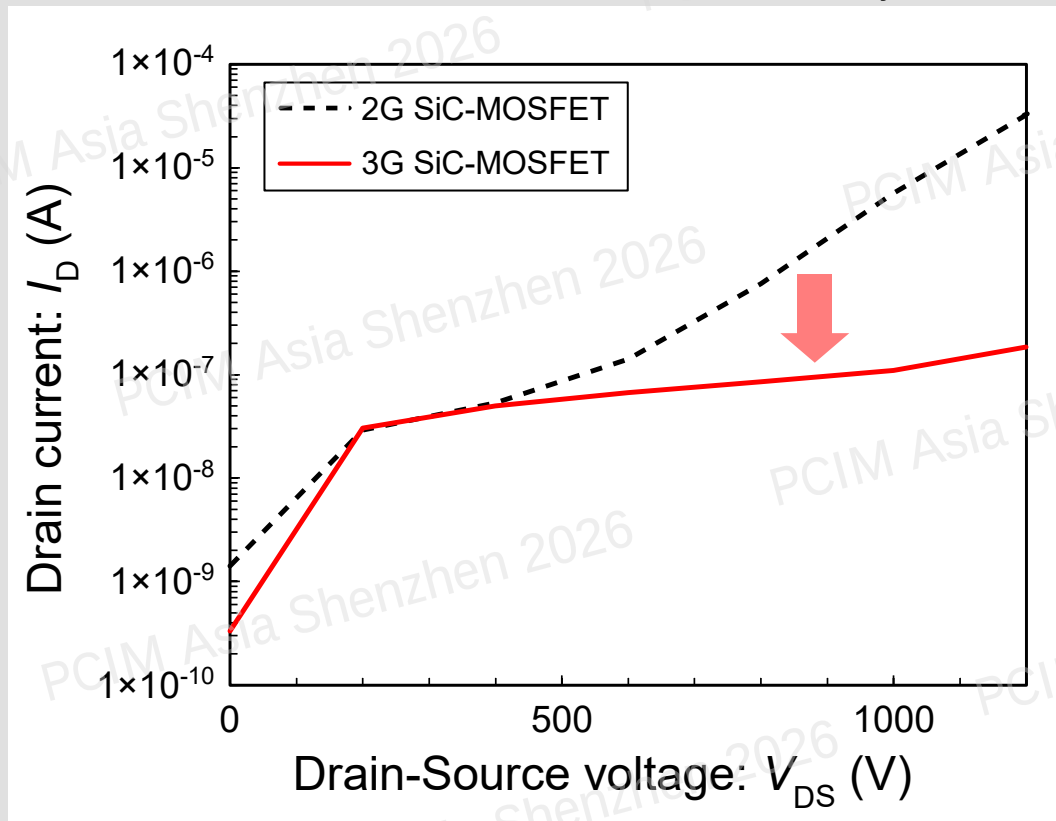
On-state voltage for 1,200V devices @ $T_{vj}=25^{\circ}\text{C}$



Blocking Characteristics in Off-State

- Mitigated electric field strength and lowered leakage current after miniaturization by optimizing p+ layer geometry and doping concentration.
- Maintained stable blocking capability up to 1200V, achieving lower leakage current I_{DSS} than 2G devices in the high-voltage region (>500V).

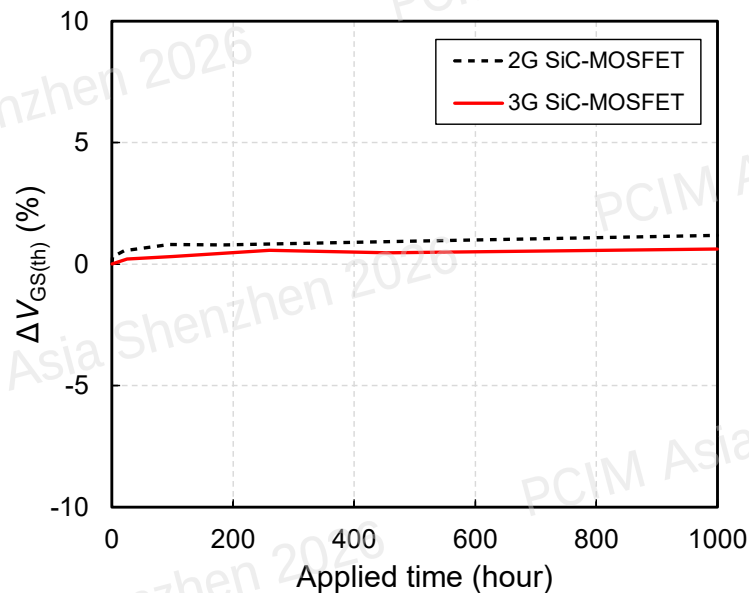
Leakage current for 1,200V devices @ $T_{vj}=25^{\circ}\text{C}$



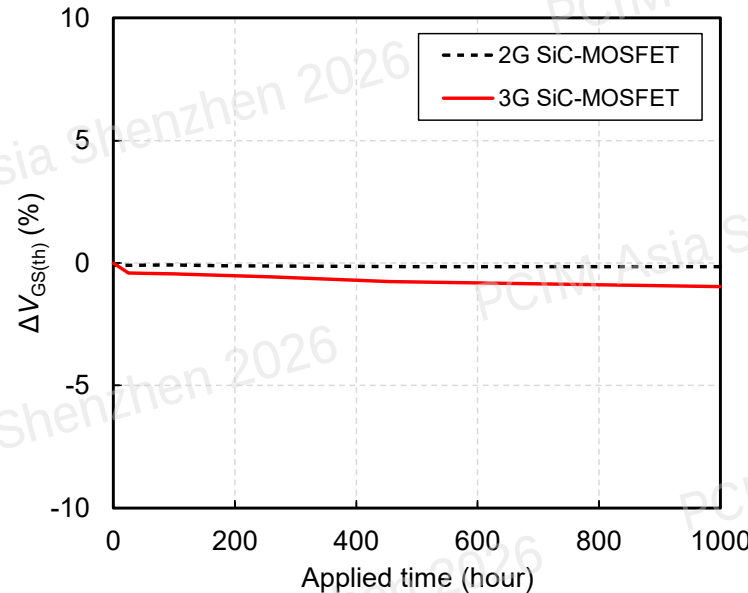
Reliability Evaluation under Gate Bias Stress

- ✓ Conducted positive/negative DC bias and AC switching stress tests under harsh conditions at 175°C.
- ✓ Suppressed $V_{GS(th)}$ shift to less than 1% even after 1000 hours via interface state control, achieved excellent long-term stability.

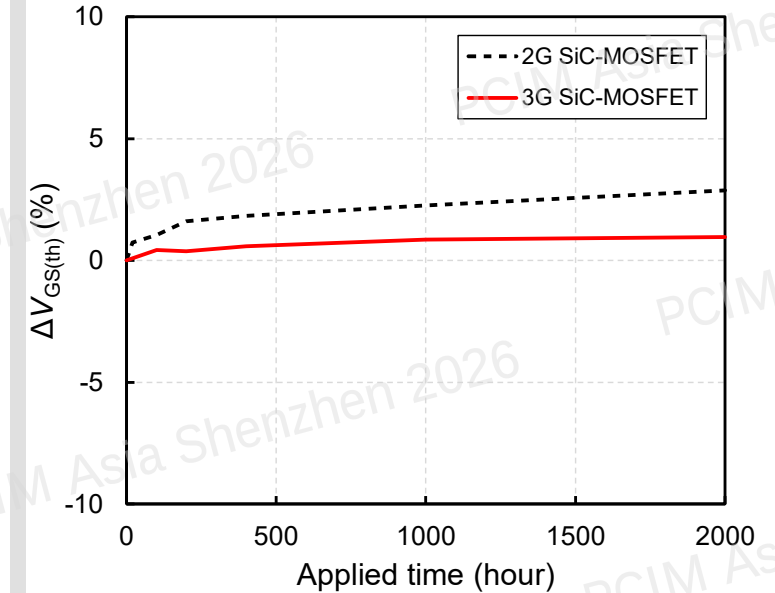
Under +DC bias



Under -DC bias



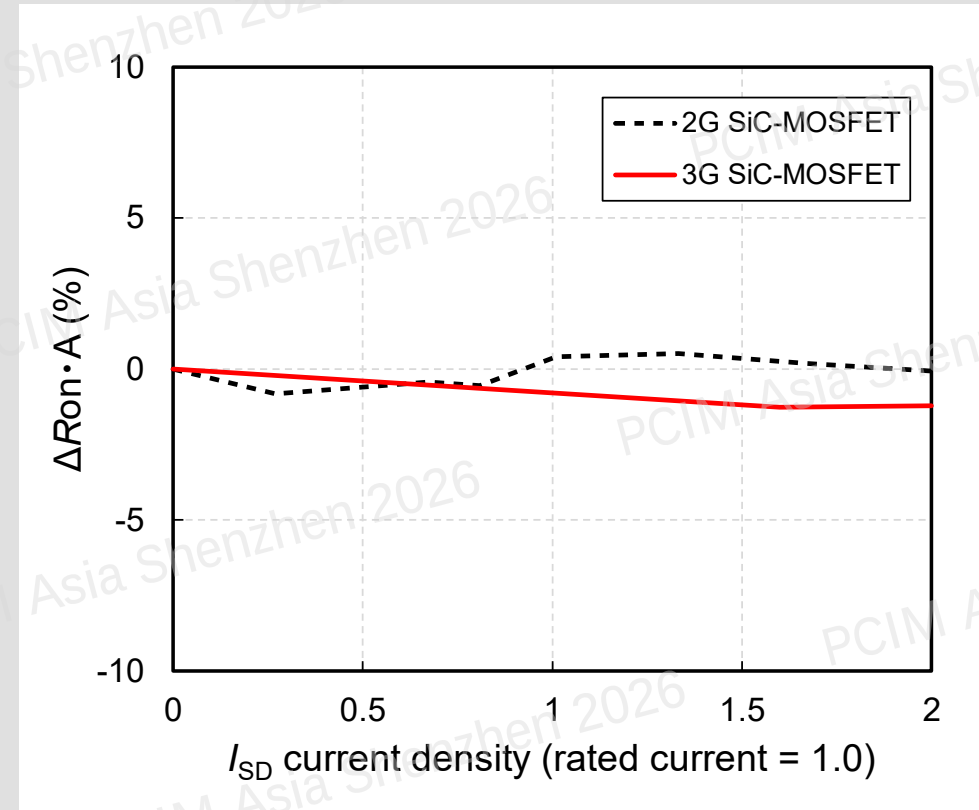
Under AC switching



Suppression of Body-Diode Degradation

- Suppressed bipolar degradation caused by crystal defects using a novel hole density control technology.
- ▼
- ✓ **< 2% $R_{on}A$ increase** even after reliability testing at twice the rated current density.
 - ✓ **Enables "SBD-less"** configuration by eliminating external SBDs, contributing to effective footprint utilization and higher current ratings.

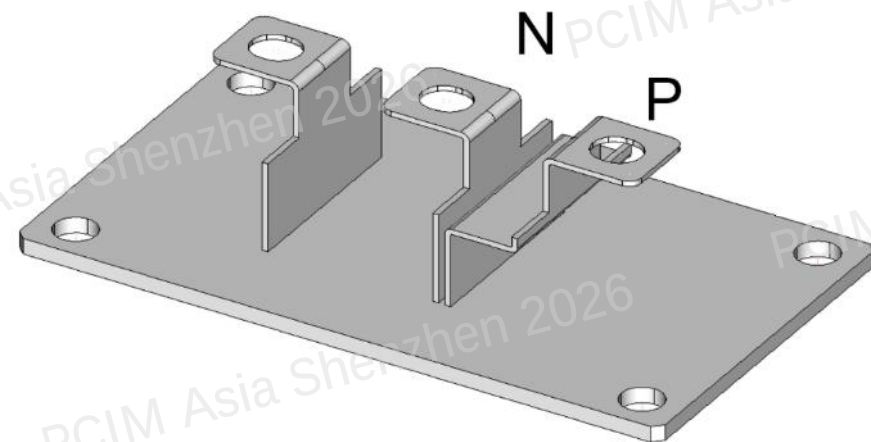
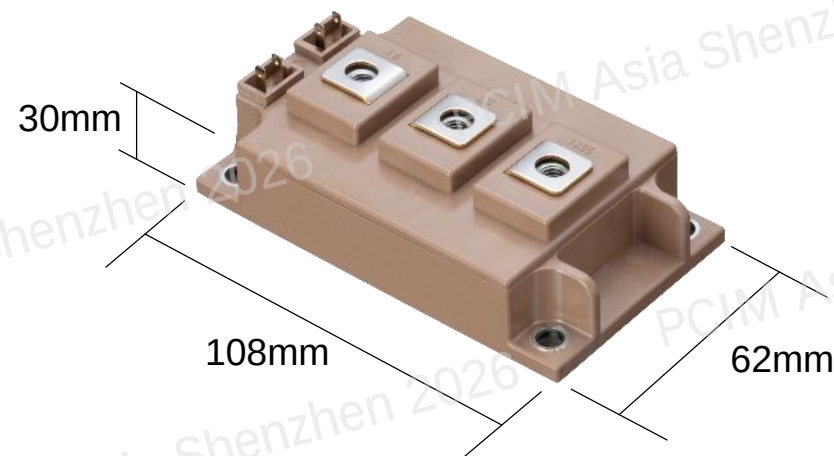
RonA shift vs. body-diode current



Low-Inductance Design of Package

Laminated Terminal Structure:

Applied to standard 62mm package to minimize parasitic effects.

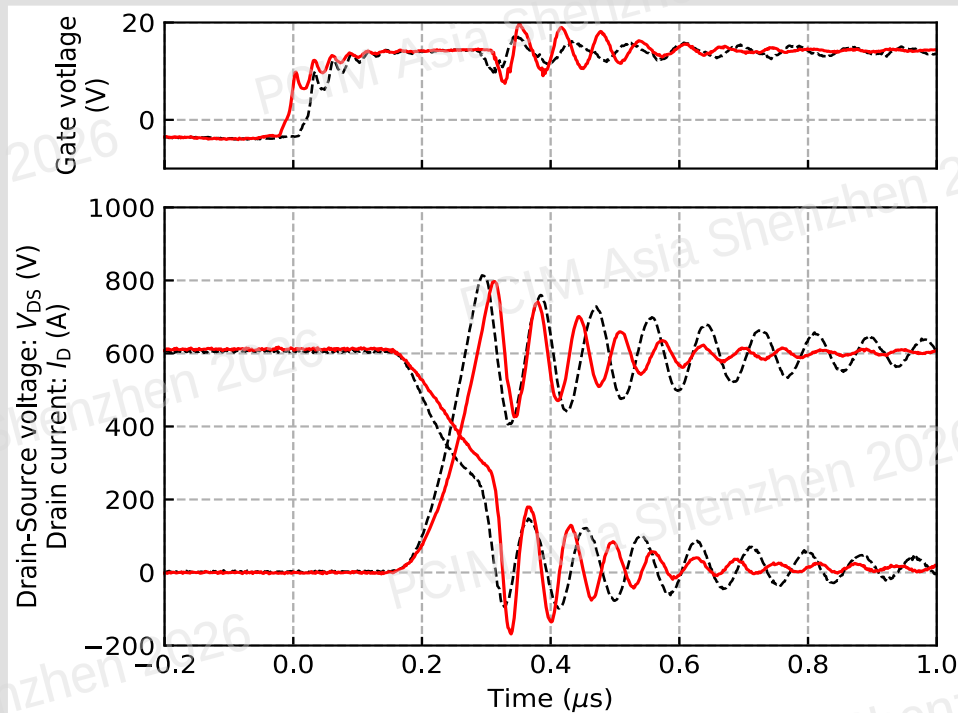


- ✓ **24% Reduction** in internal inductance compared to conventional designs by utilizing electromagnetic mutual induction.
- ✓ **Stable switching** behavior and suppressed parasitic ringing through stray inductance reduction.

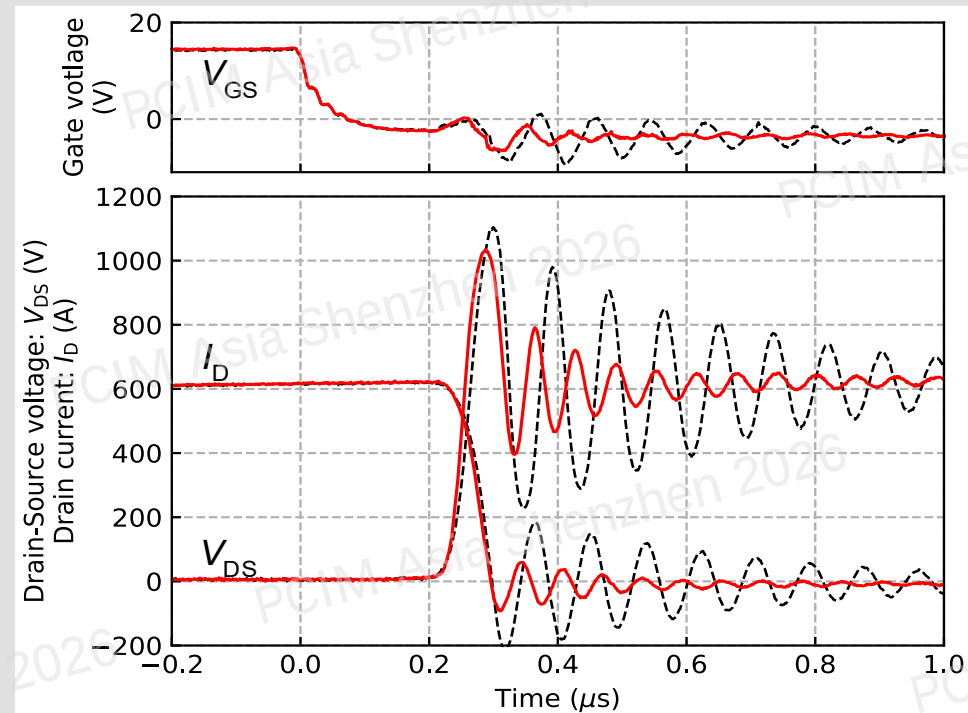
Evaluation Results of Switching Characteristics

- ✓ Confirmed highly stable operations and significantly suppressed parasitic ringing despite the SBD-less configuration.
- ✓ Decreased turn-off surge voltage from 1101 V to 1028 V, successfully expanding the Safe Operating Area (SOA).

Turn-on switching

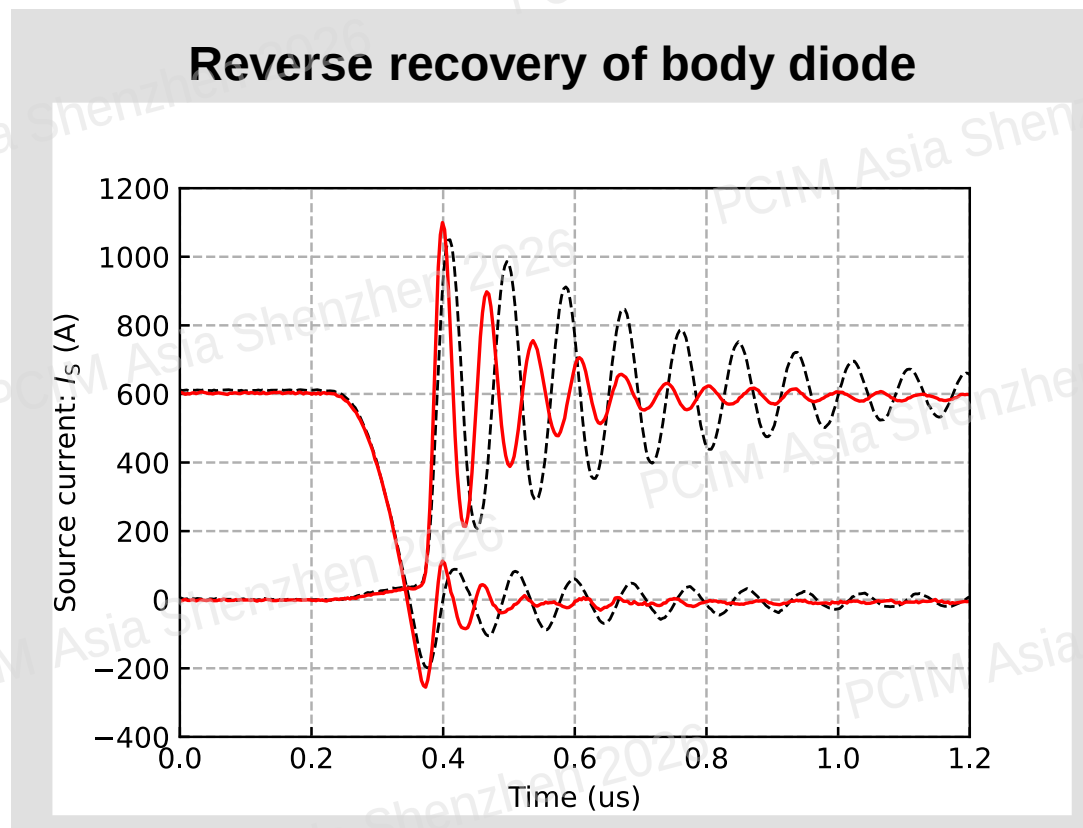


Turn-off switching



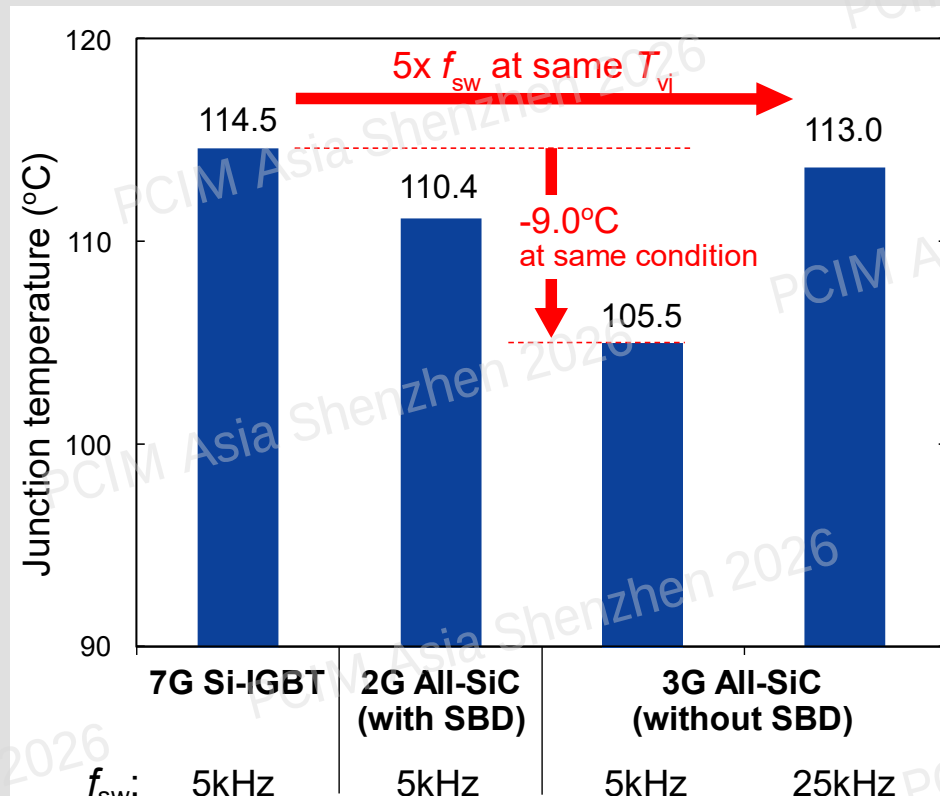
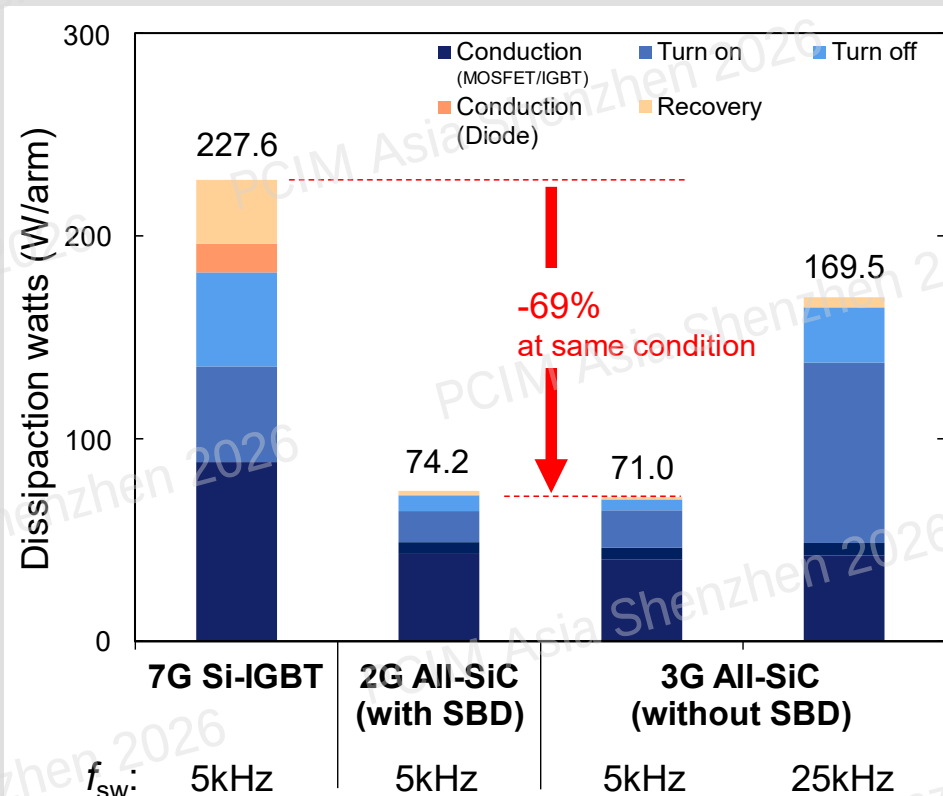
Reverse Recovery in SBD-less Configuration

- ✓ Reduced reverse recovery energy E_{rr} by 25% (from 1.2 mJ to 0.9 mJ) during commutation utilizing MOSFET third-quadrant conduction.
- ✓ Achieved effective ringing suppression without inducing abnormal voltage or current spikes.



Comparison of System Loss and Thermal Performance

- ✓ **~70% lower switching loss** compared to conventional Si-IGBTs.
- ✓ **9.0°C lower T_{vj} , (or 5x higher frequency)** compared to the Si-IGBT.
- ✓ **Lower total loss than the 2G** as conduction loss reduction outweighs the slight increase in switching loss.



Product Lineup Expansion of All-SiC Modules

- ✓ **Expanded current ratings** by installing extra MOSFET chips into the space saved by eliminating external SBDs.
- ✓ Delivered high-capacity ratings, including 1200V / 800A and 1700V / 600A, within a standard 62mm package.

Voltage	Gen	Rated current (R_{DSon} @25°C)			
		300A (3.0mΩ)	450A (2.0mΩ)	600A (1.5mΩ)	800A (1.2mΩ)
1200V	2G	●	●	●	
	3G	●	●	●	●

Voltage	Gen	Rated current (R_{DSon} @25°C)			
		200A (5.0mΩ)	300A (3.3mΩ)	400A (2.5mΩ)	600A (1.7mΩ)
1700V	2G	●	●	●	
	3G	●	●	●	●

Product Lineup for High Voltage Class

- Extend the 3G trench technology platform to 2.3kV and 3.3kV high-voltage classes.
- Future rollout: Launching a lineup of high-voltage, high-capacity modules housed in HPnC packages.



**HPnC (High Power new Core) package for
1.7kV, 2.3kV and 3.3kV All-SiC modules**

- Achieved a 23% reduction in $R_{DS(on)}$ through the 3rd-generation trench-gate MOSFET technology.
- Secured high long-term reliability in the SBD-less architecture by successfully suppressing the body-diode degradation.
- Expanded current ratings and maximized module-level power density by adopting a stable SBD-less architecture.
- Significantly contributes to higher efficiency and design flexibility in next-generation power conversion systems.

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Thank you for the attention!